Thuc Nguyen

thuchngu@bu.edu
https://www.linkedin.com/in/thucnguyen61098
https://github.com/thuchgnu

17 Aberdeen St. Apt 6
Boston, MA 02215
845-416-8037

Technical Skills

•**Programming** C, C++, Java, Python, Arduino, Verilog, MIPS, LaTex

•**Other** Linux/UNIX, Git, EAGLE, KiCAD, Atmel Studio, Xilinx ISE Design Suite

Work Experience

•**Boston University Center for Space Physics** *Research Assistant - ANDESITE Software Team* May 2018 - Present
Test and debug satellite code, analyze PCB schematics, test main sensors and electrical hardware on satellite

•**Mugar Memorial Library** *Library Assistant* September 2016 - December 2017
Check-in and check-out interlibrary loan items, prepare items to be shipped to other libraries

•**Town of Esopus Library** *Library Page* June 2013 - March 2016
Place returned items on the shelf, pull on-hold items off of the shelf, check-in and check-out items

Education

Boston University - *Bachelor of Science in Computer Engineering*
September 2016 - May 2020(anticipated)
GPA: 3.20/4.00

Relevant Coursework

Computer Architecture - Computer Organization - Introduction to Logic Design - Advanced Data Structures - Applied Algorithms - Introduction to Software Engineering - Introduction to Engineering Computation - Introduction to Electronics - Electric Circuits - Introduction to Engineering Design

Projects

•**Custom Mechanical Keyboard** *Personal Project*
A mechanical keyboard PCB designed from scratch in KiCAD with a custom layout designed in keyboard-layout-editor(project is still in progress).

•**Lamp Post Mounted Flood Detector** *Final Project for Engineering Design Course*
A water level detector composed of an arduino, an ultrasonic distance sensor, an XBee radio module, and a float switch. The system outputs the water level to a hypothetical relay station and then outputs a warning message once the level has reached or surpassed 1 ft.

•**Verilog Digital Lock** *Final Project for Logic Design Course*
A digital lock that utilizes a seven-segment display and a series of switches on an FPGA board that allow a user to input a password to unlock the lock, change the password, and lock the digital lock. The lock was programmed in Verilog and simulated using Xilinx ISE Design Suite.