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IoT-oriented RISC-V-based SOTB-65nm System-on-Chip Implementations

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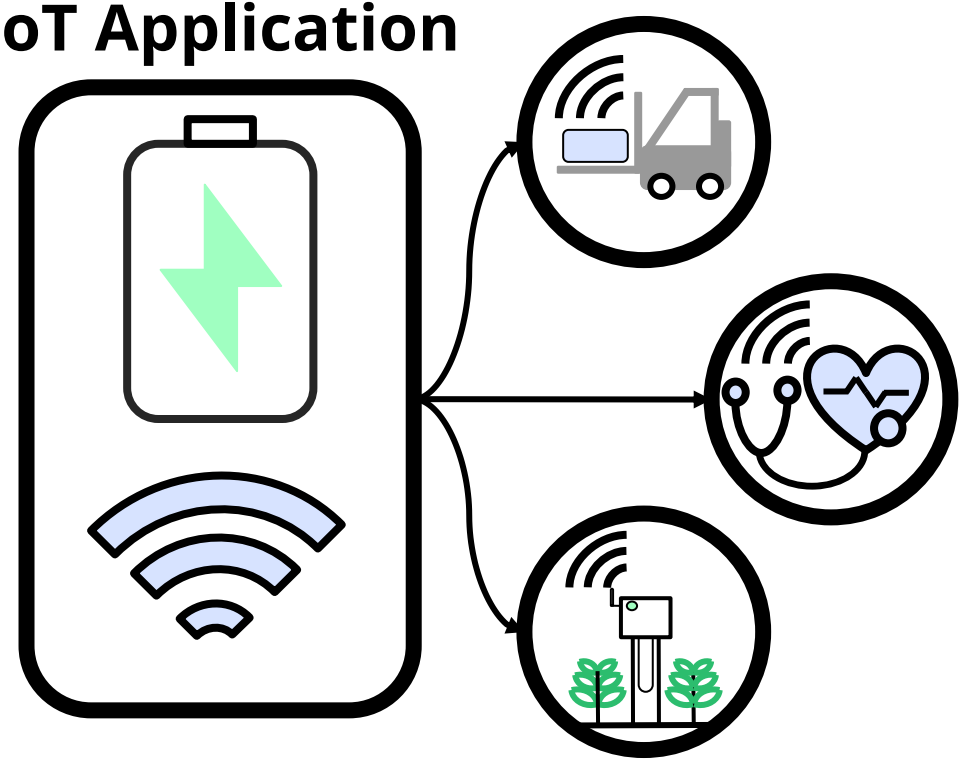
Outline

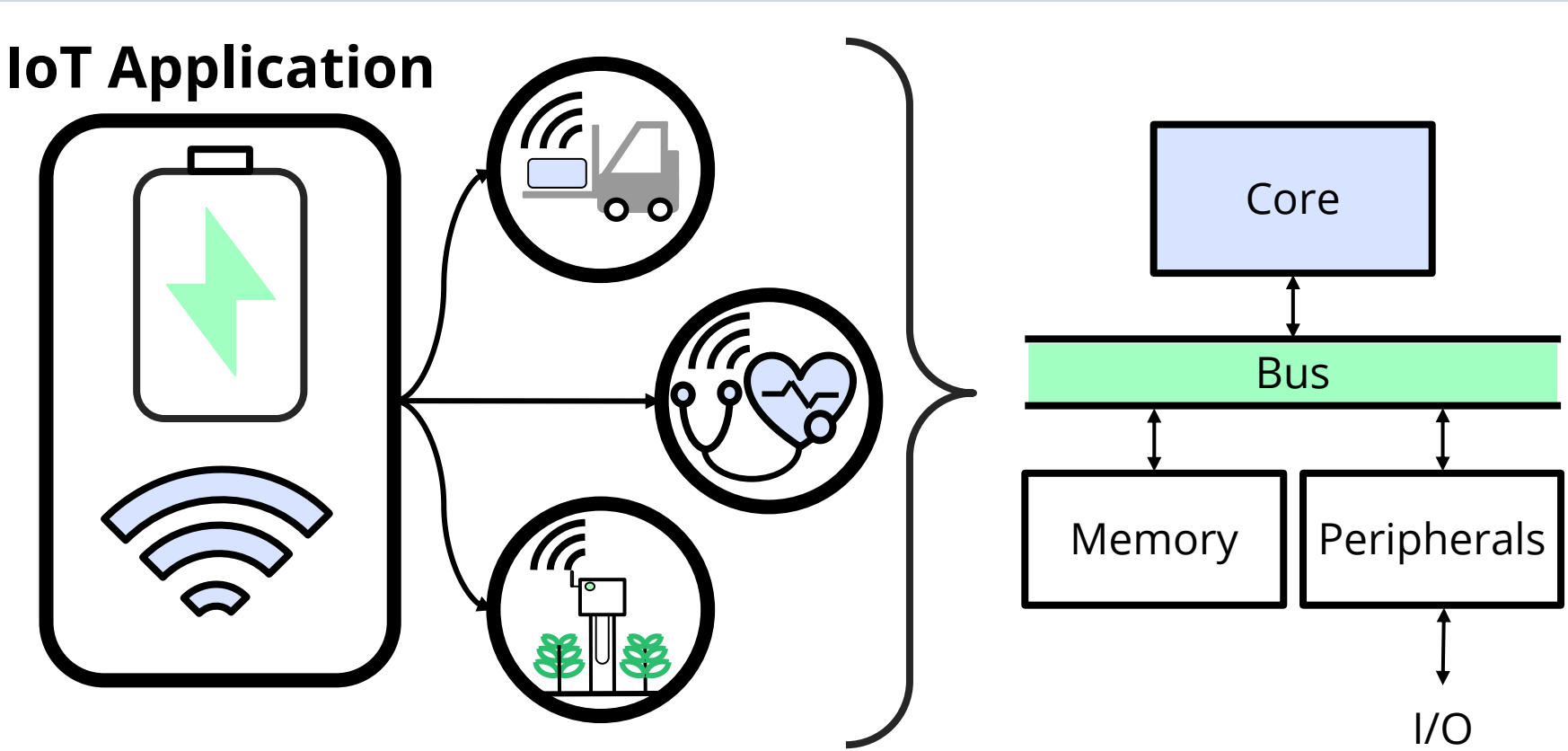
- Introduction
- System On Chip
  - System Architecture
  - Core Architecture
- Measurement and Results
- Conclusions

Introduction

IoT Application



Introduction



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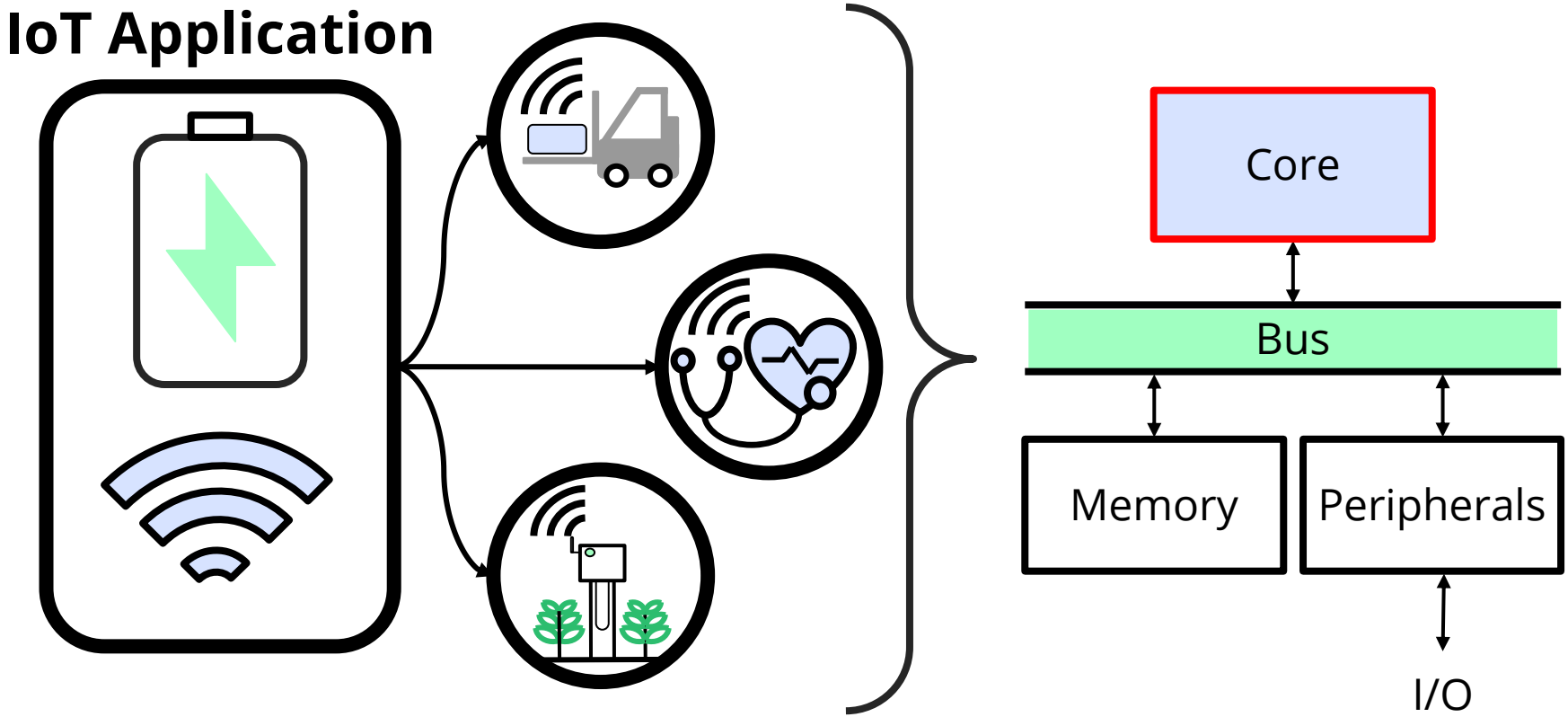
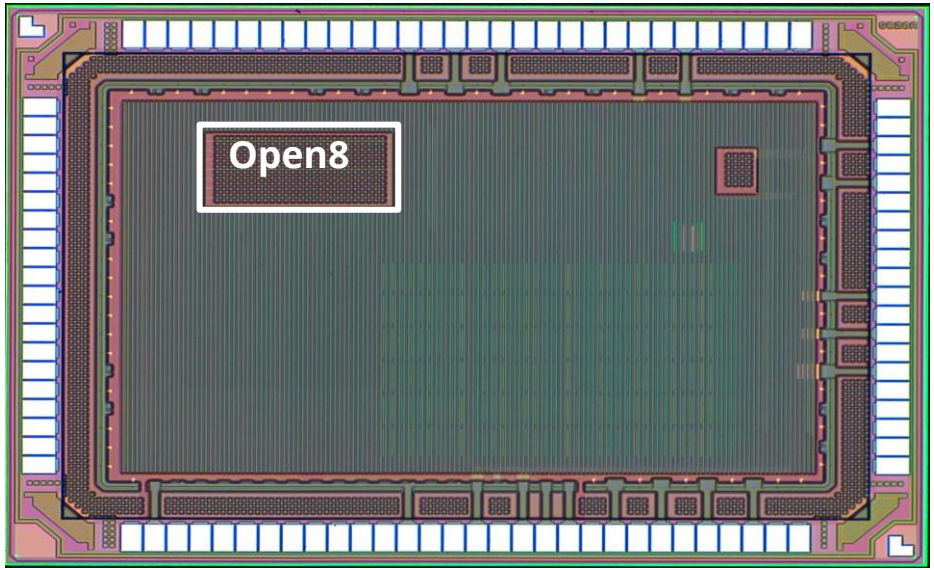
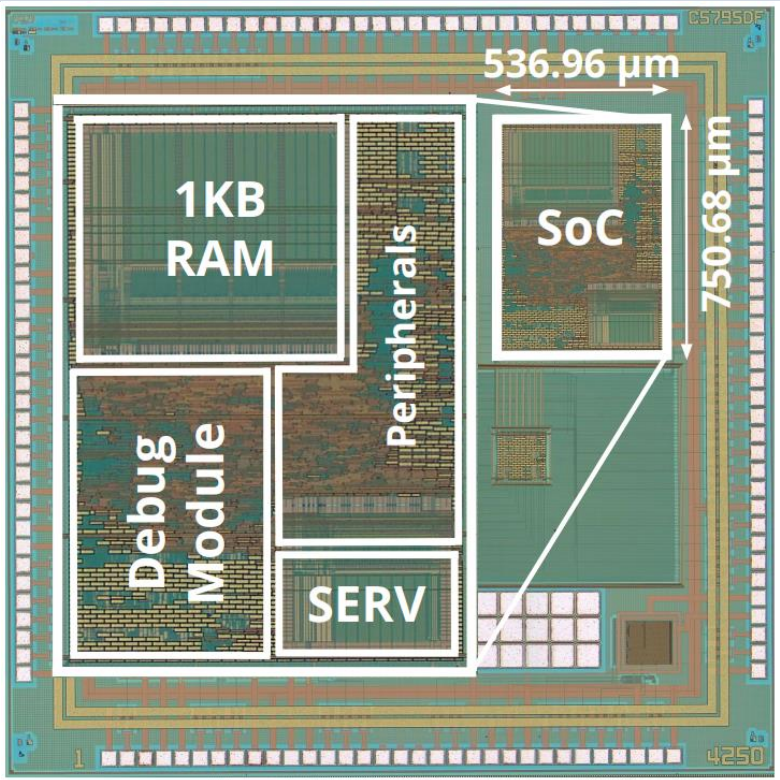


Introduction



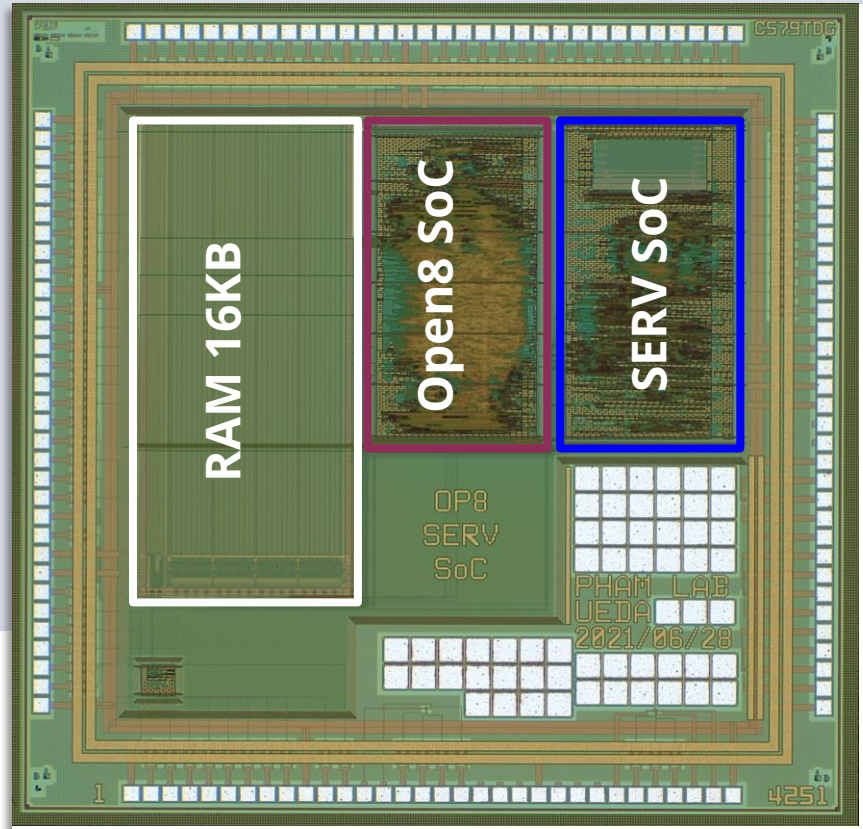
[1] 8-bit Processor in SOTB 65nm



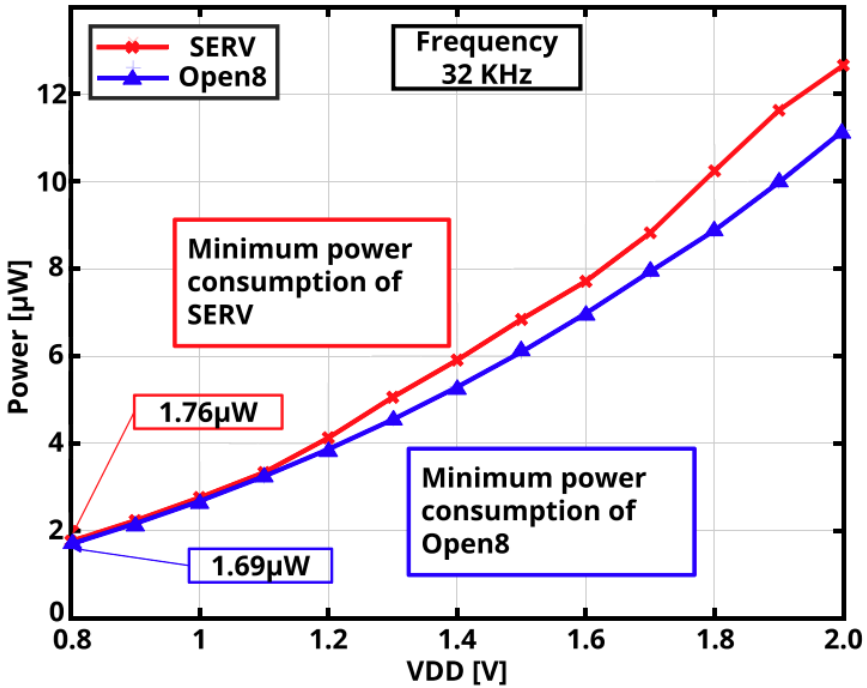
[2] 32-bit RISC-V SERV in 0.18µm.

[1] M. Sarmiento et al., IEEE TCAS-II, 2021.
[2] R. Serrano et al., ISOCC, 2021.

Introduction



[3] 8-bit and 32-bit in 0.18µm CMOS.



Power consumption of the SoCs at 32-kHz and different VDD.

[3]M. Sarmiento et al., IEEE TCAS-II, 2022.

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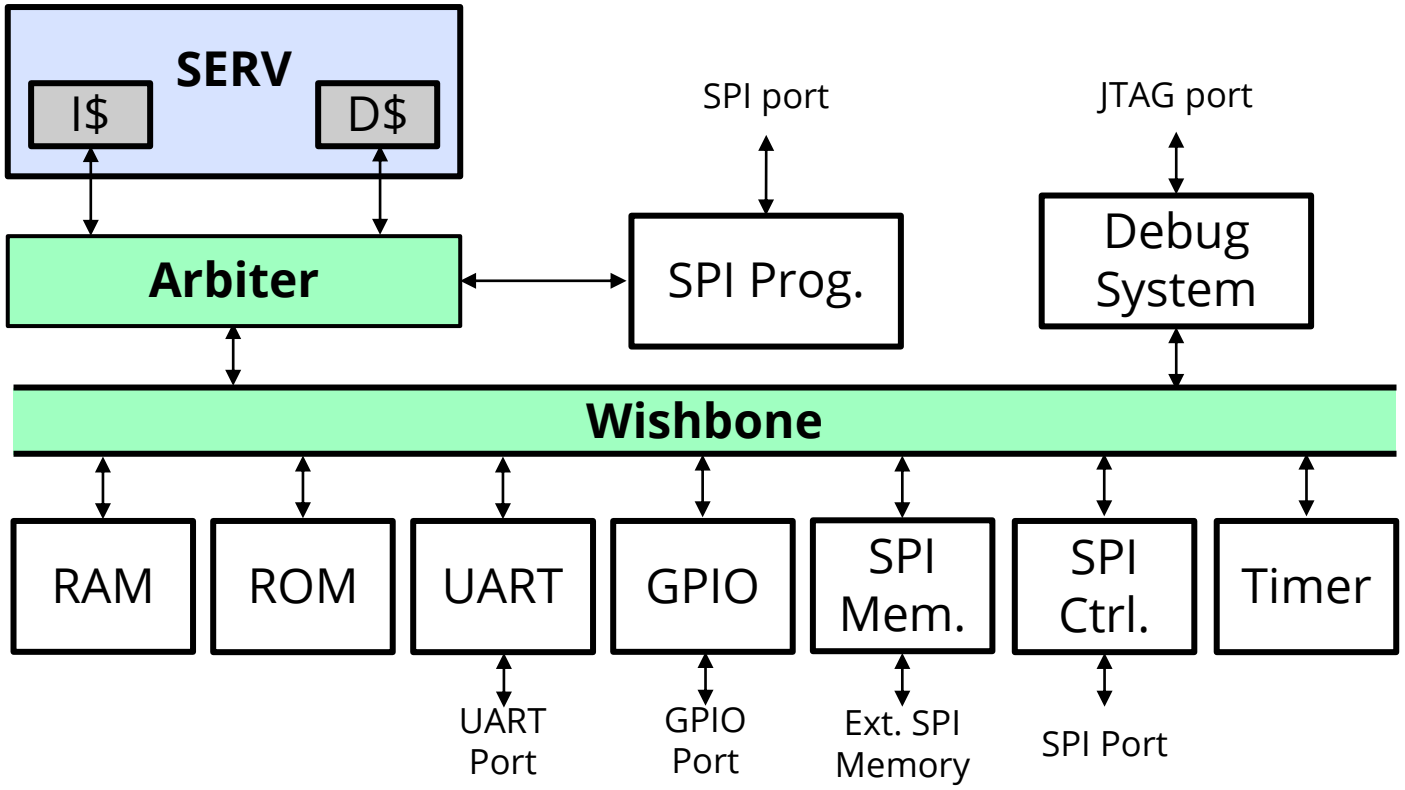
System Architecture



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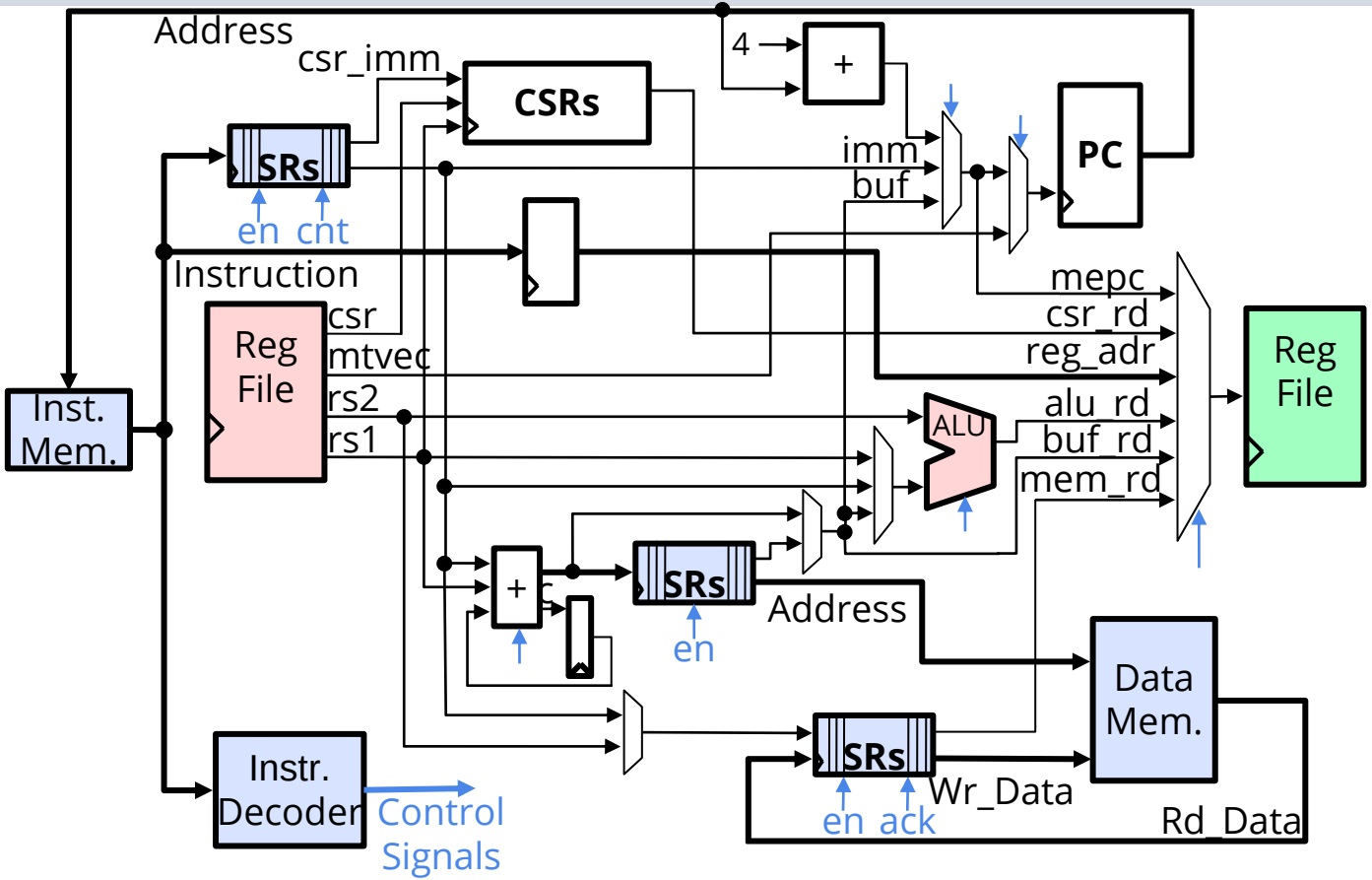
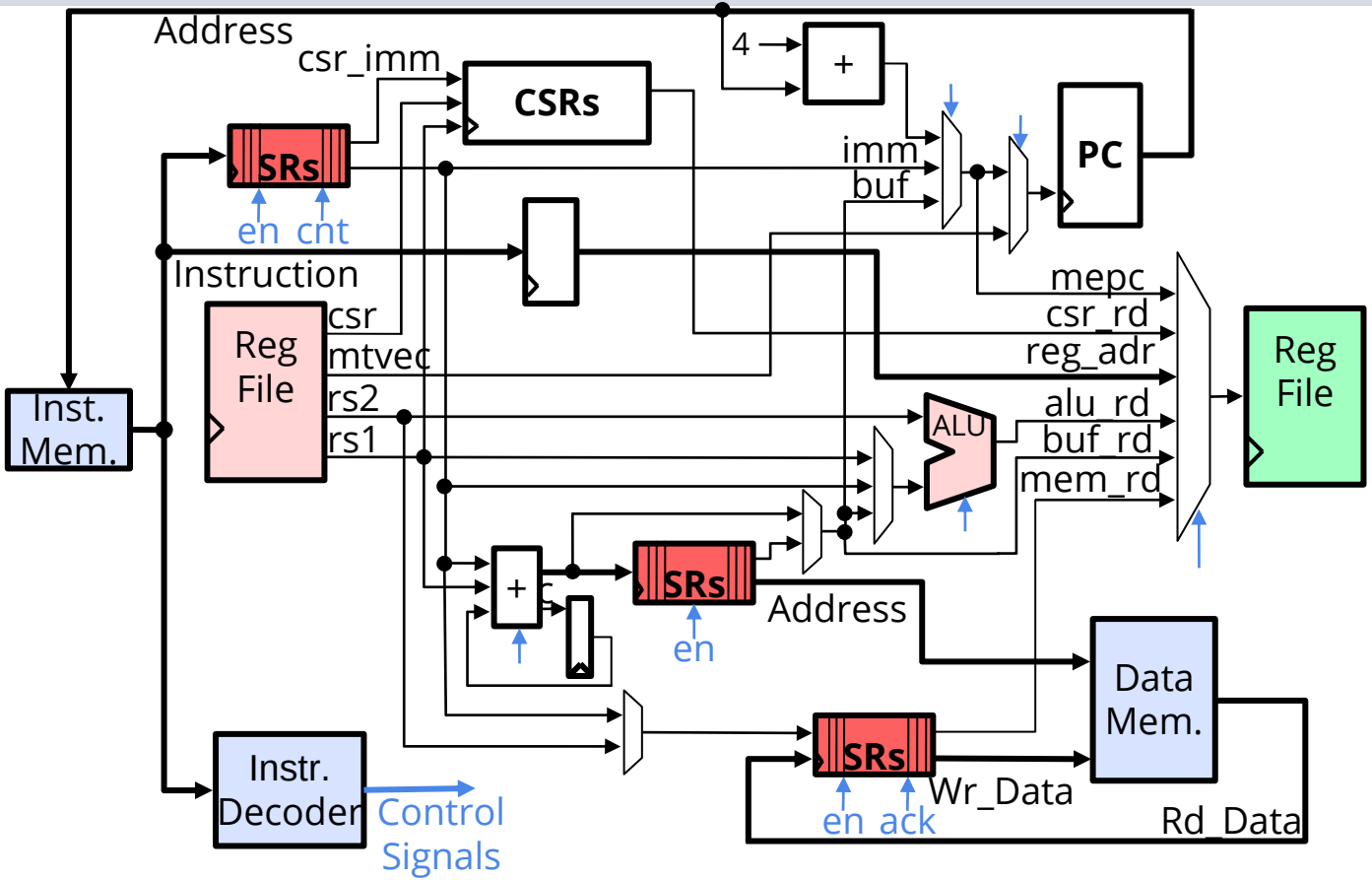
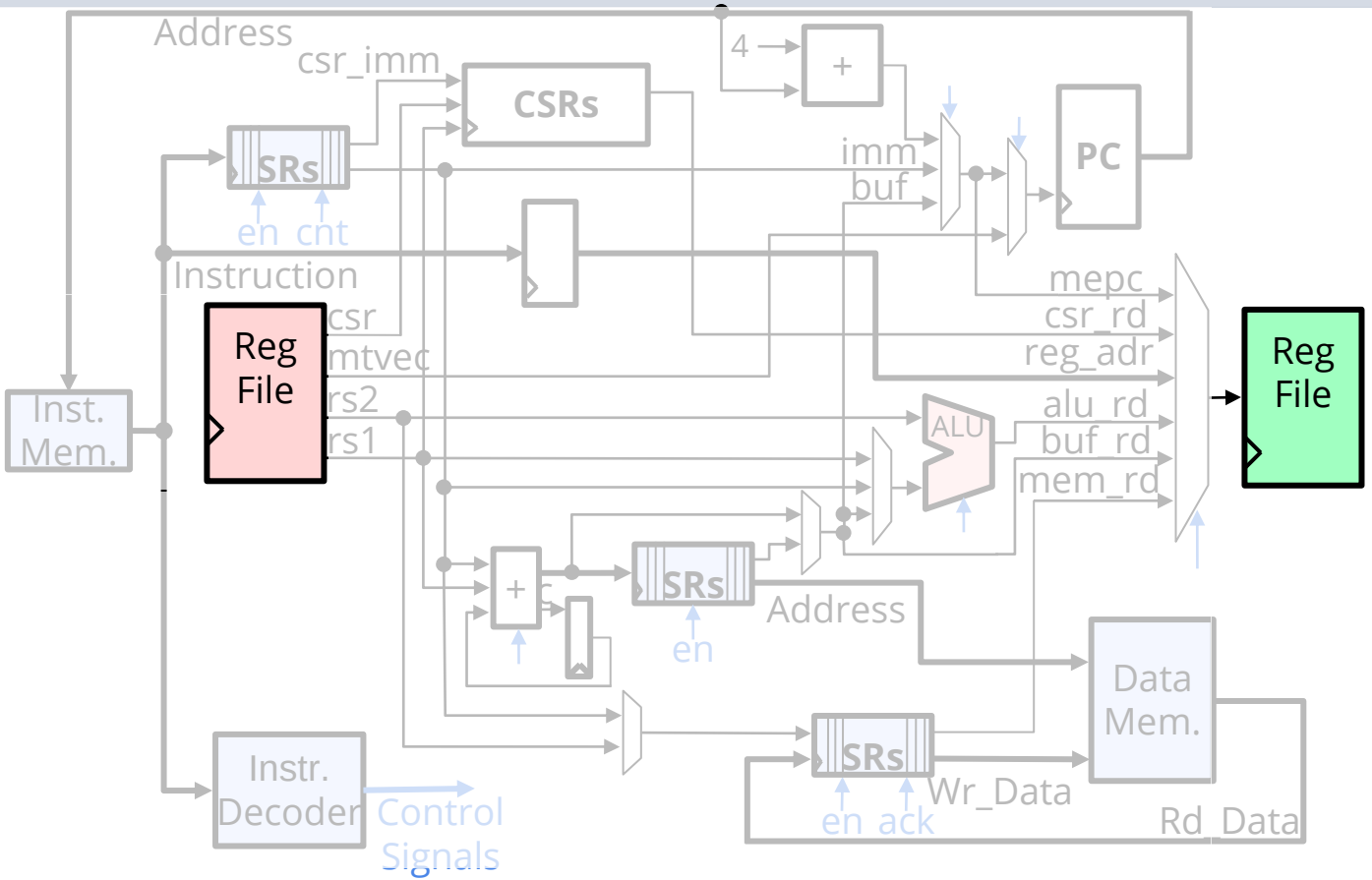
Core Architecture



Core Architecture



Core Architecture



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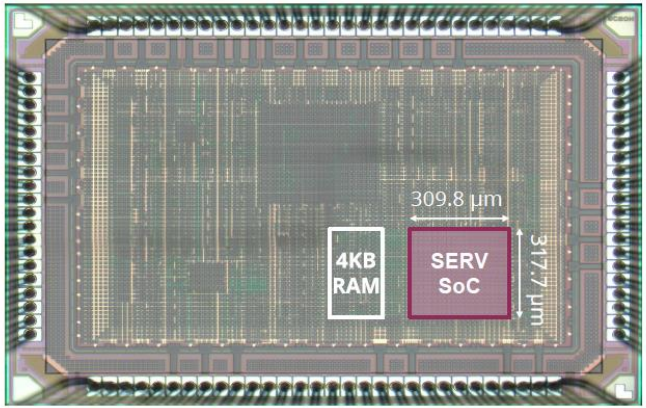
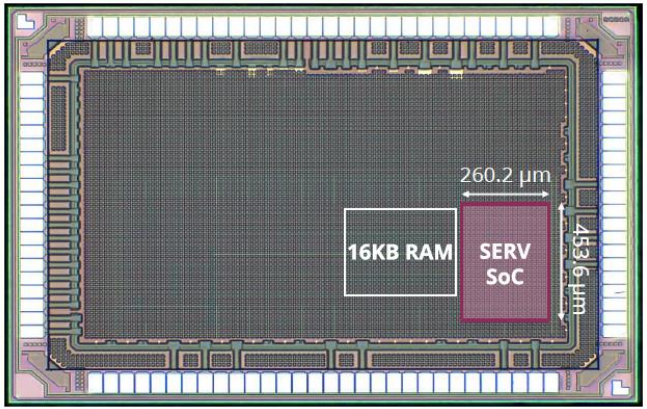
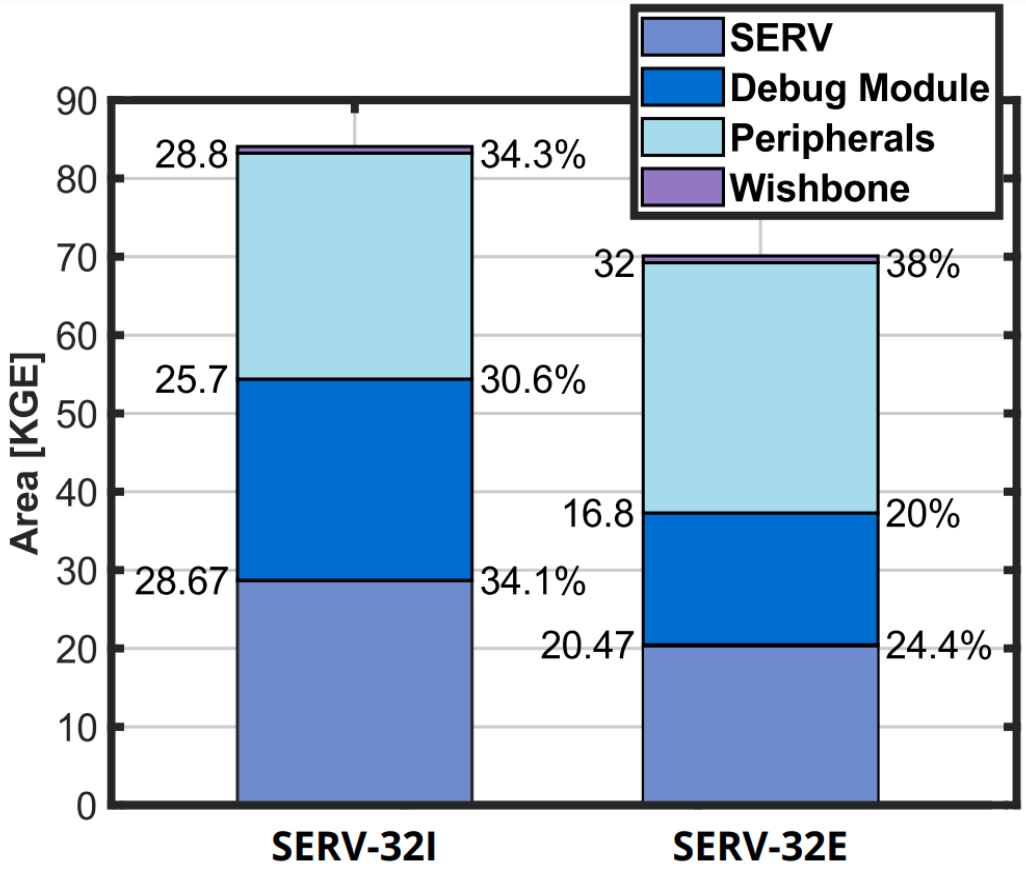
Measurement and Results

VDD:0.27V~1.2V VBB: -2.0V~2.0V	Operating Voltage	VDD:0.27V~1.2V VBB: -2.0V~2.0V
98,423	Area[μm2]	118,026
~70,000	Gate Count	~84,000
11kHz~30MHz	Operating Frequency	10kHz~30MHz
VDD: 0.27V ~ 1.1V VBB: -2.0V ~ -0.4V	Sub-μW Operating	VDD: 0.27V ~ 0.9V VBB: -2.0V ~ -0.4V
SERV-32E	Microprocessor	SERV-32I





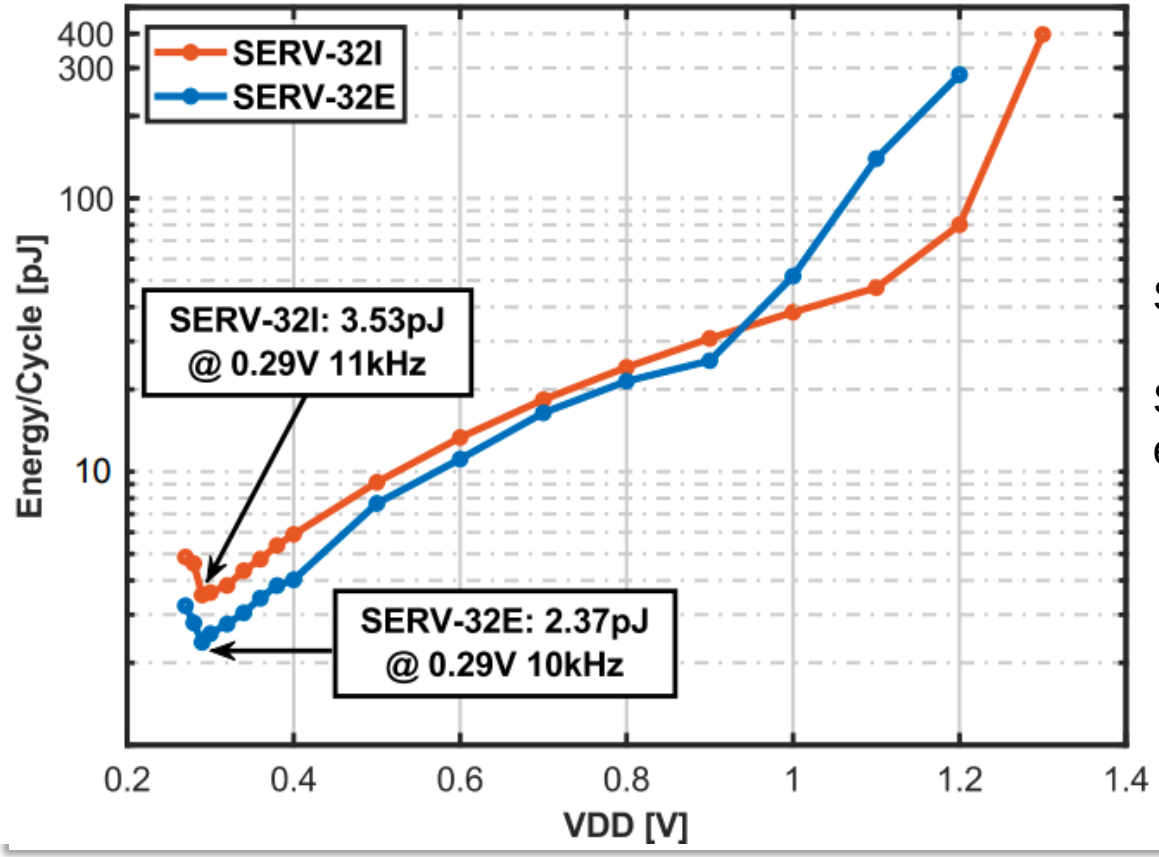
Measurement and Results



Area distribution of SoCs.

- 16 registers = 28% core footprint
- SERV-32E is approximately 17% smaller than SERV-32I

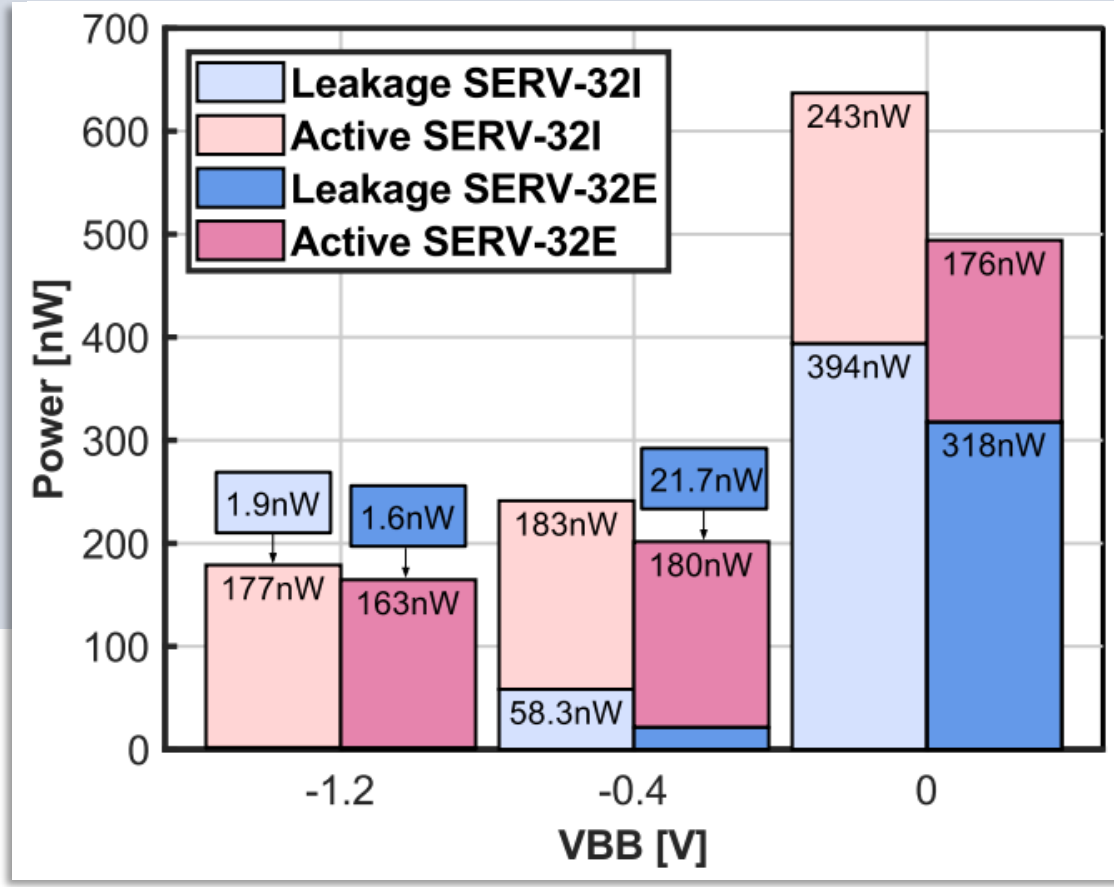
Measurement and Results



SERV SoCs power breakdown:

SERV-32I is 1.5 times more energy than SERV-32E

Measurement and Results



SERV Active Energy per cycle at different VDD

200 times reduced in leakage power

Measurement and Results

Table I. ASIC Implementation in comparison.

	Tech.	VDD [V]	Power [µW/MHz]	Leakage [µW]	NAND Gate	Freq. [MHz]
[4]	SOTB 65nm	0.22	13.3	0.049	50.1k	14
[5]	FDX 22nm	0.42	4.47	105.4	-	18
[6]	FDX 22nm	0.55	6.3	6.6	-	40
[7]	FDSOI 28nm	0.4	3.3	8.4	-	40
[8]	FDSOI 65nm	0.5	13.4	-	-	0.00207
SERV-32I	SOTB 65nm	0.29	3.53	0.007	84k	0.011
SERV-32I SoC	SOTB 65nm	0.29	6.97	0.03	-	0.011
SERV-32E	SOTB 65nm	0.29	2.37	0.0024	70k	0.01
SERV-32E SoC	SOTB 65nm	0.29	3.11	0.0037	-	0.01

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Conclusions

This paper presents two SERV serial architecture SoCs based on the RISC-V specification, SERV-32I, and SERV-32E. We have shown how architectural heterogeneity affects area overhead and power consumption. In terms of area, cutting 16 registers in the RF reduces the footprint by 28% of the processor. In terms of power consumption, the power consumption of the SERV-32I is about 1.5 times higher than that of the SERV-32E in the reverse-body bias region.

Thank You For Your Listening

Acknowledgement

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Acknowledgement

1.M. Sarmiento et al., “A Sub-µW Reversed Body-Bias 8-bit Processor on 65-nm Silicon-on-Thin-Box (SOTB) for IoT Applications,” IEEE TCAS-II, vol. 68, no. 9, pp. 3182–3186, Jun. 2021.
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