

Real-time Auto-exposure Histogram Equalization Video-system Using Frequent Items Counter

Ngoc-Tu Bui¹, Trong-Thuc Hoang², and Cong-Kha Pham³

^{1,2,3}University of Electro-Communications (UEC), 1-5-1 Chofugaoka, Chofu-shi, Tokyo 182-8585, Japan Email: ¹buingoctu@vlsilab.ee.uec.ac.jp; ²thuc@vlsilab.ee.uec.ac.jp; ³phamck@uec.ac.jp

ABSTRACT

In this paper, one of the Frequent Items Counter (FIC) applications, the real-time video Histogram Generator (HG), was developed. The video histogram was extracted in each frame by the HG module. Then, the full system of auto-exposure Histogram Equalization (HE) video-system was built which can operate in the real-time setting.

I. SYSTEM OVERVIEW

The system was based on our previous works of FIC [1-3]. The first architecture of FIC was given in 2017 [1]. Then, the improved architecture was published in July 2018 [2]. Lastly, in the same year of 2018, the journal paper [3], which is the extent writing of the conference paper [2], was published for providing more details and comparison results.

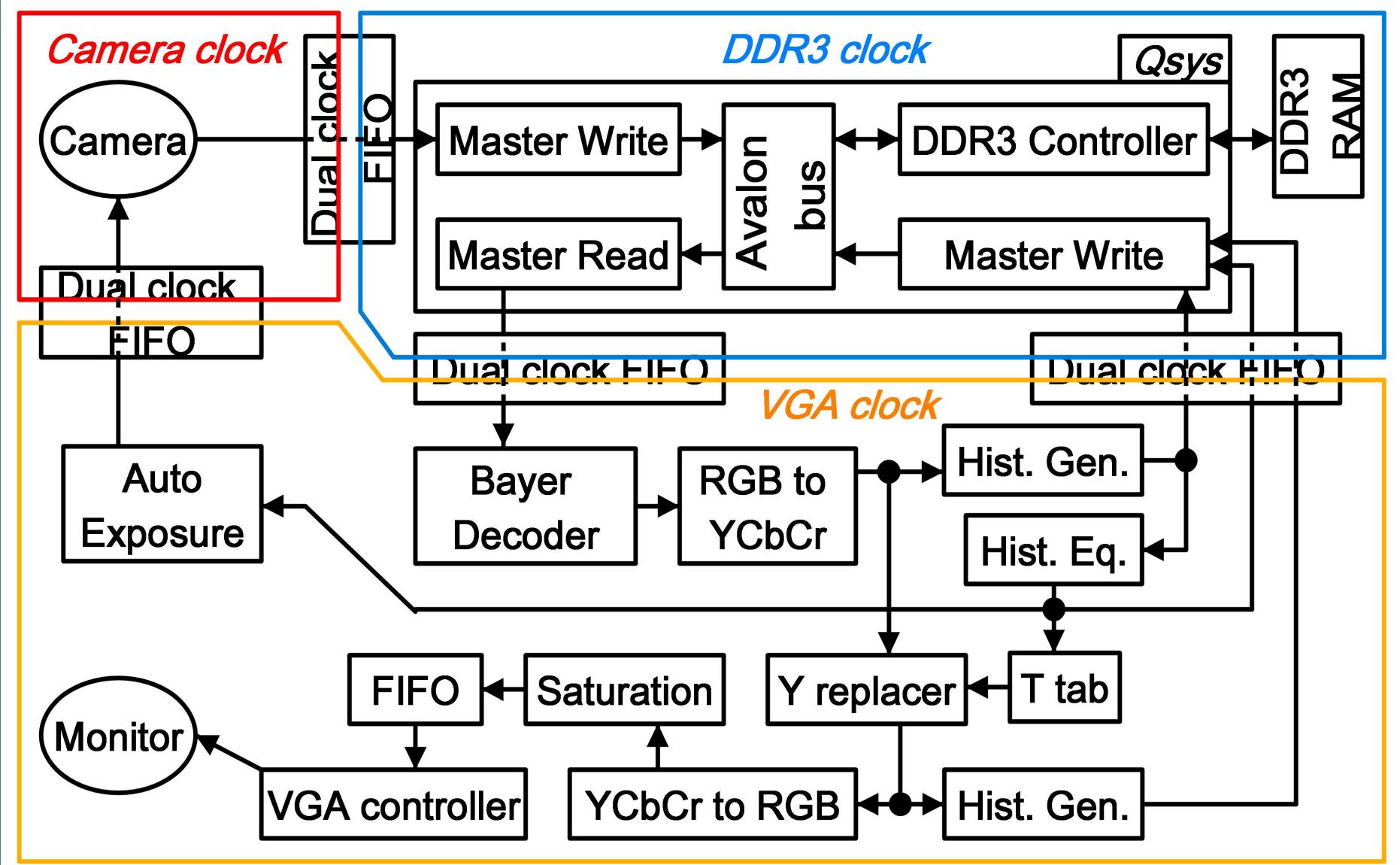


Fig. 1: The system block diagram.

Fig. 1 gives the block diagram of the proposed videosystem of Histogram Equalization (HE) with the autoexposure feature.

- *DDR3-RAM*: stores the display content.
- **Bayer-decoder:** decodes raw picture from the camera to RGB.
- *Two Histogram Generators (HG):* produce two histograms of the before and after the HE process. They operate on the luminance of the Y-value only.
- *Histogram Equalization (HE):* produces the Transformation Function (HE-TF) based on the smooth HE algorithm in [4].
- **Y-replacer:** replaces the Y-value according to the HE-TF stored in the T-table.
- Saturation: boots up the RGB-color a little bit before streaming out the video to display on the monitor.
- Auto-exposure: adjusts the camera exposure value based on the received HE-TF to fit the current luminance condition.

II. DEMONSTRATION SETUP

Fig. 2 gives the system is setup with an FPGA board and a monitor. The system used the VEEK-MT-SoCKit with the FPGA chip of Altera Cyclone V SoC and a 5-Megapixel (5-MP) Charge Coupled Device (CCD).

The figure shows the videos before and after the HE process, the histograms before and after the HE process, and the HE-TF in between the two histograms.

- The video resolution is 1280x800.
- The monitor display rate is at 60Hz.
- The CCD capture rate is at 24.28Hz to 38.98Hz depend on the exposure value.
- The histogram, the HE-TF, and the camera exposure value are changed in each frame to satisfy the real-time requirement.

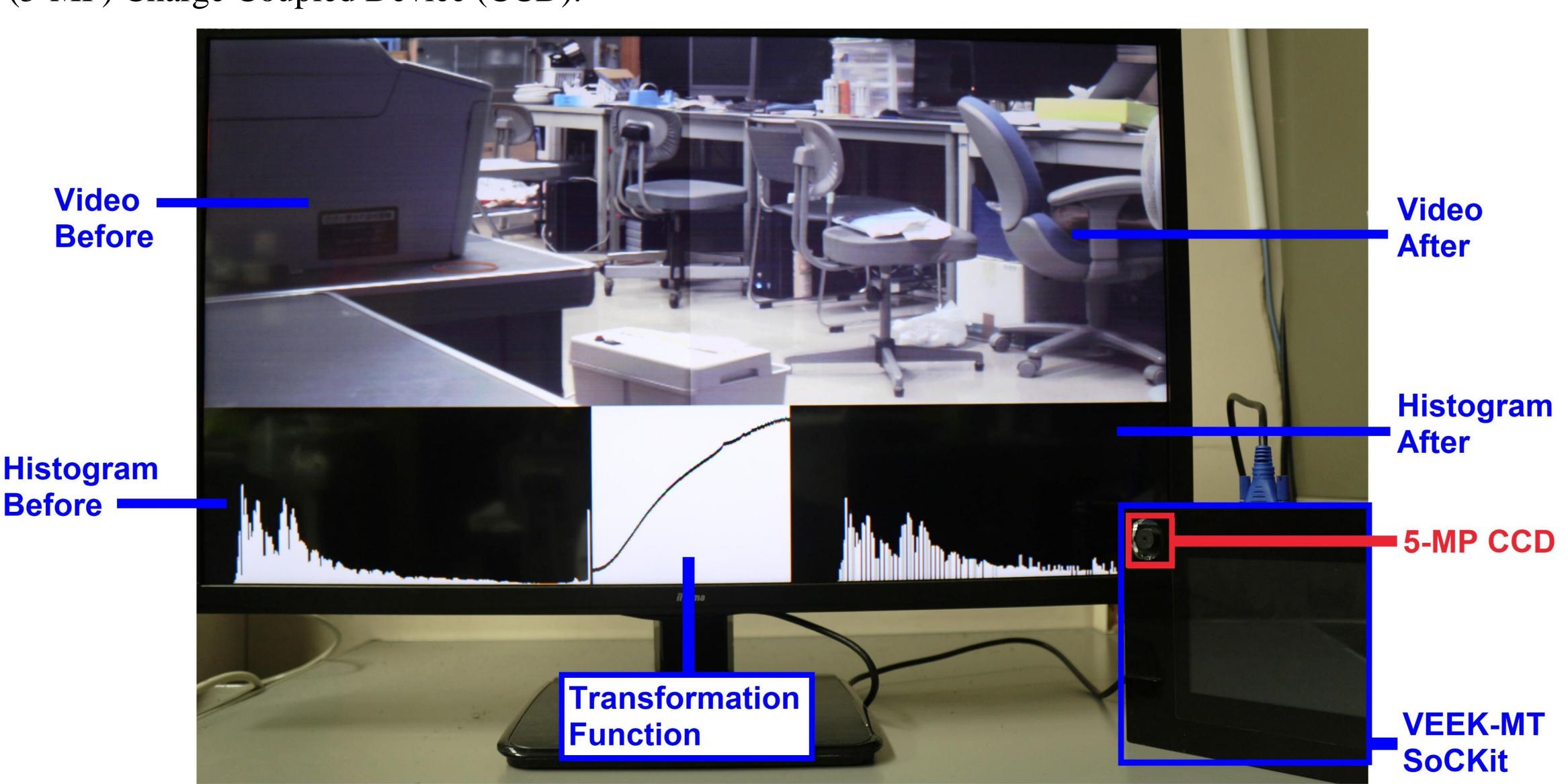


Fig. 2: The system setup.

REFERENCES

- [1] Trong-Thuc Hoang et al., "FPGA-based Frequent Items Counting Using Matrix of Equality Comparators," in *Proc. of MWSCAS*, Aug. 2017.
- [2] Katsumi Inoue et al., "VLSI Design of Frequent Items Counting Using Binary Decoders Applied to 8-bit per Item Case-study," in Proc. of PRIME, Jul. 2018.
- [3] Katsumi Inoue et al., "Frequent items counter based on binary decoders," in ELEX, 2018.
- [4] T. Arici et al., "A Histogram Modification Framework and Its Application for Image Contrast Enhancement," in IEEE Trans. on Image Processing, 2009.