Ryerson University

Department of Electrical & Computer Engineering
Faculty of Engineering & Architectural Science

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Instructor:	**Professor M. Shazzat Hossain**

Assignment/Lab Number:	
Assignment/Lab Title:	***Design Project***

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1. Introduction:

The purpose of this project is to design, simulate, analyze, implement, and test a single-supply, multistage, transistor amplifier which fulfills a set of specifications.

2. Objective(s):

The design project contains a set of specifications:

- Power supply: +15V relative to the ground;
- Total quiescent current drawn from the power supply: no larger than 8 mA;
- No-load voltage gain (at 1 kHz): |A vo | = 50 (± 10%);
- Maximum no-load output voltage swing (at 1 kHz): no smaller than 8 V peak to peak;
- Loaded voltage gain (at 1 kHz and with R L = 1 kΩ): no smaller than 90% of the no-load
- voltage gain;
- Maximum loaded output voltage swing (at 1 kHz and R L = 1 kΩ): no smaller than 4 V peak to peak;
- Input resistance (at 1 kHz): no smaller than 50 kΩ;
- Amplifier type: inverting or non-inverting;
- Frequency response: 20 Hz to 50 kHz (−3dB response);
- Type of transistors: BJT;
- Number of transistors (stages): no more than 3;
- Resistances permitted: values smaller than 220 kΩ from the E24 series;
- Capacitors permitted: 0. 1 μF, 1. 0 μF, 2. 2 μF, 4. 7 μF, 10 μF, 47 μF, 100 μF, 220 μF;
- Other components (BJTs, diodes, Zener diodes, etc.): only from your ELE404 lab kit.

Other specifications:

- The output voltage must be free from distortions (clipping, etc.) in all test conditions. The source resistance, R s , must be 600 Ω for all tests.
- The designed amplifier must be AC-coupled for the load and the signal source, but the coupling between its intermediate stages may be of AC or DC type as per the designer's choice.
- There are no restrictions in terms of using NPN or PNP transistors.

3. Description of the circuit:

The circuit was designed with 3 stages each containing a 2N3904 NPN transistor which all 3 stages are designed to be in active mode. The purpose of the first stage is to set the input resistance (>50 kohm) and to provide a large gain. A 6v voltage source is connected from the collector of the first stage and the base of the 2nd stage in order to compensate for the very large voltage output from the first stage of the collector (creates a voltage drop). The purpose of the second stage is to provide a small gain, such than when cascaded with the first stage its able to reach to the specified voltage gain. CE amplifiers are able to create a relatively large gain therefore the first stage and the second stage contains the Common Emitter configuration.

A voltage divider is created at the base of the first stage transistor(Q1) in order to control the transistor's base voltage, VB at a constant voltage proportional to the supply voltage, VCC. A bypass capacitor is also connected parallel to the emitter resistance for the first two stages in order for the voltage gain of the CE amplifier to increase. Coupling capacitors are also involved in series with the Load resistor and the Rs resistor in order for DC signals to be blocked and to have AC signals to enter. Emitter degeneration was added to first and the second stage in order to control their gain.

The third stage was made in a Common- Collector configuration to provide a large load to the second stage, while simultaneously having a very small output resistance. The third stage was also designed to create a buffer where the voltage gain is approximately equal to one and to maintain the voltage gain from the two CE stages. The design of the circuit was also based on the quiescent point (Q point), which is the point on the output characteristics and its by setting its Collector current (I_C) to a constant and steady state value without an input signal applied to the transistor's Base. The calculations were done based on these various assumptions and are

shown in the appendix. **Figure 1** displays an overview of the the design schematic. The three stages of the amplifier and their respective parameters are explained in greater detail below:

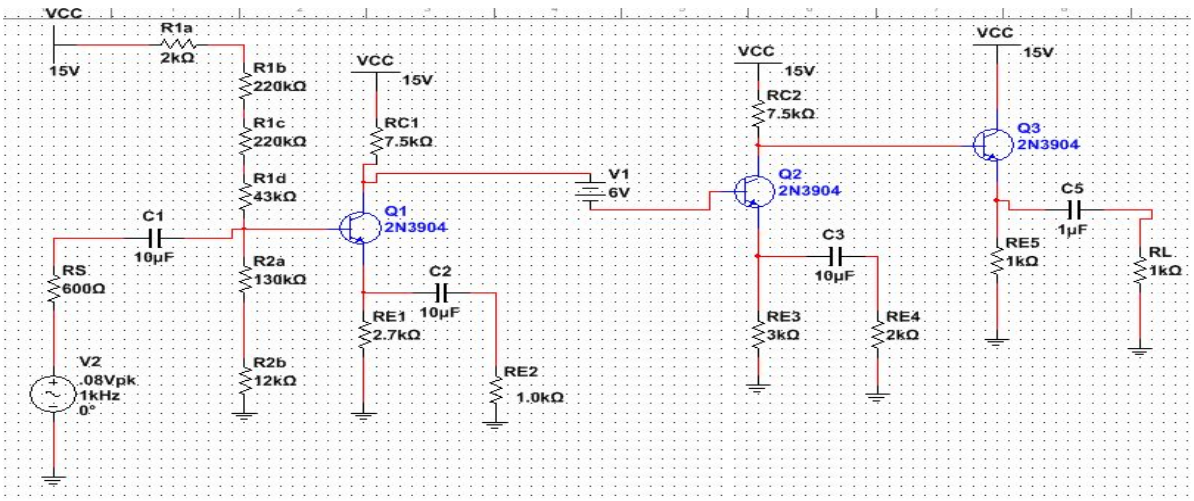


Figure 1: Q1 and Q2 are within a CE amplifier configuration. Q3 is within a CC amplifier configuration.

4. Circuit under test:

Stage 1: Stage 1 contains Common Emitter configuration. It was designed to have a gain of 10[V/V] and a current draw of 25.2 uA through R1 and 780uA through RC1. The input resistance of the whole amplifier circuit is equivalent to the parallel of the input resistance of Q1, R1, and R2. gm1 is assumed to approximately be 30 in order to get a high input resistance of 50 kohm. In order to get Q1 to be in Active mode and for the Q- point to be stable, I assumed that VE1 is approximately 2.0V. When manual calculations are made based on these assumptions, the R1 and R2 are over 220k ohm. In order to compensate this discrepancy within the specifications, series of resistors are used for R1 and R2 in order to meet the specifications and the E24 series. In order to meet the requirements of 8V peak to peak voltage swing an upper bound approximation has been made where VC1= 9V. This assumption allowed Rc1= 7.5

k ohm, RE1= 2.7kohm and RE2= 1.0k ohm. Coupling capacitor C1 was used before the RS in order to cancel out any DC signals within the circuit. A bypass capacitor C2 was used in parallel with the emitter resistor in order to let the signal from the emitter to be passed onto the ground of the circuit. **Figure 2** shows the current drawn from the VCC and the respected voltage gain. After design, its parameters are:

- Stage Gain (without load): | AVO1 |= 9.745 [V/V]
- Stage gain (with load): |AV1| = 9.52 [V/V]
- Input resistance: Rin(Q1)= 120.6 kohm
- Input resistance of the whole amplifier: Rin= 57.4 kohm (specification has been met)
- Output resistance: RO= 7.5 kohm
- R1= R1a +R1b +R1c + R1d
- R2= R2a +R2b

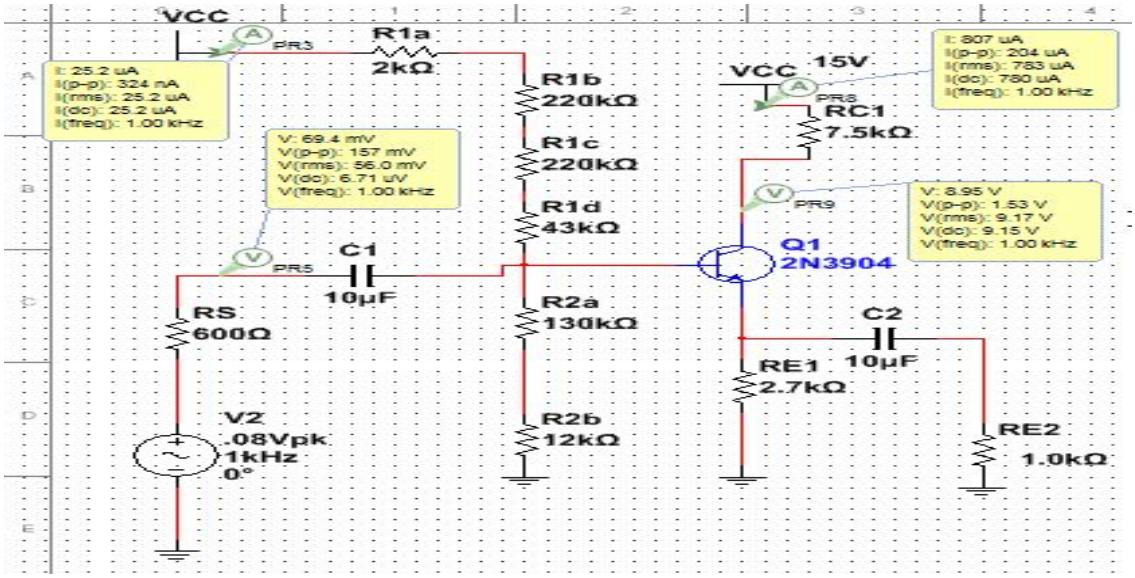


Figure 2: Stage 1- CE amplifier is designed to have a 1.53 V(Pk-Pk) at the collector of Q1. The signal source is .08 Vpk in order to avoid clipping in the waveforms.

Stage 2: Stage 2 contains Common Emitter configuration. It was designed to have a gain of 10[V/V] and a current draw of 860uA through RC1. gm2 is also assumed to approximately be 30 in order to get a high input resistance for Q2 BJT of 50 kohm and to be consistent with the first stage CE amplifier. A 6V voltage source is implemented in order to create a voltage drop from Stage 1's collector and VB at the base of Q2. Another reason for this implementation of the 6V source is that the main objective is to create a specified gain that will allow |AVO| to be approximately be 50 when cascaded. RC2 is also assumed to be 7.kohm in order to be consistent with Stage 1 of the CE amplifier and to approximately have the same amount of current drawn from the VCC. |AVO2| is approximately 5 V in order to satisfy the specification when cascaded. Based on these assumptions made and manual calculations RE3=3.0 kohm and RE4= 2kohm. A bypass capacitor C3 is implemented within the second stage in order to stay consistent with the CE amplifier of the first stage. **Figure 3** shows the current drawn from the VCC and the respected voltage gain. After design, its parameters are:

- Stage Gain (without load): | AVO 2|= 5.5 [V/V]
- Stage gain (with load): |AV2| = 5.45 [V/V]
- Input resistance: Rin(Q2)= 226.366 kohm
- Output resistance: RO= 7.5 kohm

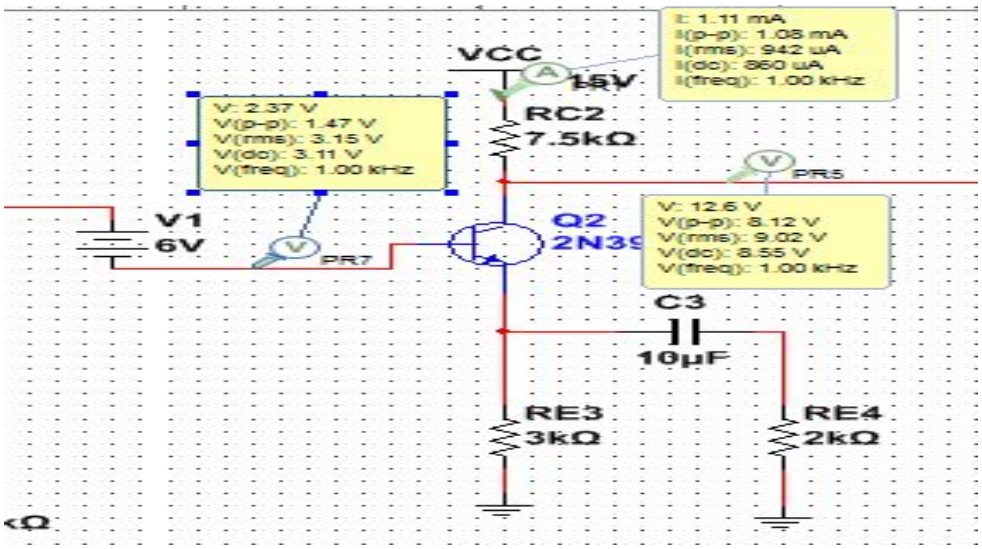


Figure 3: Stage 2-CE amplifier is designed to have a 8.12 V(Pk to Pk) at the collector of Q2.

Stage 3: Stage 3 contains Common Collector configuration. It was designed to have a gain of approximately 1[V/V] and a current draw of 7.80 mA where the majority of the quiescent current is created. Based on the CC- Amplifier configuration, the emitter resistance is supposed to be less than or equal to the load resistance of 1k ohm in order to have an approximate gain of one for stage 3. Based on this consideration, RE5= 1kohm in order to have an approximate 1V gain. A coupling capacitor C5 is implemented within the second stage in order to cancel out any AC noise or DC signals. This helps avoid any clipping of the waveform for the final stage. **Figure 4** shows the current drawn from the VCC and the respected voltage gain. After design, its parameters are:

- Stage Gain (without load): | AVO 3|= 0.96 [V/V]
- Stage gain (with load): |AV| = 0.86 [V/V]
- Input resistance: Rin(Q3)= 108.1 kohm
- Output resistance: RO= re= 0.215 kohm

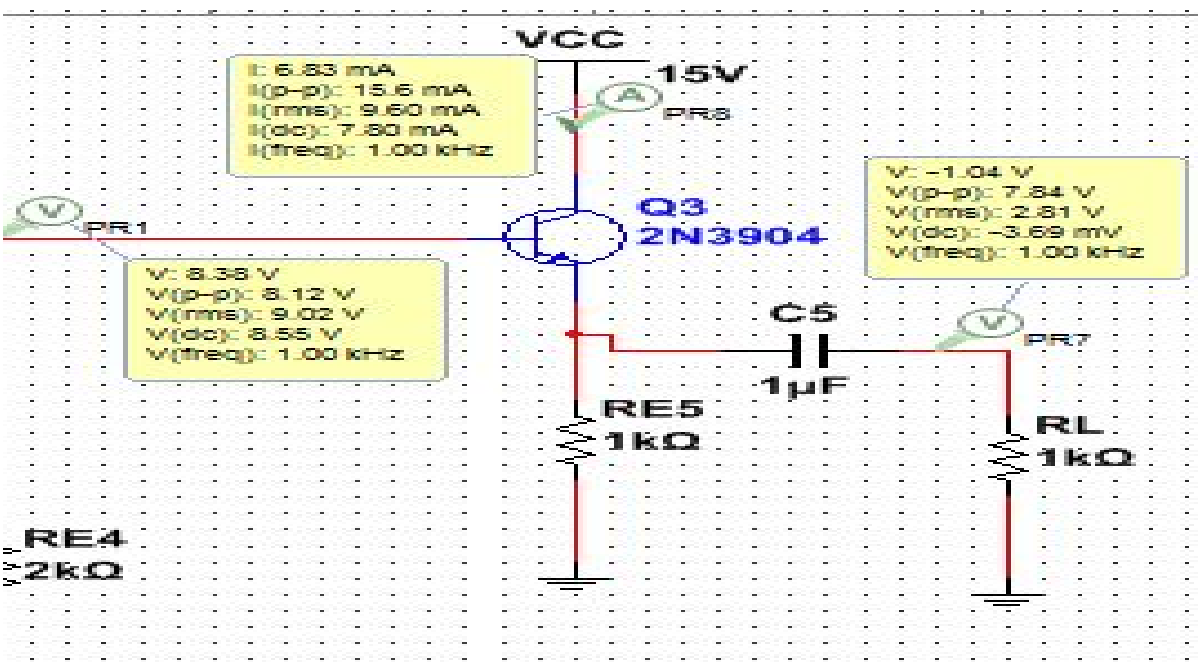
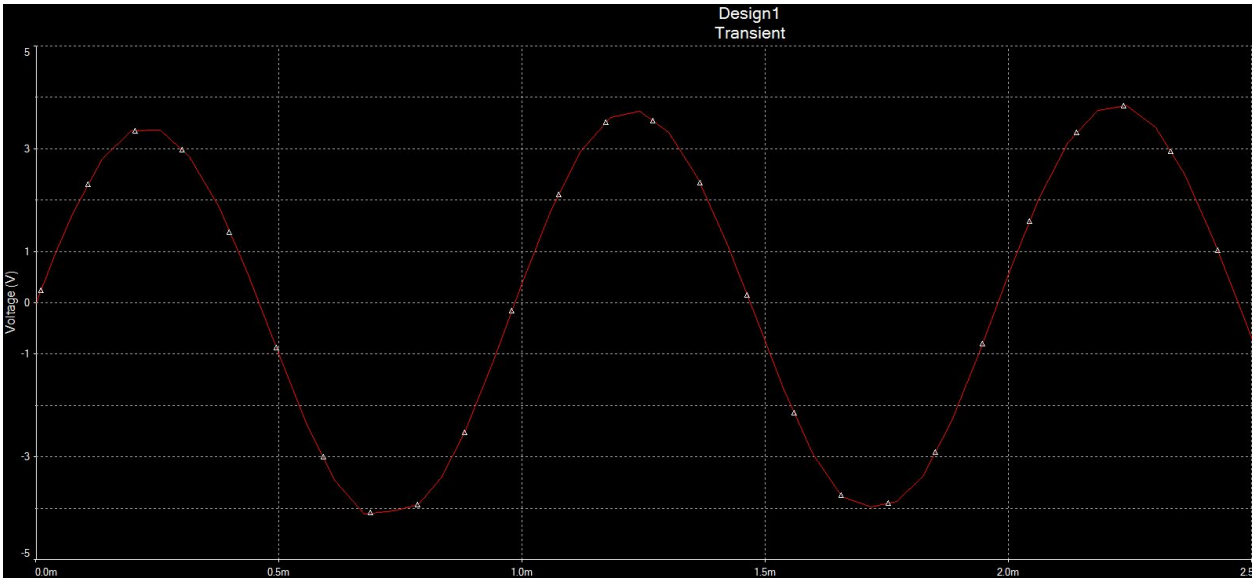


Figure 4: Stage 3- CC amplifier is designed to have 7.84 V(Pk-Pk) at the emitter of Q3.

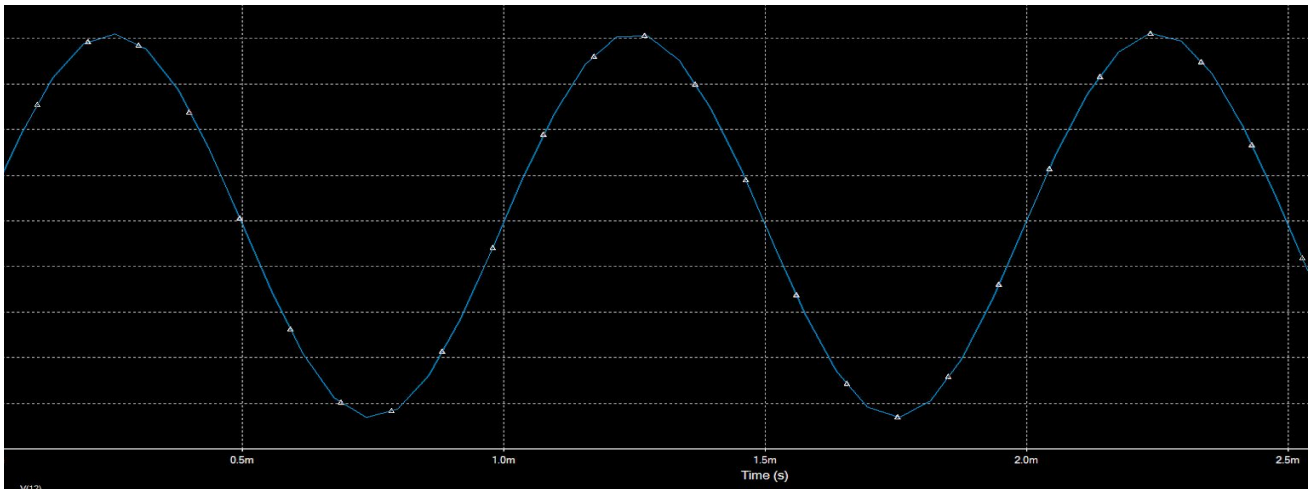
Overall circuit design

- No loaded total gain voltage: |AVO|= |AVO1| *|AVO2| * |AVO3| = 51.4 V (therefore specification has been met)
- Loaded total gain voltage: |AV|= |AV1| *|AV2| * |AV3| = 47.7 V (therefore specification has been met)
- Loaded voltage gain is no smaller than 90% of the unloaded voltage gain (AV>0.9 AVO) (specification has been met)
- Total Quiescent Current: 7.95 mA (specification has been met)
- **Graph 1** demonstrates that the the maximum loaded output voltage swing is approximately 7.2 V (Pk- Pk) and contains no clipping therefore the specification has been met.

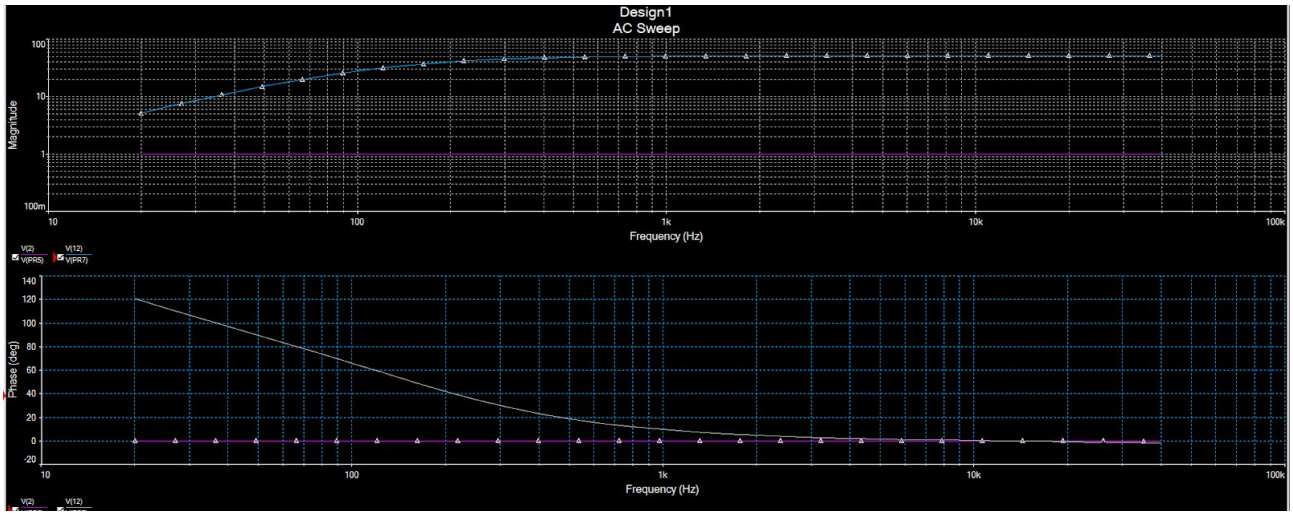
- **Graph 2** demonstrates the maximum no-load output voltage is approximately 8.2 V(Pk -Pk) and contains no clipping therefore the specification has been met.
- **Graph 3** shows the Frequency response of the amplifier circuit and its within the (-3dB) response therefore the specification has been met.
- **Figure 5** shows the circuit with no load and proves that all specifications are met.
- **Figure 6** shows the circuit with load and proves that all specifications are met



Graph 1: Waveform of the Loaded output voltage with 7.2 V(Pk-Pk)



Graph 2: Waveform of the no-load output voltage with 8.2 V(Pk-Pk)



Graph 3: Frequency response of the amplifier circuit (20 Hz to 50 kHZ)

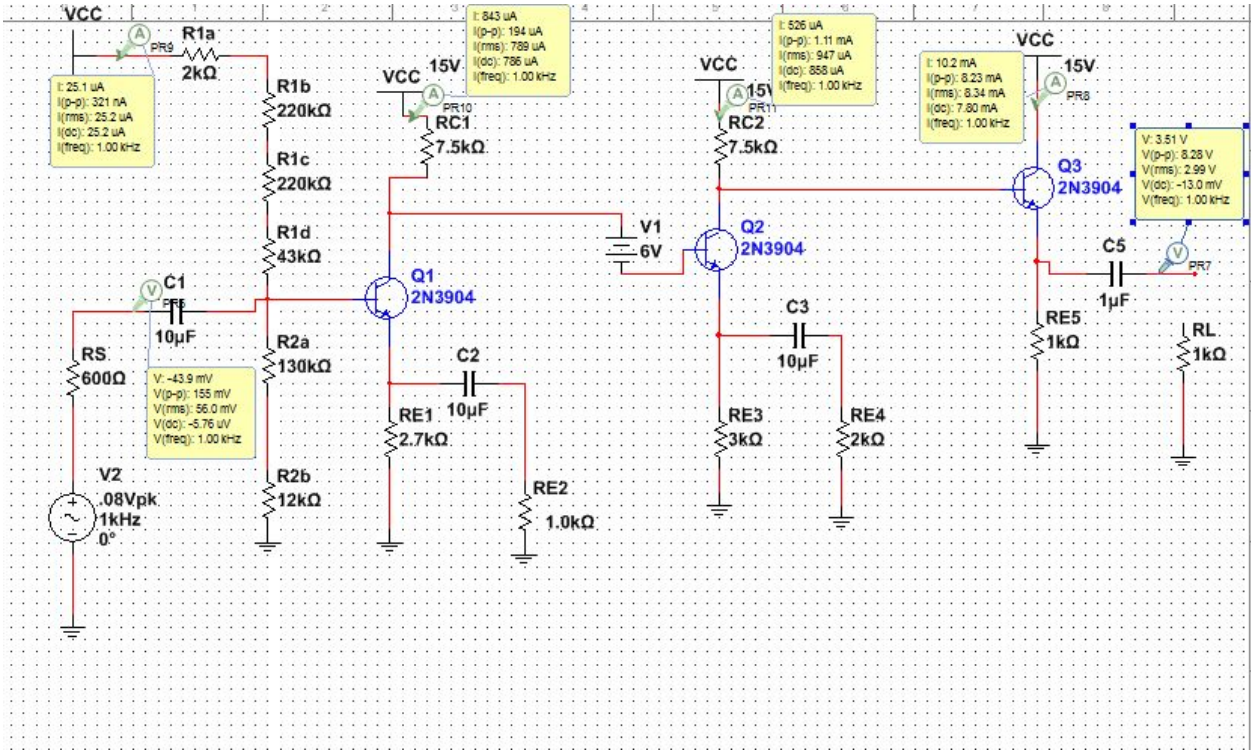


Figure 5: Amplifier circuit of no load with fulfilled specifications

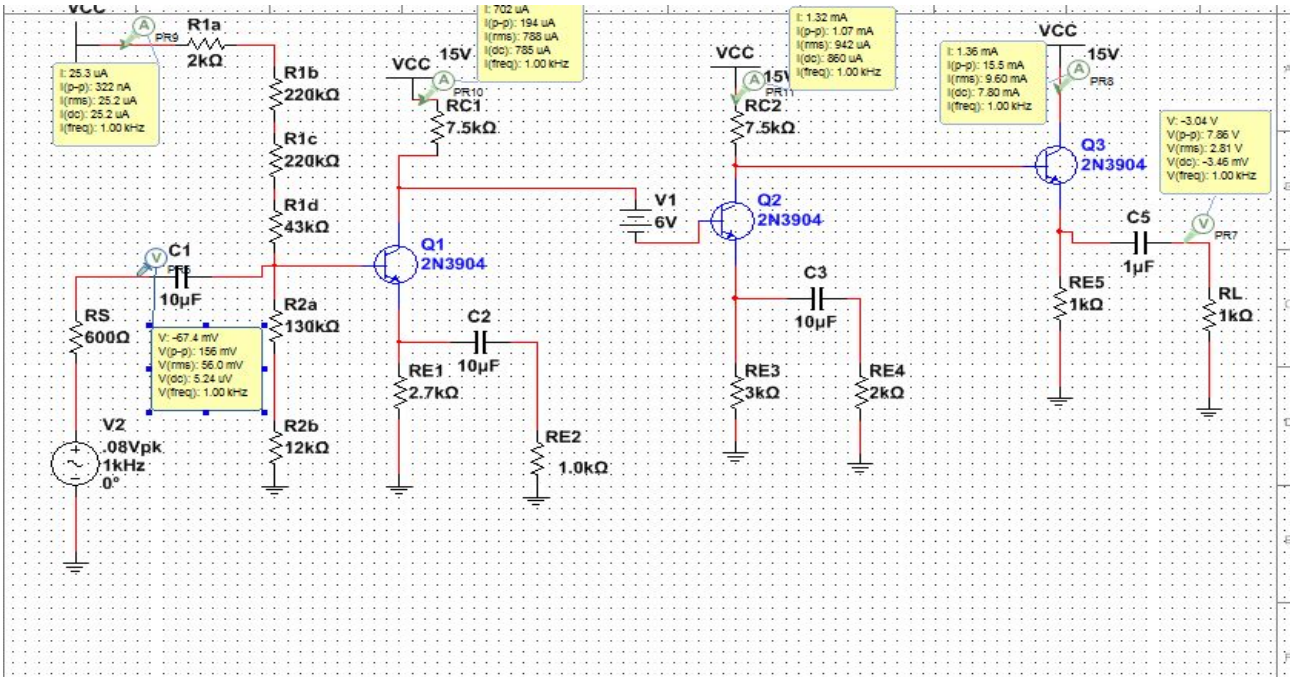


Figure 6: Amplifier Circuit with load and fulfilled specifications.

5. Conclusion:

Overall, the 3 stage Amplifier (CE CE CC) circuit has fulfilled all the requirements within the objective of this design. The first two CE stages are used to create a specified voltage gain when cascaded. CC amplifier is used as the third stage to help maintain that voltage gain within the specific requirements and to provide a large load resistance to the second stage. Bypass and coupling capacitors were implemented in order to avoid clipping within the circuit and to help control the signals of the circuit. C1, C2, and C3, and C5 were determined based on the clipping of the waveforms and many capacitors were tested to fulfill the requirements. Minor discrepancies may occur between the manual calculations and the simulation of the circuit in order to fulfill the requirements of the E24 series of the resistors.

6. APPENDIX