PRAC1 - Report

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CSSE4010

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UQ

Aim:

The aim of the following project is to design and to create a testbed within Vivado that exhaustively tests the operation of a basic and2or gate.

Design Block Diagram (Gate Level):

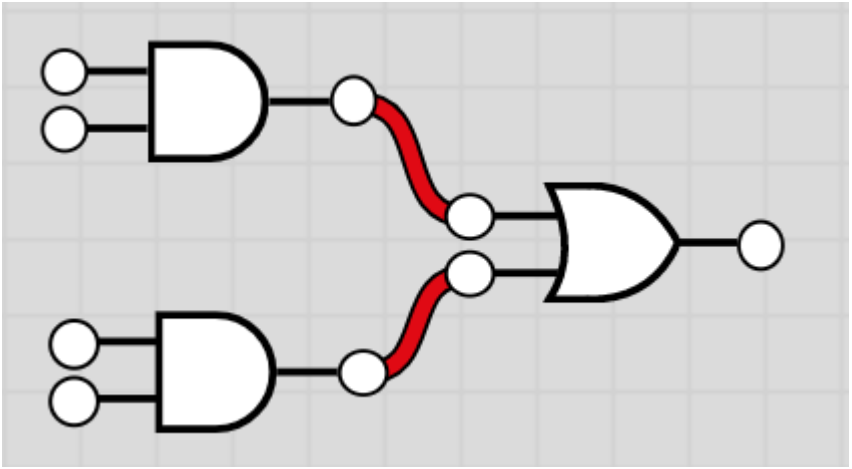

Figure 1 and2or gate design implementation

The above design is to be used when setting up the and2or gate in the FPGA. The outputs of the and gates are fed to the inputs of the or gate.

Synthesized Design:

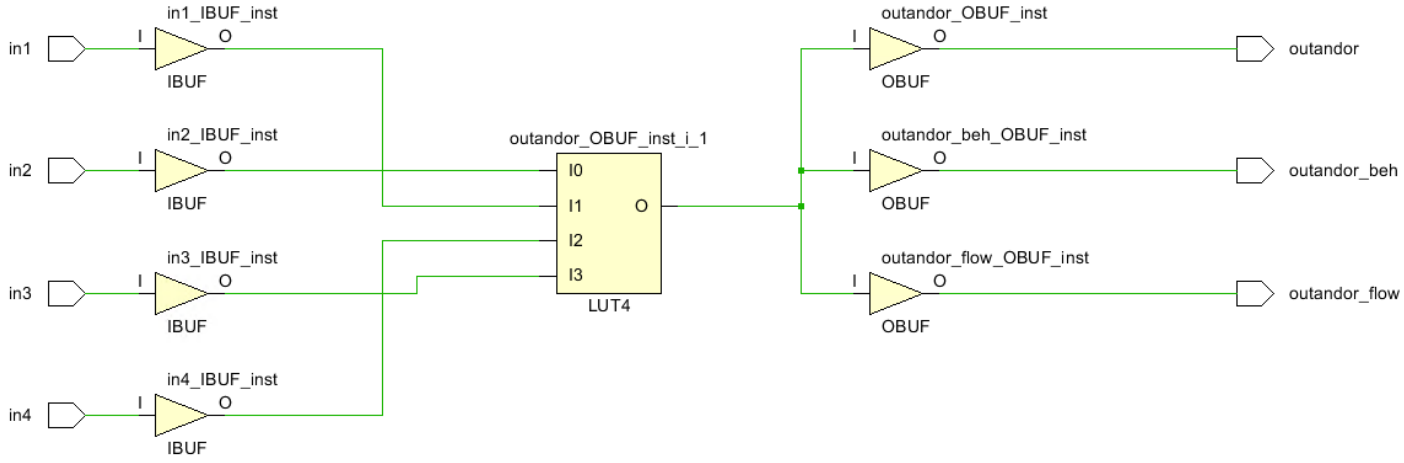

Figure 2 Synthesized Design, FPGA Setup

Figure 2 shows the synthesized design for the and2or gate implementation. All 4 inputs are buffered and then processed through look up table, and each of the outputs are also buffered.

For testing purposes, there are 3 outputs from the or gate, representing the structural, behavioral and signal flow. However, as seen in the design, they are all connected to the one output node of the LUT ('O'), since the output definitions are logically the same. Thus, we expect all three outputs to always be the same.

Test Bed Spec:

I. The inputs to the and gates are setup as an input bus, the outputs from the or gates are setup in the same way.

```
signal inputs : std_logic_vector(3 downto 0) := "0000";
signal outputs : std_logic_vector(2 downto 0) := "000";
```

II. Unit Under Test Signal Mapping

```
uut: and2or PORT MAP (
in1 => inputs(0),
in2 => inputs(1),
in3 => inputs(2),
in4 => inputs(3),
outandor => outputs(0),
outandor_flow => outputs(1),
outandor_beh => outputs(2));
```

III. Input Incrementation and Error Checking

```
input_gen: process
BEGIN

    inputs <= "0000";
    FOR I IN 1 TO 16 LOOP

        WAIT FOR 10ps;
        --ERROR CHECKING
        if (inputs = "1100") then
           assert (outputs(0) = '0') report "bad gate" severity error;
           assert (outputs(1) = '0') report "bad gate" severity error;
           assert (outputs(2) = '0') report "bad gate" severity error;

        elsif (inputs = "0011") then
           assert (outputs(0) = '0') report "bad gate" severity error;
           assert (outputs(1) = '0') report "bad gate" severity error;
           assert (outputs(2) = '0') report "bad gate" severity error;

        elsif (inputs = "1111") then
           assert (outputs(0) = '0') report "bad gate" severity error;
           assert (outputs(1) = '0') report "bad gate" severity error;
           assert (outputs(2) = '0') report "bad gate" severity error;
        end if;
        --ERROR CHECKING

        inputs <= inputs + '1';

        END LOOP;
        WAIT;
END PROCESS;
```

Simulation Results:

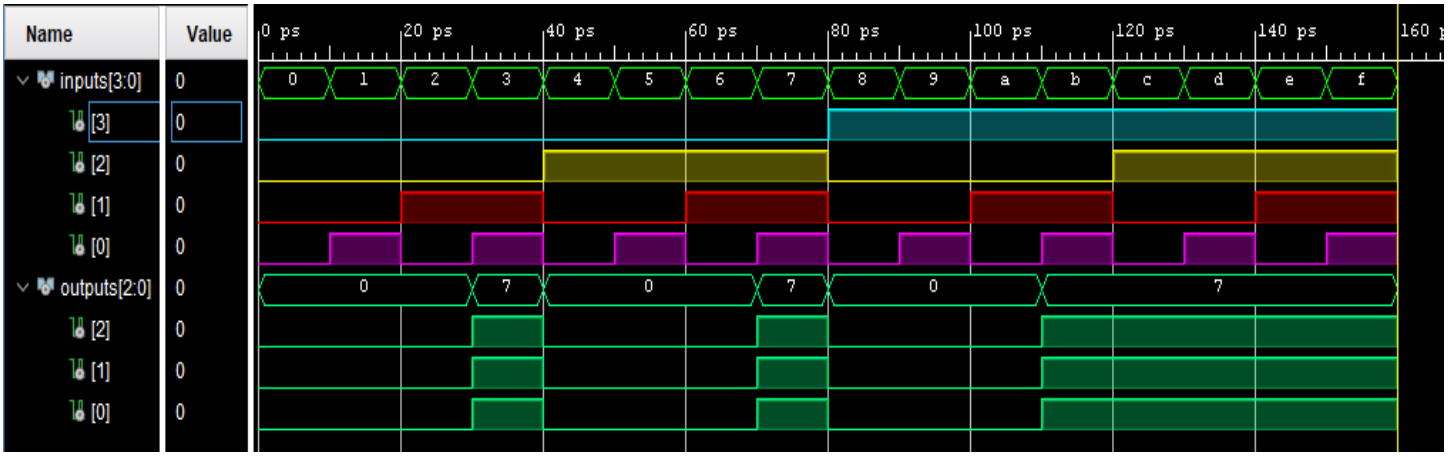

Figure 3 Simulation Results for And2Or gate. *AND GATE 1: inputs 0,1 AND GATE 2: inputs: 2, 3*

Figure 3 shows the simulation results for the and2or gate, the inputs are marked in different colors according to their bus position (seen on the left). Compiling the test bed did not trigger any of the error checking statements previously declared.

Looking at the output bus, it is seen that all outputs (0-2) are HIGH when at least both inputs to a single AND gate are also HIGH, this is the expected behavior of the circuit seen in *Figure 1*. Therefore, simulation results appear to be correct.

Resource Consumption:

Name	Slice LUTs (63400)	Bonded IOB (210)
and2or	1	7

Figure 4 Synthesized Design Utilization

The board will be utilizing:

- 1 Look up table
- 7 Bonded IOB

The utilization can be seen in *Figure 2*.

Figure 5 shows the **on-chip component utilization.**

Name	Slice LUTs (63400)	Slice (15850)	LUT as Logic (63400)	Bonded IPADs (2)
and2or	1	1	1	7

Figure 5 Implementation Utilization

Power Usage

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.094 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**30.0°C**
Thermal Margin:	70.0°C (15.1 W)
Effective ϑJA:	4.6°C/W
Power supplied to off-chip devices:	0 W

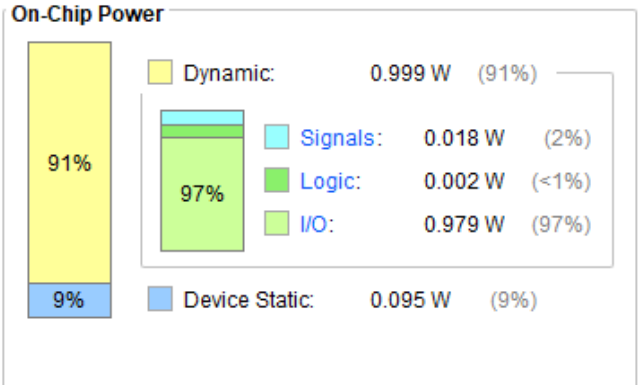

Figure 6 FPGA Power Usage

Seen above are the expected power usage on the device based on the following input voltages (Default Profile – 25C Ambient Temp)

Figure 7 Input Voltage

Internal Connections:

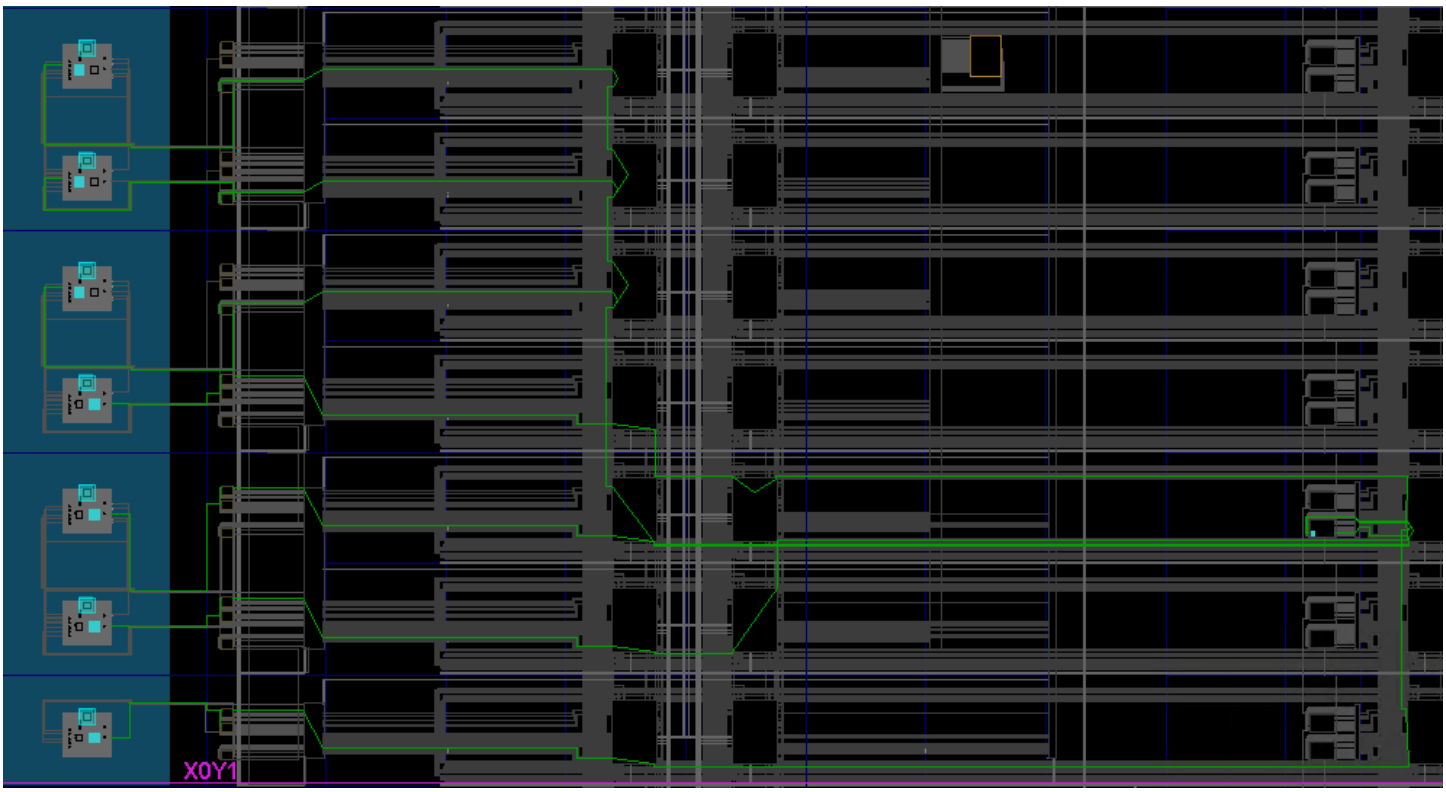

Figure 8 ALU Far Right, Inputs and Output Bus Left

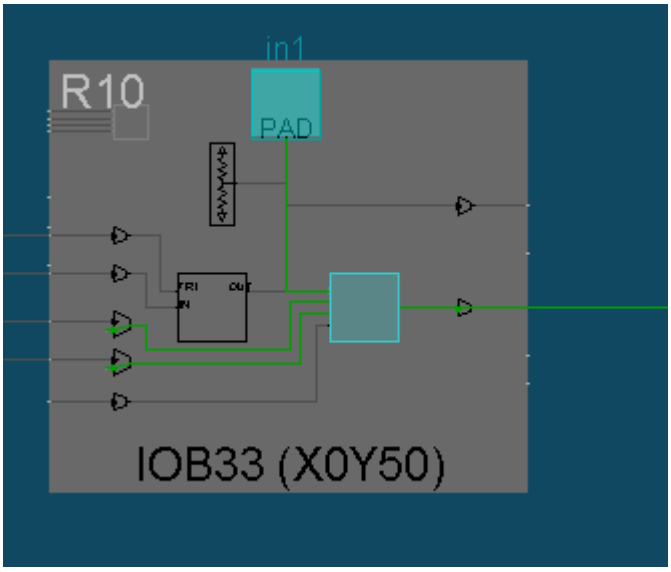

Figure 9 Example: Input 1 connections setup

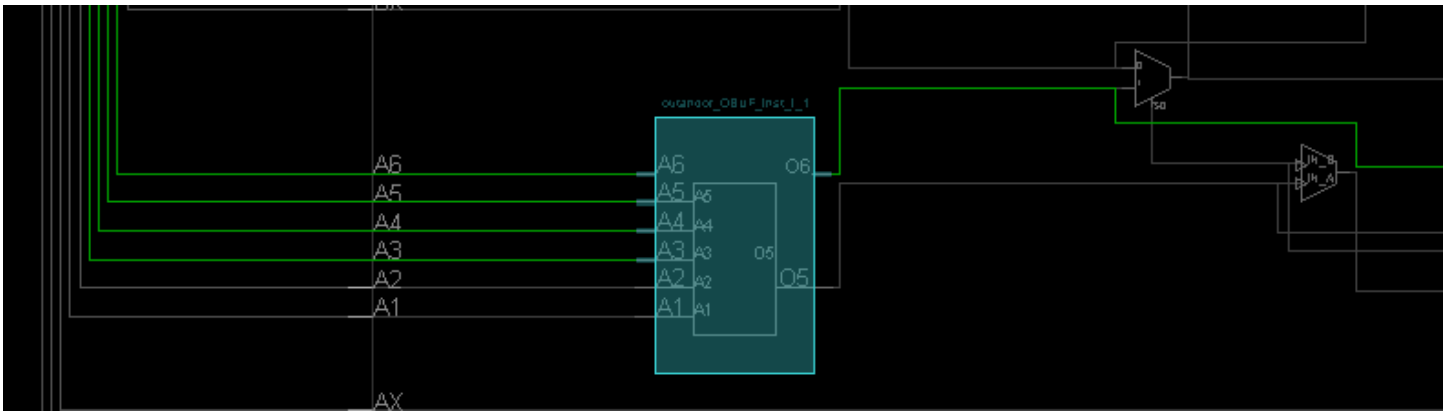

Figure 10 Look Up Table in Use Within Device