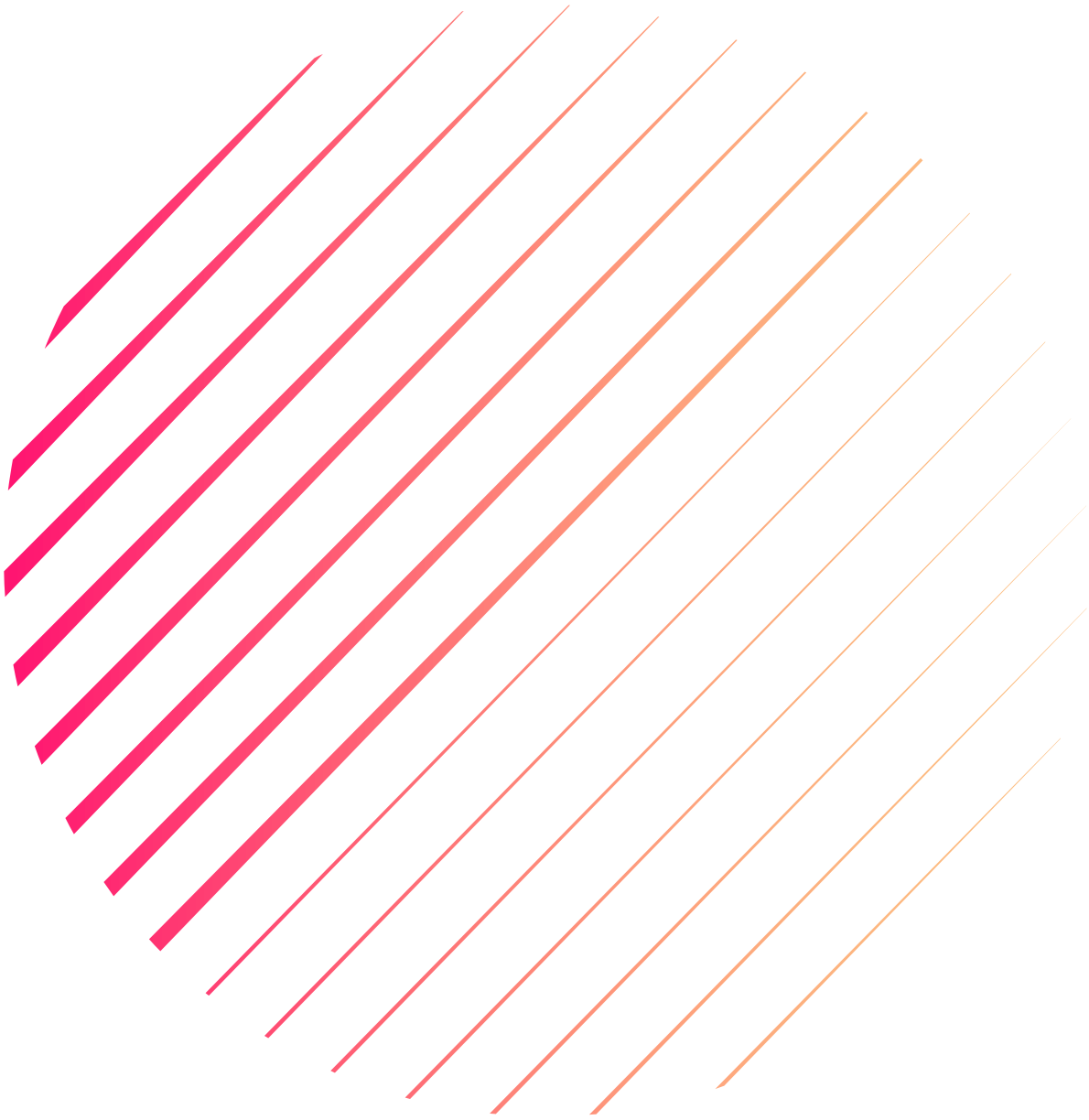
Registers & Combinational Logic



Prac 2 Report:
CSSE 4010

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1. Introduction.

1.1 Design Brief and Aims

The aim of this task is to design and exhaustively test the a 4-digit combination lock. It is required that 2 designs are implemented, a circuit that operates on a synchronous clock and another that operated with an asynchronous clock. To verify the accuracy of the design, a simulation test bed is to be created and the 2 designs are tested for the correct outputs.

2. Design Description.

2.1 Design Assumptions

- The orientation in which the student number is entered, is assumed to be such that the last two digits are entered first (in reverse order).
  - i.e. "0422" is entered as 22 PushButton1, 40 PushButton2.

- The 7 Segment Display requires a LOW signal to display values (general orientation).

- The testbed algorithm is such that input digits are entered prior to push buttons are pressed, otherwise the default signal float values are set to LOW.

2.2 Synchronous Design

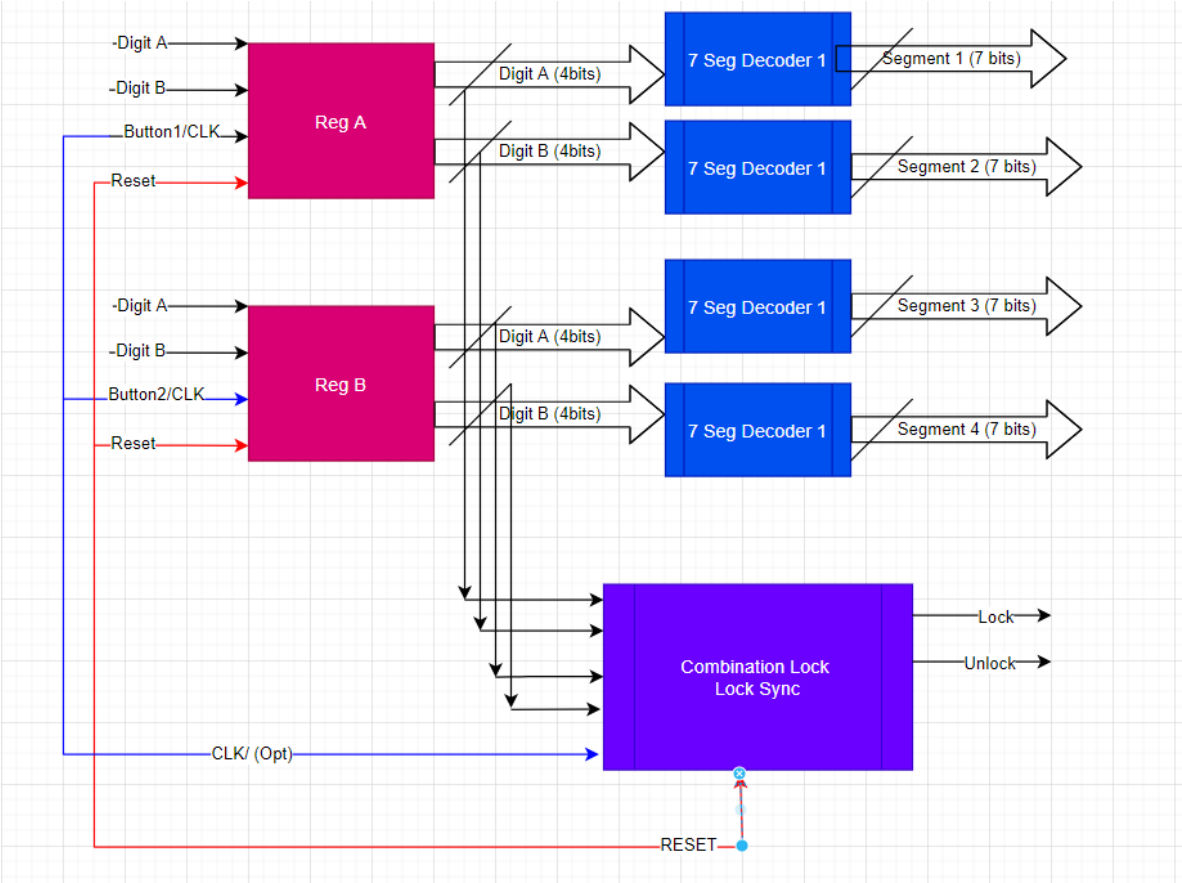

Figure 1 Synchronous Design, Block Flow Diagram.

2.3 Asynchronous Design

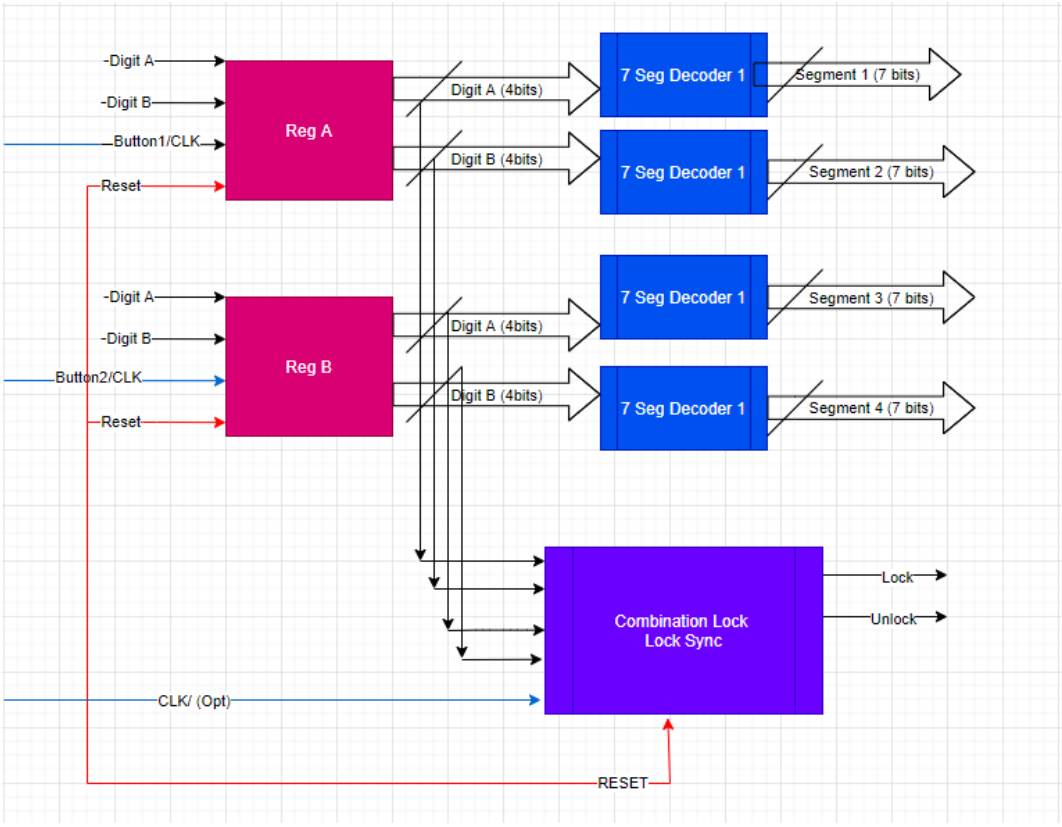

Figure 2 Asynchronous Design, Block Flow Diagram.

- Notes:
  - Here the reset switches are connected in common to reduce design complexity.
  - Notice that the Register clocks are now independent of each other, thus the circuit now behaves asynchronously at the register level.

2.4 Design Approach and Flow Description

- A **top down test-driven** development approach was used to create the above systems, following these steps.
  I. Planning and a high-level overview of how the system works. (design of *figures 1,2)*
  II. Creating the individual blocks and test beds for these blocks to test I/O
  III. Creating a top-level design which connects the blocks one at a time and testing I/O with a system testbed.
  IV. Verify simulations meet design criteria.

3. Simulation and Results

3.1 Synchronous Design Results

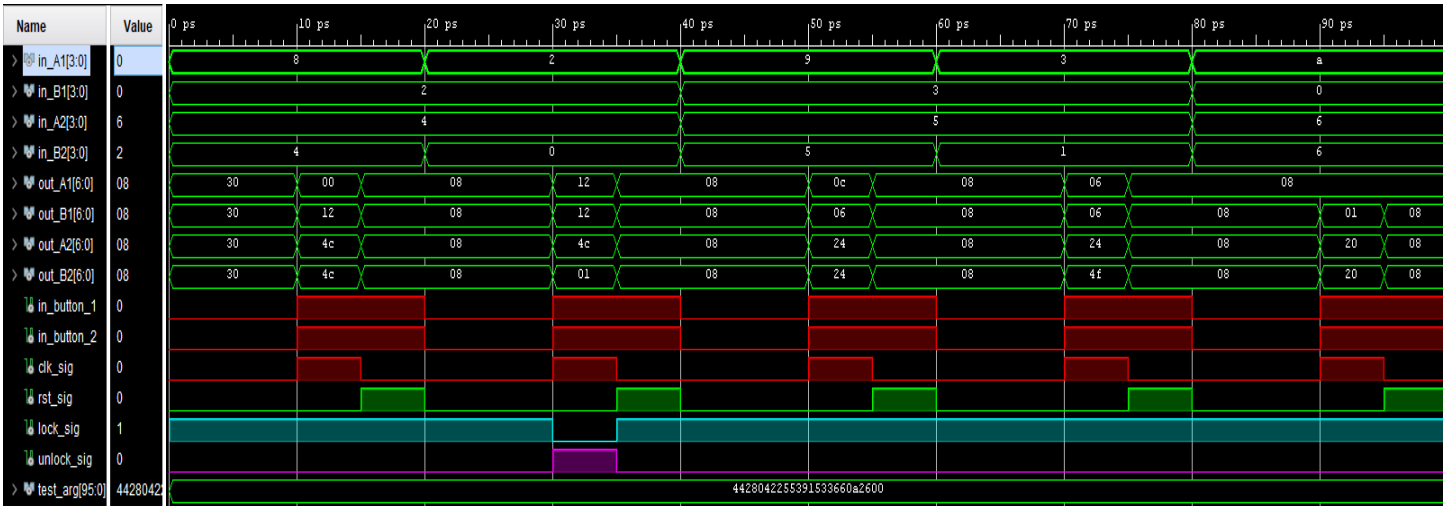

Figure 3 Synchronous Design Simulation Results

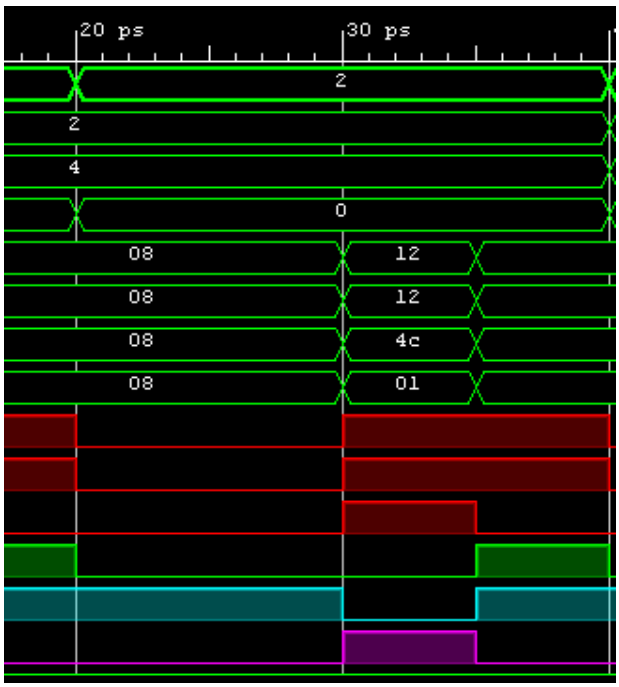

Figure 4 Synchronous Design Simulation Results Zoomed In

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Note: Lock Has Been Unlocked
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Figure 5 Unlock Assertion Statement

The simulation results indicate the system is responding as expected, as seen here, the *unlock_sig* (pink), is only HIGH when the right sequence is entered (0422) in the order specified in the assumptions *(sections 2.1)*. It is also seen that the register outputs (and thus the segment decoder outputs) only update on a positive clock edge event and will display "AAAA" when reset (08). Here, we can treat the buttons as an 'ENABLE' as I designed it this way. This is to clearly show that, when reset occurs, regardless of CLK the registers are reset to make the 7 segments display "AAAA" **immediately**.

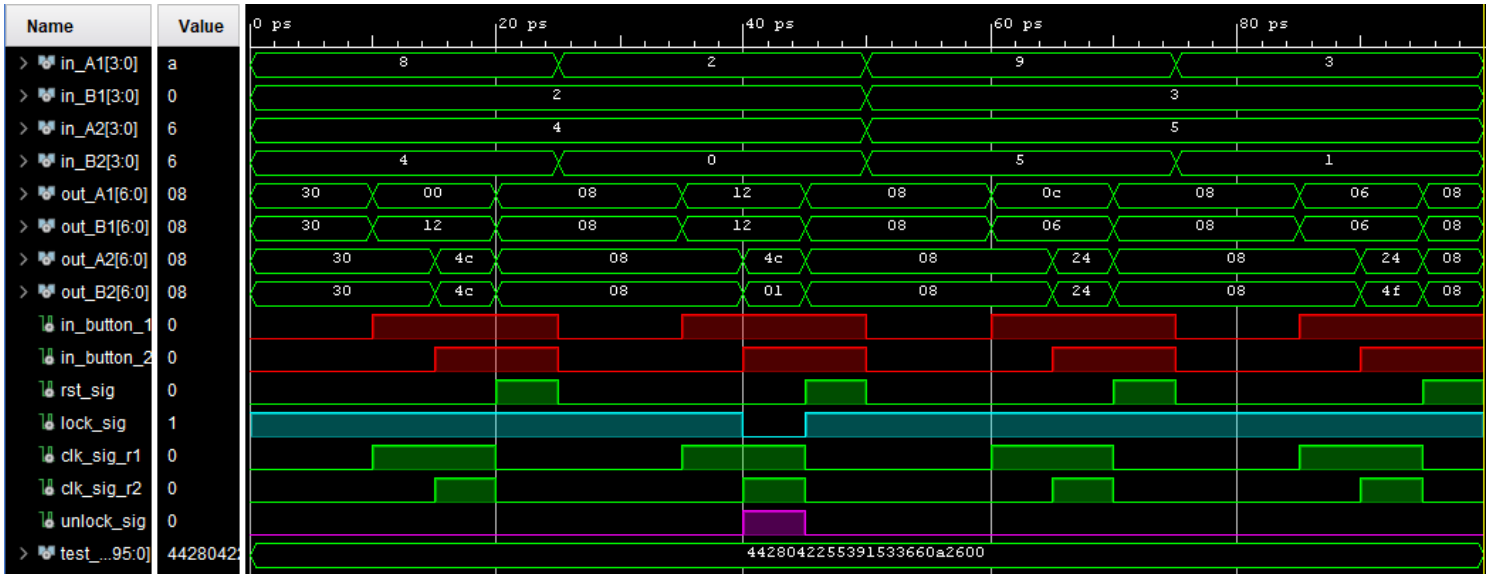

Figure 6 Asynchronous Design, Simulation

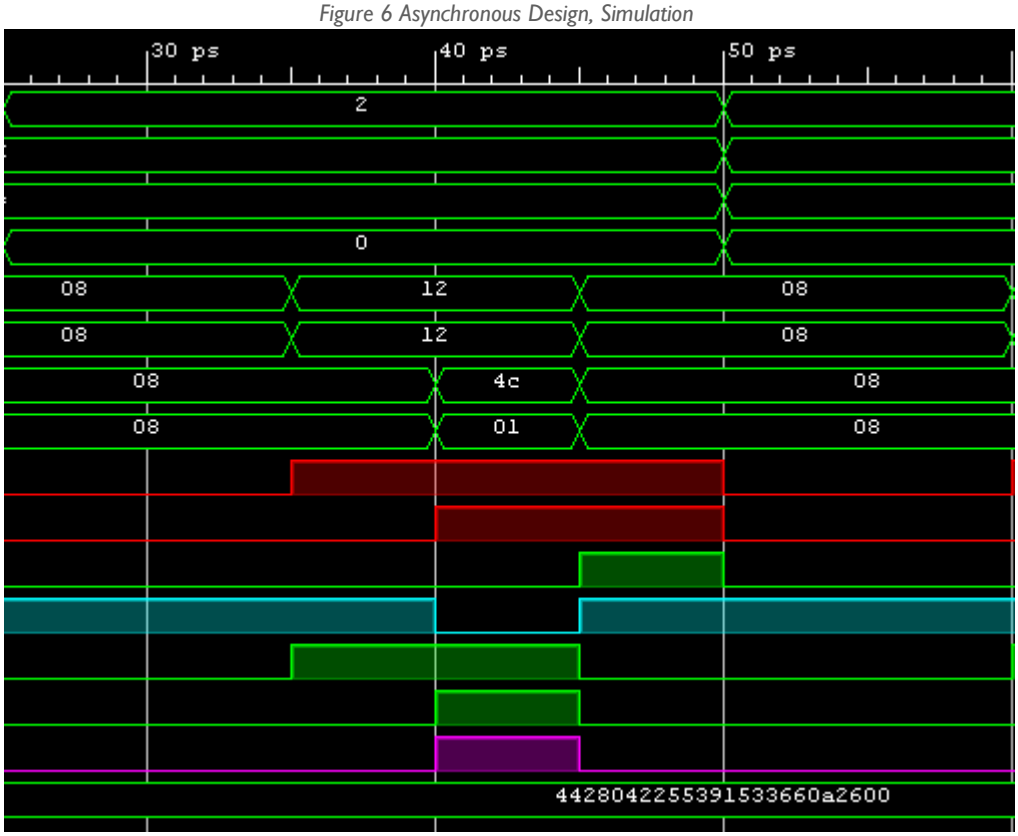

Figure 7 Asynchronous Design, Zoomed

Within the testbed, I have set a clock delay and a button press delay, this is seen in *figure 6/7* on the red signals and clk_sig_r1/r2. Notice how unlock_sig is only high when all the correct inputs are sent out from the registers. This is the expected behavior of this Asynchronous design. In contrast, *figure 4*, **synchronous design the system has a common clock,** and everything works based on that.

4. Schematics

4.1 Synchronous Design – RTL Schematic

Refer to appendix 6.1 for a full implemented schematic view.

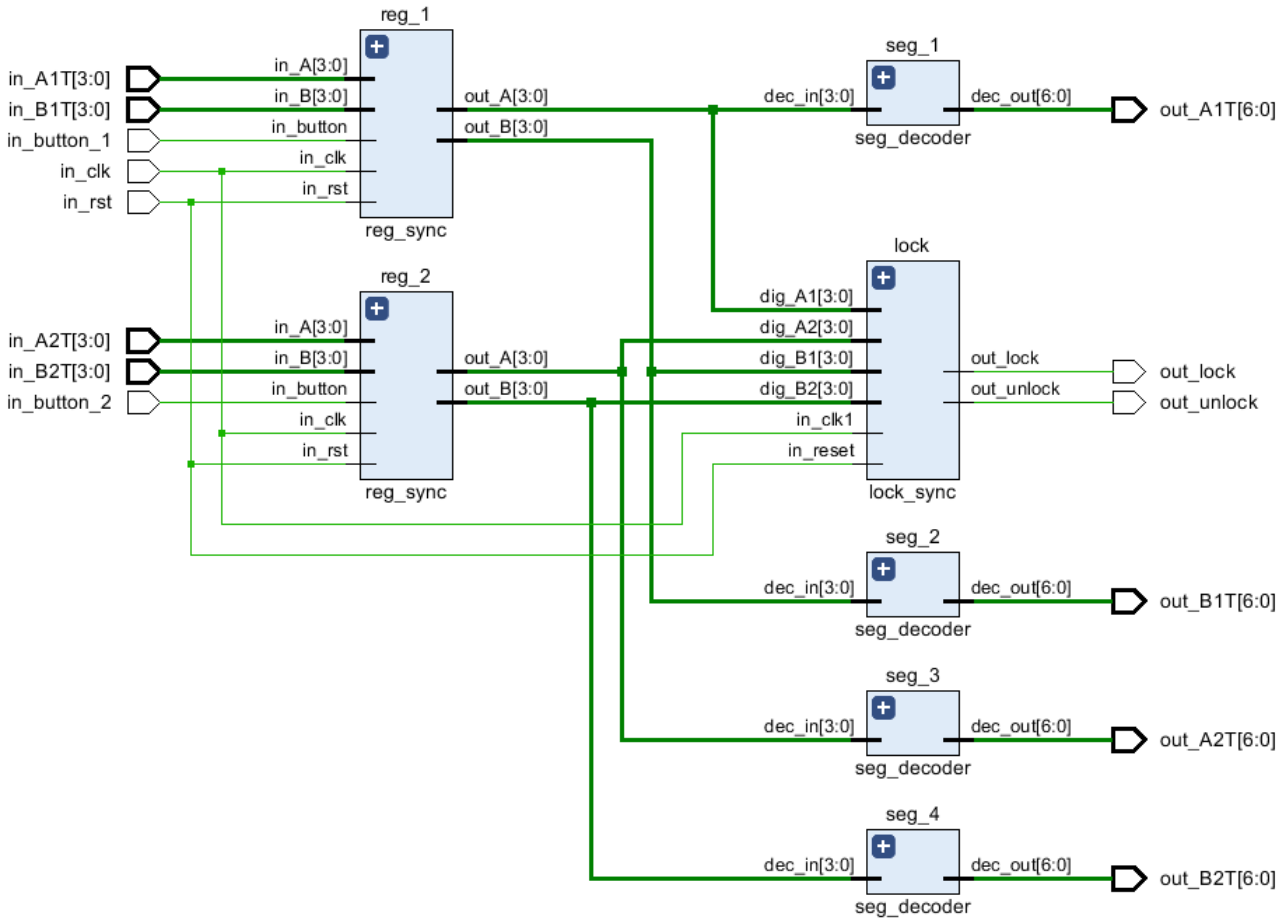

Figure 8 RTL Schematic Register I/O

Figure 6 shows the RTL synthesized schematic for the synchronous design, here we see that this design is quite like the implemented top-level design in *figure1*. Registers 1 and 2 (reg_1, reg_2) both have the expected design I/O and most importantly a common CLK/RST due to the synchronous nature of this device.

Note Design Assumption:

- The component **lock_sync** also operates on the same CLK/RST signal as the registers as I assumed that this is what the spec wanted to be implemented, however, this can be change within the behavioral description of the component if required.
- I have since removed the functionality of this CLK signal on the LOCK (but the connection is still there and serves no purpose as of now – To be removed) [1].

4.2 Asynchronous Design – RTL Schematic

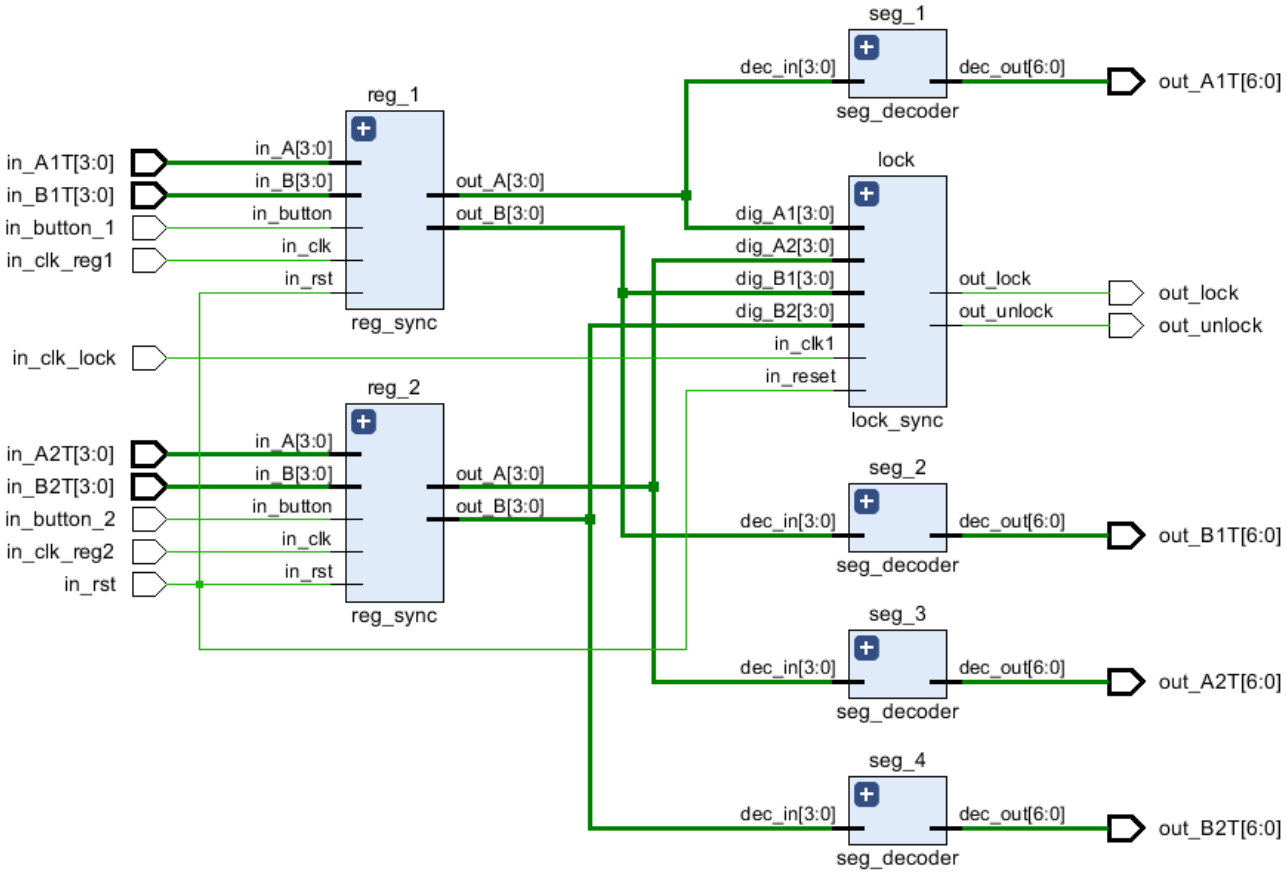

Figure 9 Asynchronous Design RTL Schematic - Uncommon Clock

Comparing the asynchronous design to the synchronous design, it is seen that the register clocks are independent. This theoretically allows for faster processing speed as **their speed is limited mainly by the propagation delay of the logic gates/circuit** (not having to wait for a clock). This would be the ideal design for combinational lock circuit.

Note Design Assumption:

- I initially interpreted the push buttons to work as an 'Enable' in both the designs, hence why there's both a button input and a clock input to the registers [2].
- In the test bed these two signals are essentially linked together (for individual register – remains asynchronous). As the register entity I made requires them **both to be high**, to process input.

5. FPGA Resource Consumption

5.1 Resource Consumption – Synchronous Design

Name	Slice LUTs (63400)	Slice Registers (126800)	Slice (15850)	LUT as Logic (63400)	Bonded IOB (210)	BUFGCTRL (32)
N locktop_sync	20	16	10	20	50	1
reg_1 (reg_sync)	9	8	7	9	0	0
reg_2 (reg_sync_0)	11	8	7	11	0	0

Figure 10 The FPGA resource utilization of the implemented design

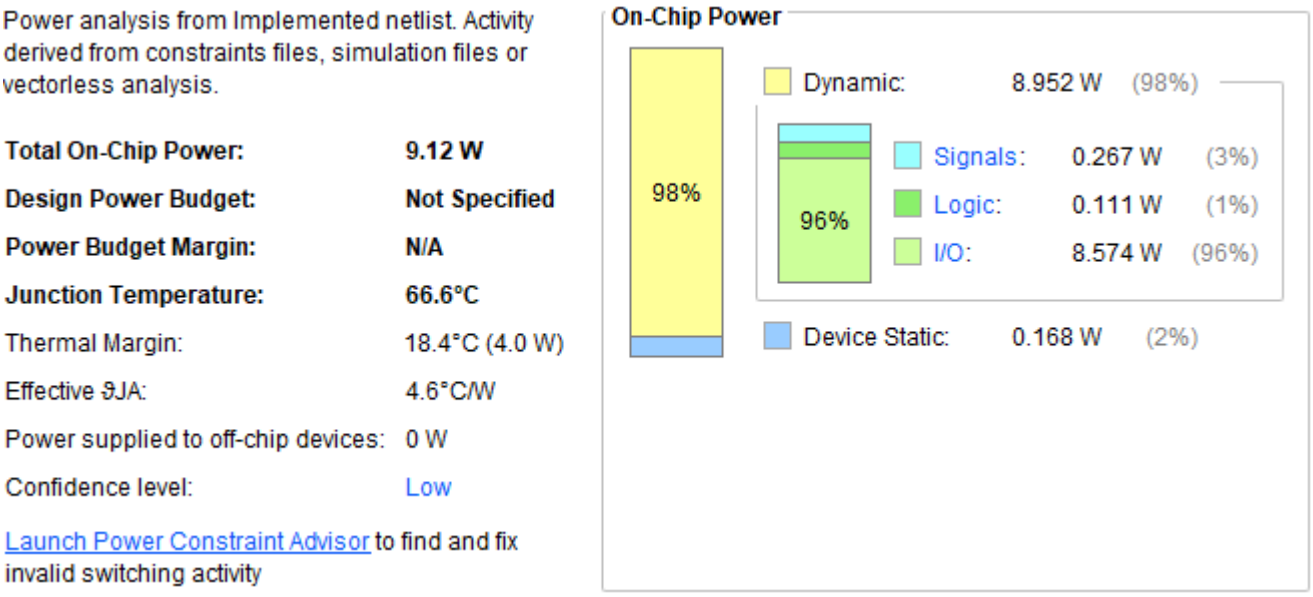

Figure 11 Power Usage - Synchronous Design

The power usage is based on **default Vivado config** settings for a power supply, as device specifications are not listed in the spec.

Figure 9 shows the total usage of components on the synthesized designed that is to be implemented on the FPGA.

5.2 Resource Consumption – Asynchronous Design

Name	Slice LUTs (63400)	Slice Registers (126800)	Slice (15850)	LUT as Logic (63400)	Bonded IOB (210)	BUFGCTRL (32)
N locktop_sync	20	16	10	20	51	2
reg_1 (reg_sync)	9	8	6	9	0	0
reg_2 (reg_sync_0)	11	8	5	11	0	0

Figure 12 Asynchronous Design, Implementation (FBGA) resource consumption

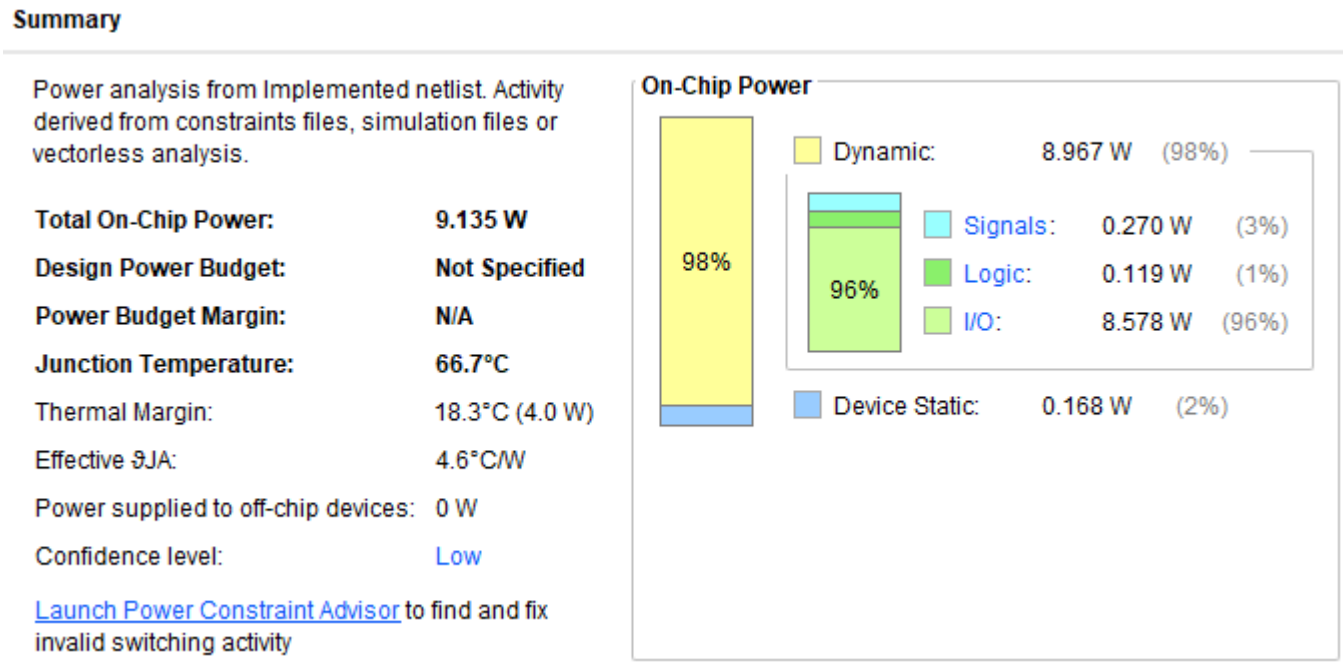

Figure 13 Expected Power Usage (Default PSU Config)

Comparing the above resource consumption to the synchronous design, they are mostly identical due to the overlap in component usage, however, less slices are used by the asynchronous implementation. Additionally, the power usage is almost identical (both using default PSU config) with the asynchronous design having a slightly high Junction Temp due to the slightly higher power draw.

6. Summary and Recommendations

Two design implantations have been made in this project, a synchronous combinational lock and an asynchronous one. To ensure that the designs work as expected, a self-checking test bed was created to test the accuracy of the designs. There were a few design flaws that were addressed in the assumptions section in *sections 4.1 and 4.2* see [1], [2]. To improve the design, and to reduce the implementation resource cost, it is recommended that these changes are made (clock / button).

The goal to understand the top down test driven development approach and to learn the operational differences between synchronous and asynchronous designs has been **achieved in this project.**

7. Appendix

6.1 RTL Synthesized Schematic – Synchronous Design

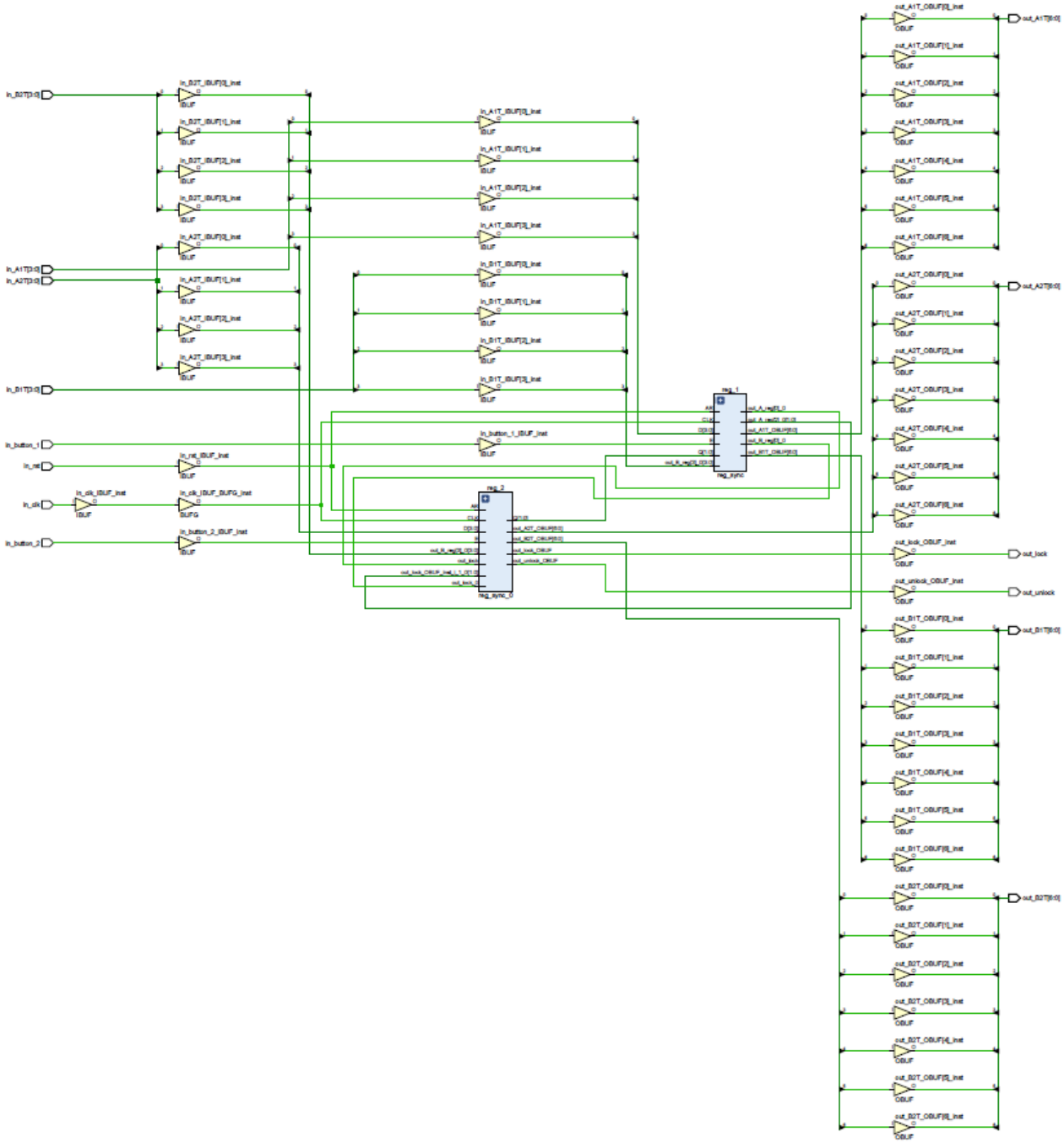

Figure 14 Implemented Design

6.2 RTL Synthesized Schematic – Asynchronous Design

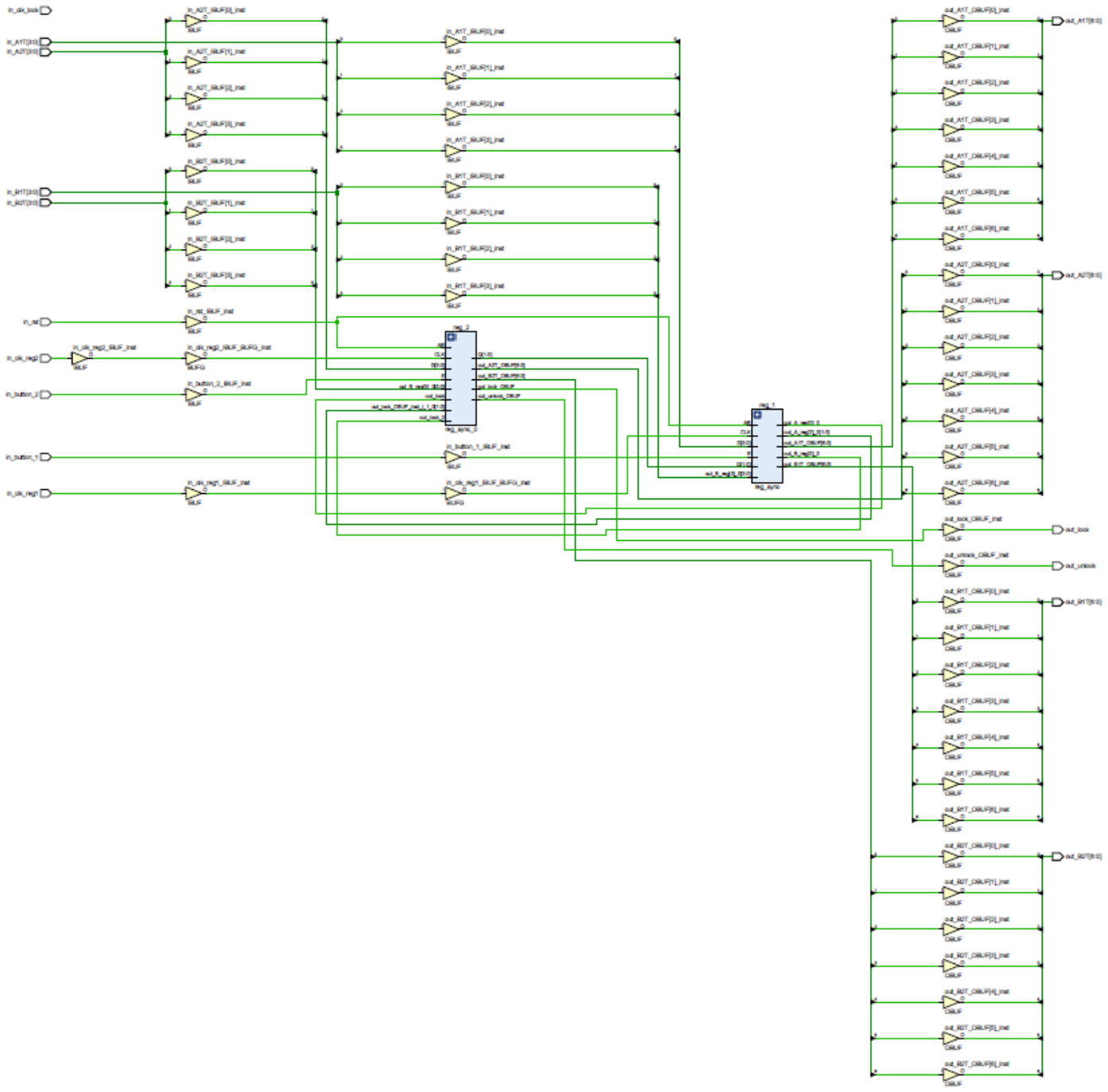

Figure 15 A synchro Design Implementation

8. Marking Criteria

Marks	Criteria
Simulation	
0	Simulation not attempted or does not work
1	Simulation partially works for one or both designs (waveforms only)
2	Simulation fully works (no self checking) for only one design
3	Simulation fully works (self checking) for only one design
4	Simulation fully works (self checking) for both designs
Report	
0	No evidence of content or work
1	Some content, insufficient explanation of circuit
2	Reasonable content, some explanation of circuit
3	Good content, reasonable explanation of circuit
4	Excellent content, good explanation of circuit
Oral assessment	
0	No knowledge of the design
1	Very little knowledge of the design
2	Reasonable knowledge of the design
3	Good knowledge of the design.
4	Excellent knowledge of the design.
Total (12):	**Marker Initials:** **Date:**