2022100124 권서은

1. RCA 16

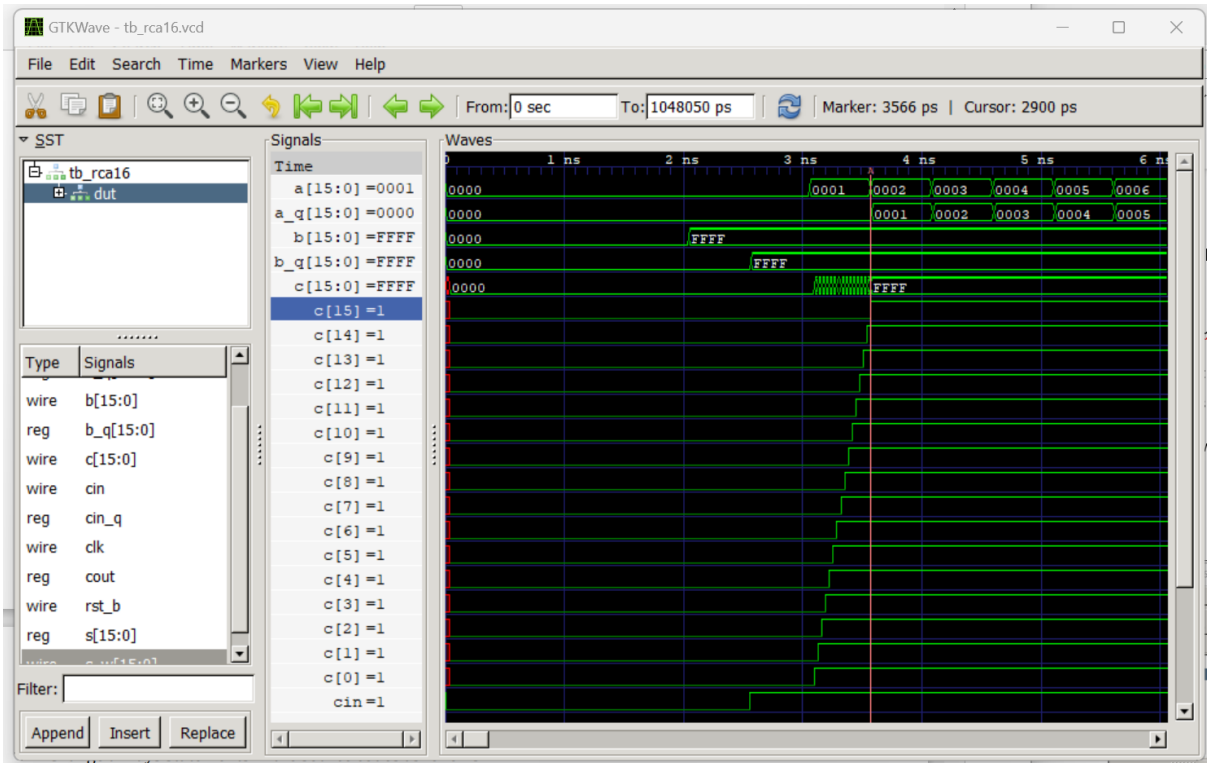
b) The critical path is Cin -> Cout.

If we look at the 16-bit adder, the input signals to adders are a, b and cin, and the output signals are s and cout.

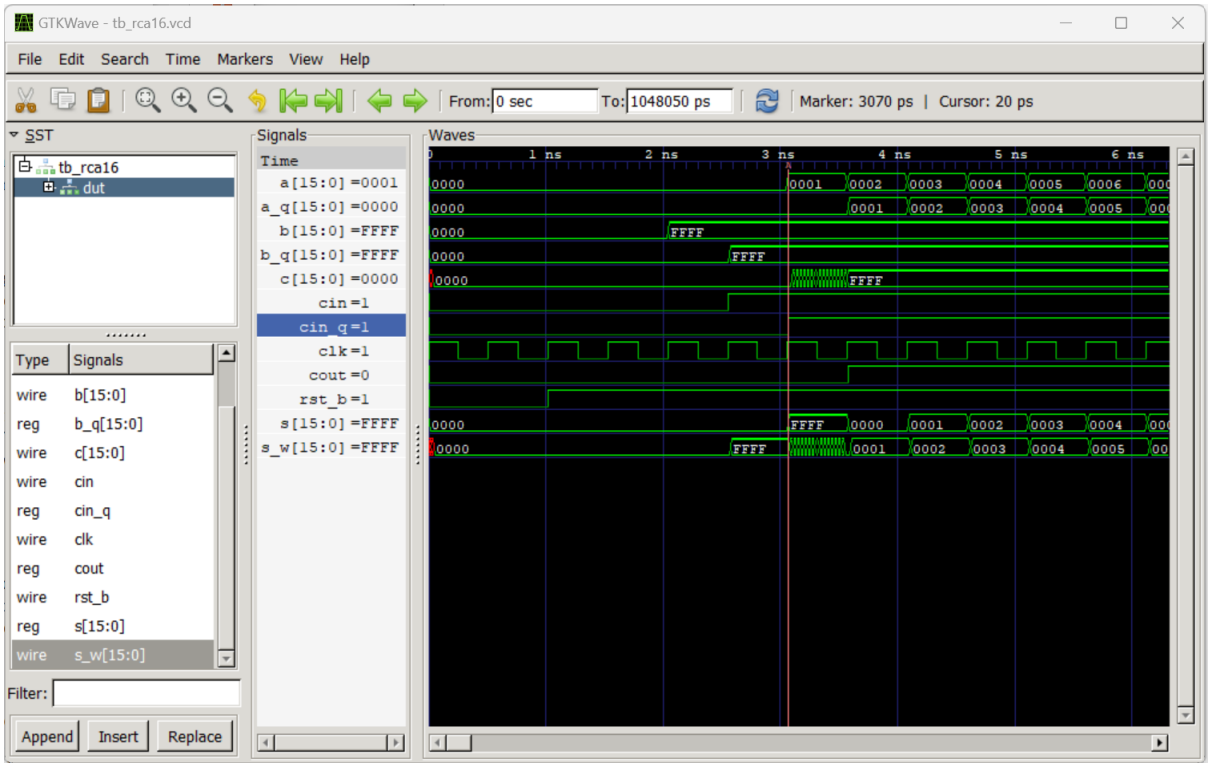
If we look at the waveform, the time when c[15], the last node of cout, becomes 1 is 3566ps, and the time when cin_q becomes 1 is 3070ps. Since c[15] is the last node of cout, the delay from cin_q to cout is 496ps.

However, if we consider Cin -> S, we have to see the delay from cin_q to s_w[15], the last node of S. The time when s_w[15] becomes 1 is 3545ps, and the time when cin_q becomes 1 is 3070ps. So the delay from cin_q to s_w[15] is 475ps.

c)



This is the marker line when c[15], the last node of cout, changes from 1'b0 to 1'b1. The location (time) of a marker is 3566ps.



This is the marker line when cin_q changes from 0 to 1. The location (time) of a marker is 3070ps.

Since 3566ps – 3070ps is 496ps, the delay of the critical path in the RCA16 design is 496ps.

d)

The shortest clock period that can generate correct result is 510 ps, since the delay of the critical path is 496ps, and the t_pcq of D flip-flop is 10ps. If we add them together, it is 506ps, but since the clock periods should be figured out in 10ps resolution, we can say that the shortest clock period is 510ps.

2. CLA

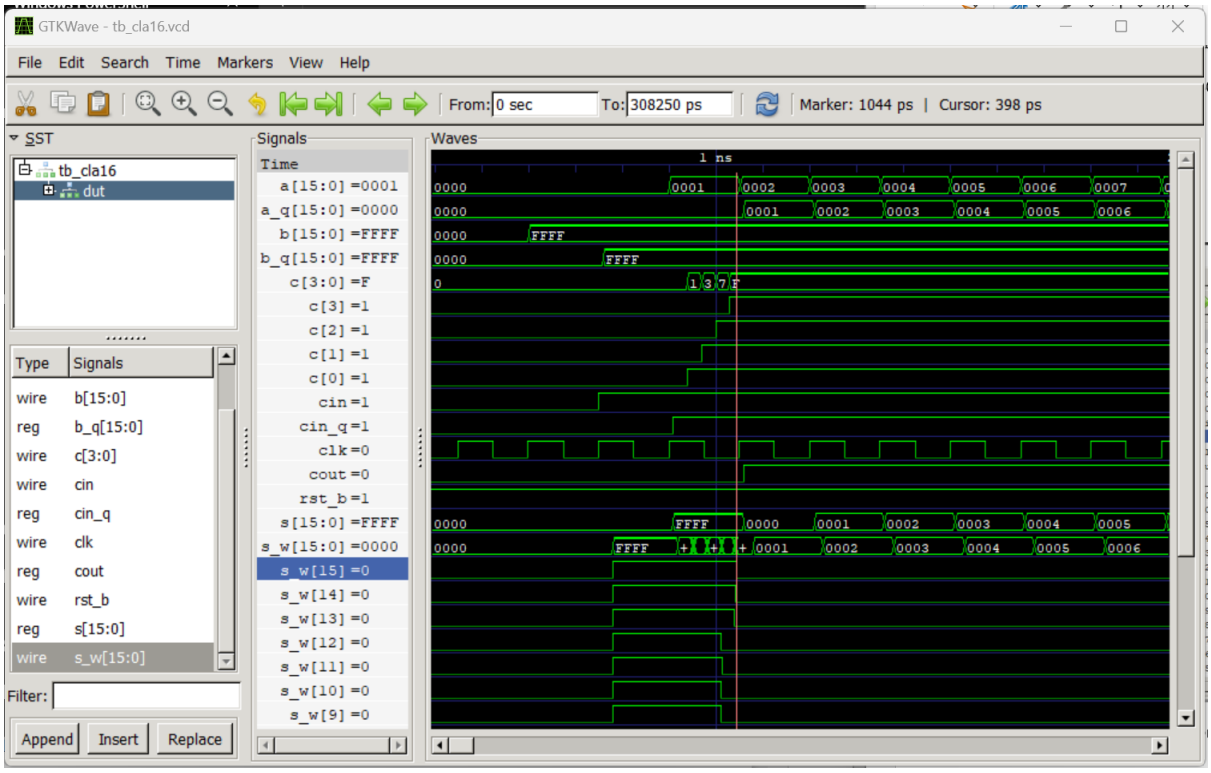
b) The critical path is cin -> s.

If we look at the 16-bit adder, the input signals to adders are a, b and cin, and the output signals are s and cout.

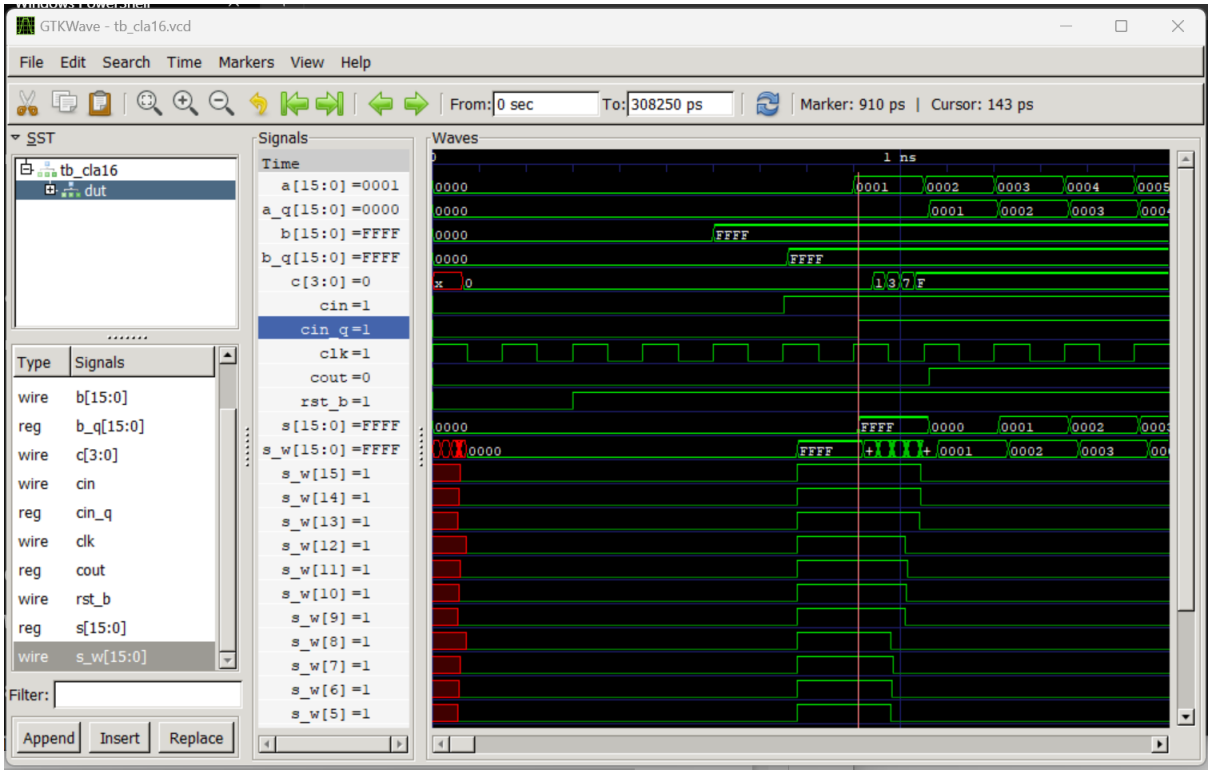
If we look at the waveform, the time when c[3], the last node of cout, becomes 1 is 1030ps, and the time when cin_q becomes 1 is 910ps. Since c[3] is the last node of cout, the delay from cin_q to cout is 120ps.

However, if we consider Cin -> S, we have to see the delay from cin_q to s_w[15], the last node of S. The time when s_w[15] becomes 1 is 1044ps, and the time when cin_q becomes 1 is 910ps. So the delay from cin_q to s_w[15] is 134ps.

c)



This is the marker line when s_w[15], the last node of s, changes from 1'b0 to 1'b1. The location (time) of a marker is 1044ps.



This is the marker line when cin_q changes from 0 to 1. The location (time) of a marker is 910ps.

Since 1044ps – 910ps is 134ps, the delay of the critical path in the CLA16 design is 134ps.

d)

The shortest clock period that can generate correct result is 150 ps, since the delay of the critical path is 134ps, and the t_pcq of D flip-flop is 10ps. If we add them together, it is 144ps, but since the clock periods should be figured out in 10ps resolution, we can say that the shortest clock period is 150ps.