



### Chapter 6 Topics



- Assembly Language
- Machine Language
- Programming
- Addressing Modes
- Lights, Camera, Action: Compiling, Assembling, & Loading
- Odds and Ends



### Introduction



### Architecture:

- Programmer's view of computer
- Defined by instructions & operand locations
- Instruction set architecture (ISA)
- Chapter 6

### Microarchitecture:

- How to implement an architecture in hardware
- Chapter 7

# Assembly Language



- Instructions: commands in a computer's language
  - Assembly language: human-readable format of instructions
  - Machine language: computer-readable format (1's and 0's)
- MIPS architecture:
  - Developed by John Hennessy and his colleagues at Stanford and in the 1980's.
  - Used in many commercial systems, including Silicon Graphics, Nintendo, and Cisco

Once you've learned one architecture, it's easy to learn others

### John Hennessy



- President of Stanford University
- Professor of Electrical Engineering and Computer Science at Stanford since 1977
- Coinvented the Reduced Instruction Set Computer (RISC) with David Patterson
- Developed the MIPS architecture at Stanford in 1984 and cofounded MIPS Computer Systems
- As of 2004, over 300 million MIPS microprocessors have been sold





# Architecture Design Principle

Underlying design principles, as articulated by Hennessy and Patterson:

- 1. Simplicity favors regularity
- 2. Make the common case fast
- 3.Smaller is faster
- 4.Good design demands good compromises



### Instructions: Addition



```
C Code a = b + c;
```

MIPS assembly code

add a, b, c

- add: mnemonic indicates operation to perform
- b, c: source operands (on which the operation is performed)
- a: destination operand (to which the result is written)



### Instructions: Subtraction



Similar to addition - only mnemonic changes

```
C Code a = b - c;
```

MIPS assembly code

sub a, b, c

- sub: mnemonic
- b, c: source operands
- a: destination operand



# Design Principle 1



### Simplicity favors regularity

- Consistent instruction format
- Same number of operands (two sources and one destination)
- easier to encode and handle in hardware







 More complex code is handled by multiple MIPS instructions.

## C Code a = b + c - d;

#### MIPS assembly code

```
add t, b, c \# t = b + c sub a, t, d \# a = t - d
```



# Design Principle 2



### Make the common case fast

- MIPS includes only simple, commonly used instructions
- Hardware to decode and execute instructions can be simple, small, and fast
- More complex instructions (that are less common) performed using multiple simple instructions
- MIPS is a *reduced instruction set computer* (RISC), with a small number of simple instructions
- Other architectures, such as Intel's x86, are complex instruction set computers (CISC)



### Operands



- Operand location: physical location in computer
  - Registers
  - Memory
  - Constants (also called *immediates*)



# Operands: Registers



- MIPS has 32 32-bit registers
- Registers are faster than memory
- MIPS called "32-bit architecture" because it operates on 32-bit data



# Design Principle 3



### **Smaller** is Faster

MIPS includes only a small number of registers







Name	Register Number	Usage		
\$0	0	the constant value 0		
\$at	1	assembler temporary		
\$v0-\$v1	2-3	Function return values		
\$a0-\$a3	4-7	Function arguments		
\$t0-\$t7	8-15	temporaries		
\$s0-\$s7	16-23	saved variables		
\$t8-\$t9	24-25	more temporaries		
\$k0-\$k1	26-27	OS temporaries		
\$gp	28	global pointer		
\$sp	29	stack pointer		
\$fp	30	frame pointer		
\$ra	31	Function return address		



# Operands: Registers



- Registers:
  - \$ before name
  - Example: \$0, "register zero", "dollar zero"
- Registers used for specific purposes:
  - \$0 always holds the constant value 0.
  - the saved registers, \$s0-\$s7, used to hold variables
  - the *temporary registers*, \$t0 \$t9, used to hold intermediate values during a larger computation
  - Discuss others later



# Instructions with Registers



Revisit add instruction

#### C Code

$$a = b + c$$

### MIPS assembly code

```
\# $s0 = a, $s1 = b, $s2 = c add $s0, $s1, $s2
```



## Operands: Memory



- Too much data to fit in only 32 registers
- Store more data in memory
- Memory is large, but slow
- Commonly used variables kept in registers



# Word-Addressable Memory

Each 32-bit data word has a unique address

Word Address	Data	
	•	•
•	•	•
0000003	4 0 F 3 0 7 8 8	Word 3
00000002	0 1 E E 2 8 4 2	Word 2
0000001	F 2 F 1 A C 0 7	Word 1
0000000	ABCDEF78	Word 0

# Reading Word-Addressable Memory

- Memory read called *load*
- Mnemonic: load word (lw)
- Format:
- lw \$s0, 5(\$t1)
- Address calculation:
  - add base address (\$t1) to the offset (5)
  - address = (\$t1 + 5)
- Result:
  - \$s0 holds the value at address (\$t1 + 5)
- Any register may be used as base address



# Reading Word-Addressable Memory

- Example: read a word of data at memory address 1 into \$s3
  - address = (\$0 + 1) = 1
  - \$s3 = 0xF2F1AC07 after load

#### **Assembly code**

```
lw $s3, 1($0) # read memory word 1 into $s3
```

Word Address				Da	ta				
				•					•
				•					•
00000003	4	0	F	3	0	7	8	8	Word 3
00000002	0	1	Ε	Ε	2	8	4	2	Word 2
0000001	F	2	F	1	Α	С	0	7	Word 1
00000000	Α	В	С	D	Ε	F	7	8	Word 0

# Writing Word-Addressable Memory



- Memory write are called *store*
- Mnemonic: store word (sw)



# Writing Word-Addressable Memory



- **Example:** Write (store) the value in \$t4 into memory address 3
  - add the base address (\$0) to the offset (0x3)
  - address: (\$0 + 0x3) = 3
  - Offset can be written in decimal (default) or hexadecimal
     Assembly code

```
sw $t4, 0x3($0) # write the value in $t4 # to memory word 3
```

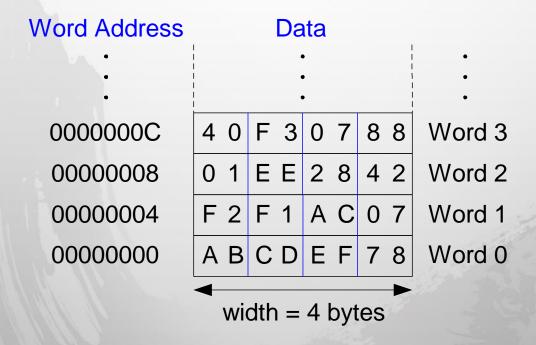
Word Address	Data	
•	•	•
	•	•
00000003	4 0 F 3 0 7 8 8	Word 3
00000002	0 1 E E 2 8 4 2	Word 2
0000001	F 2 F 1 A C 0 7	Word 1
00000000	ABCDEF78	Word 0



# Byte-Addressable Memory



- Each data byte has unique address
- Load/store words or single bytes: load byte (1b) and store byte (sb)
- 32-bit word = 4 bytes, so word address increments by 4



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## Reading Byte-Addressable Memory



- The address of a memory word must now be multiplied by 4. For example,
  - the address of memory word 2 is  $2 \times 4 = 8$
  - the address of memory word 10 is  $10 \times 4 = 40$  (0x28)
- MIPS is byte-addressed, not wordaddressed

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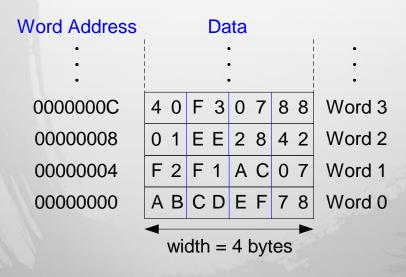
# Reading Byte-Addressable Memory



- **Example:** Load a word of data at memory address 4 into \$s3.
- \$s3 holds the value 0xF2F1AC07 after load

#### MIPS assembly code

lw \$s3, 4(\$0) # read word at address 4 into \$s3



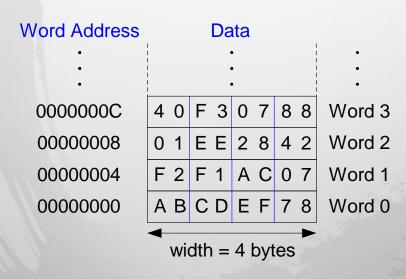


# Writing Byte-Addressable Memory

Example: stores the value held in \$t7 into memory address 0xC (12)

#### MIPS assembly code

```
sw $t7, 12($0) # write $t7 into address 12
```



# Big-Endian & Little-Endian Memory



- How to number bytes within a word?
- Little-endian: byte numbers start at the little (least significant) end
- Big-endian: byte numbers start at the big (most significant) end
- Word address is the same for big- or little-endian

Big-Endian				an	L	ittle	9- <b>E</b>	nc	liar	1
	Byte				Word					
	F	\dd	res	S	Address	F	Add	res	3	
			•	 	:	 			    	
	C	D	Е	F	С	F	Е	D	С	
	8	9	Α	В	8	В	Α	9	8	
1	4	5	6	7	4	7	6	5	4	
1	0	1	2	3	0	3	2	1	0	
MSB LSB			VISE	3	42	SB				

# Big-Endian & Little-Endian Memory



- Jonathan Swift's *Gulliver's Travels*: the Little-Endians broke their eggs on the little end of the egg and the Big-Endians broke their eggs on the big end
- It doesn't really matter which addressing type used except when the two systems need to share data!

Big-Endian				ian	L	ittle	e-E	nc	liar	1
Byte Address			/te res:	S	Word Address					
			•	•				   		
	С	D	Е	F	С	F	Е	D	С	
18	8	9	Α	В	8	В	Α	9	8	
1	4	5	6	7	4	7	6	5	4	
1	0	1	2	3	0	3	2	1	0	
MSB LSB				LSE	8	MSE	3	23.2	LSB	3



# Big-Endian & Little-Endian Example

- Suppose \$t0 initially contains 0x23456789
- After following code runs on big-endian system, what value is \$s0?
- In a little-endian system?

sw 
$$$t0, 0($0)$$
  
lb  $$s0, 1($0)$ 

- Big-endian: 0x0000045
- Little-endian: 0x00000067

# Big-Endian Word Byte Address 0 1 2 3 Address 3 2 1 0 Byte Address Data Value 23 45 67 89 0 23 45 67 89 Data Value MSB LSB MSB LSB



# Design Principle 4



### Good design demands good compromises

- Multiple instruction formats allow flexibility
  - add, sub: use 3 register operands
  - lw, sw: use 2 register operands and a constant
- Number of instruction formats kept small
  - to adhere to design principles 1 and 3 (simplicity favors regularity and smaller is faster).

# Operands: Constants/Immediates

- lw and sw use constants or *immediates*
- immediately available from instruction
- 16-bit two's complement number
- addi: add immediate
- Subtract immediate (subi) necessary?

#### C Code

$$a = a + 4;$$
  
 $b = a - 12;$ 

### MIPS assembly code

```
\# $s0 = a, $s1 = b addi $s0, $s0, 4 addi $s1, $s0, -12
```



### Machine Language



- Binary representation of instructions
- Computers only understand 1's and 0's
- 32-bit instructions
  - Simplicity favors regularity: 32-bit data & instructions
- 3 instruction formats:
  - R-Type: register operands
  - I-Type:immediate operand
  - J-Type: for jumping (discuss later)







- Register-type
- 3 register operands:

- rs, rt: source registers

rd: destination register

Other fields:

op: the operation code or opcode (0 for R-type instructions)

- funct: the function

with opcode, tells computer what operation to

perform

- shamt: the shift amount for shift instructions, otherwise it's 0

### **R-Type**

op	rs	rt	rd	shamt	funct
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits



# R-Type Examples



### **Assembly Code**

add \$s0, \$s1, \$s2 sub \$t0, \$t3, \$t5

#### Field Values

ор	rs	rt	rd	shamt	funct
0	17	18	16	0	32
0	11	13	8	0	34
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

### **Machine Code**

ор	rs	rt	rd	shamt	funct	
000000	10001	10010	10000	00000	100000	(0x02328020)
000000	01011	01101	01000	00000	100010	(0x016D4022)
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits	

Note the order of registers in the assembly code:

add rd, rs, rt







- Immediate-type
- 3 operands:
  - rs, rt: register operands
  - imm: 16-bit two's complement immediate
- Other fields:
  - op: the opcode
  - Simplicity favors regularity: all instructions have opcode
  - Operation is completely determined by opcode

### **I-Type**

ор	rs	rt	imm
6 bits	5 bits	5 bits	16 bits







### **Assembly Code**

### addi \$s0, \$s1, 5 addi \$t0, \$s3, -12 lw \$t2, 32(\$0) sw \$s1, 4(\$t1)

### Field Values

ор	rs	rt	imm
8	17	16	5
8	19	8	-12
35	0	10	32
43	9	17	4
6 bits	5 bits	5 bits	16 bits

**Note** the differing order of registers in assembly and machine codes:

addi	rt,	rs,	imm
lw	rt,	imm	(rs)
SW	rt,	imm	(rs)

#### Machine Code

ор	rs	rt	imm	
001000	10001	10000	0000 0000 0000 0101	(0x22300005)
001000	10011	01000	1111 1111 1111 0100	(0x2268FFF4)
100011	00000	01010	0000 0000 0010 0000	(0x8C0A0020)
101011	01001	10001	0000 0000 0000 0100	(0xAD310004)
6 bits	5 bits	5 bits	16 bits	



# Machine Language: J-Type



- Jump-type
- 26-bit address operand (addr)
- Used for jump instructions (j)

### **J-Type**

op	addr	
6 bits	26 bits	



# Review: Instruction Formats



### **R-Type**

op	rs	rt	rd	shamt	funct	
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits	

### **I-Type**

ор	rs	rt	imm
6 bits	5 bits	5 bits	16 bits

### **J-Type**

op	addr	
6 bits	26 bits	371.65



### Exercise



Encode the following instruction to the machine language.

Mnemonic	OP code	Function code	Туре
add	0x0	32	R

### **Assembly Code**

add \$a0, \$t0, \$t1

#### Field Values

ор	rs	rt	rd	shamt	funct	
	6					
		1 11 1				
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits	

Register name	Register number
\$0	0
\$at	1
\$v0-\$v1	2-3
\$a0-\$a3	4-7
\$t0-\$t7	8-15
\$s0-\$s7	16-23
\$t8-\$t9	24-25
\$k0-\$k1	26-27
\$gp	28
\$sp	29
\$fp	30
\$ra	31



# Power of the Stored Program

- 32-bit instructions & data stored in memory
- Sequence of instructions: only difference between two applications
- To run a new program:
  - No rewiring required
  - Simply store new program in memory
- Program Execution:
  - Processor fetches (reads) instructions from memory in sequence
  - Processor performs the specified operation



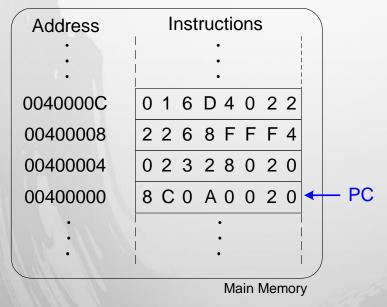




As	sembl	Machine Code		
lw	\$t2,	32 (\$	0)	0x8C0A0020
add	\$s0,	\$s1,	\$s2	0x02328020
addi	\$t0,	\$s3,	-12	0x2268FFF4

sub \$t0, \$t3, \$t5 0x016D4022

#### **Stored Program**



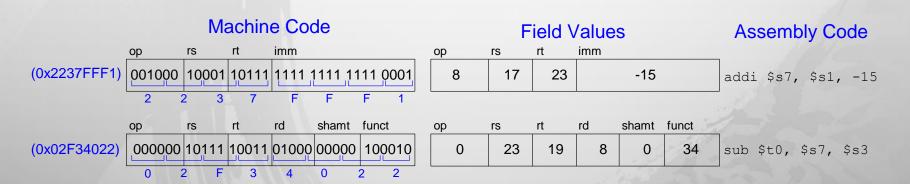
**Program Counter (PC):** keeps track of current instruction



# Interpreting Machine Code



- Start with opcode: tells how to parse rest
- If opcode all 0's
  - R-type instruction
  - Function bits tell operation
- Otherwise
  - opcode tells operation





## Programming



- High-level languages:
  - e.g., C, Java, Python
  - Written at higher level of abstraction
- Common high-level software constructs:
  - if/else statements
  - for loops
  - while loops
  - arrays
  - function calls

## Logical Instructions



- and, or, xor, nor
  - and: useful for masking bits
    - Masking all but the least significant byte of a value:
    - 0xF234012F AND 0x000000FF = 0x0000002F
  - or: useful for combining bit fields
    - Combine 0xF2340000 with 0x000012BC:
    - 0xF2340000 OR 0x000012BC = 0xF23412BC
  - nor: useful for inverting bits:
    - A NOR \$0 = NOT A
- andi, ori, xori
  - 16-bit immediate is zero-extended (not sign-extended)
  - nori not needed







### Source Registers

<b>\$</b> s1	1111	1111	1111	1111	0000	0000	0000	0000
--------------	------	------	------	------	------	------	------	------

\$s2	0100	0110	1010	0001	1111	0000	1011	0111
------	------	------	------	------	------	------	------	------

### **Assembly Code**

and	\$s3,	\$s1,	\$s2
or	\$s4,	\$s1,	\$s2
xor	\$s5,	\$s1,	\$s2
nor	\$s6,	\$s1,	\$s2

### Result

<b>\$</b> s3					3//
<b>\$</b> s4				19	
<b>\$</b> s5				of la	
<b>\$</b> s6					a di





### Source Registers

<b>\$</b> s1	1111	1111	1111	1111	0000	0000	0000	0000
		· · · · · · · · · · · · · · · · · · ·						

s2 (	0100	0110	1010	0001	1111	0000	1011	0111
------	------	------	------	------	------	------	------	------

### **Assembly Code**

and	\$s3,	\$s1,	\$s2
or	\$s4,	\$s1,	\$s2
xor	\$s5,	\$s1,	\$s2
nor	\$s6,	\$s1,	\$s2

### Result

<b>\$</b> s3	0100	0110	1010	0001	0000	0000	0000	0000
<b>\$</b> s4	1111	1111	1111	1111	1111	0000	1011	0111
<b>\$</b> s5	1011	1001	0101	1110	1111	0000	1011	0111
<b>\$</b> s6	0000	0000	0000	0000	0000	1111	0100	1000



xori \$s4, \$s1, 0xFA34 **\$s4** 





#### Source Values

								4.00	aido			
				<b>\$</b> s1	0000	0000	0000	0000	0000	0000	1111	1111
				imm	0000	0000	0000	0000	1111	1010	0011	0100
					4	zero-ex	xtended					
A	ssemb	ly Code	е					Resi	ult			
andi	\$s2,	\$s1,	0xFA34	<b>\$</b> s2								1
ori	\$s3,	\$s1,	0xFA34	\$s3							À	4/4







#### **Source Values**

<b>\$</b> s1	0000	0000	0000	0000	0000	0000	1111	1111		
imm	0000	0000	0000	0000	1111	1010	0011	0100		
zero-extended >										

### **Assembly Code**

### Result

andi	\$s2,	\$s1,	0xFA34	<b>\$</b> s2	0000	0000	0000	0000	0000	0000	0011	0100
ori	\$s3,	\$s1,	0xFA34	<b>\$</b> s3	0000	0000	0000	0000	1111	1010	1111	1111
xori	\$s4,	\$s1,	0xFA34	<b>\$</b> s4	0000	0000	0000	0000	1111	1010	1100	1011

### Shift Instructions



- sll: shift left logical
  - Example: sll \$t0, \$t1, 5 # \$t0 <= \$t1 << 5</pre>
- srl: shift right logical
  - Example: srl \$t0, \$t1, 5 # \$t0 <= \$t1 >> 5
- sra: shift right arithmetic
  - Example: sra \$t0, \$t1, 5 # \$t0 <= \$t1 >>> 5

# Variable Shift Instructions



- sllv: shift left logical variable
  - Example: sllv \$t0, \$t1, \$t2 # \$t0 <= \$t1 << \$t2</pre>
- srlv: shift right logical variable
  - Example: srlv \$t0, \$t1, \$t2 # \$t0 <= \$t1 >> \$t2
- srav: shift right arithmetic variable
  - Example: srav \$t0, \$t1, \$t2 # \$t0 <= \$t1 >>> \$t2







Assem	bl۱	/ Co	ode
, ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	$\sim$ .		

### Field Values

			ор	rs	rt	rd	shamt	funct
sll \$t0,	\$s1,	2	0	0	17	8	2	0
srl \$s2,	\$s1,	2	0	0	17	18	2	2
sra \$s3,	\$s1,	2	0	0	17	19	2	3
			6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

### Machine Code

ор	rs	rt	rd	shamt	funct	
000000	00000	10001	01000	00010	000000	(0x00114080)
000000	00000	10001	10010	00010	000010	(0x00119082)
000000	00000	10001	10011	00010	000011	(0x00119883)
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits	







• 16-bit constants using addi:

#### C Code

```
// int is a 32-bit signed word int a = 0x4f3c;
```

### MIPS assembly code

```
# $s0 = a addi $s0, $0, 0x4f3c
```

• 32-bit constants using load upper immediate (lui) and ori:

#### C Code

```
int a = 0xFEDC8765;
```

### MIPS assembly code







 What is the value stored in \$s1 at the end of its execution?

```
lui $s0, 0xFEDC
ori $s0, $s0, 0x4321
addi $t0, $0, 8
srav $s1, $s0, $t0
```







 How can we get the upper 16 bit of register \$s0?







Translate the following C code to MIPS assembly code. Suppose a is stored in \$s0, b is in \$s1, and c is in \$s2

```
c = (\sim (a \& 0xFF)) + 1 + (b \& 0xFF);
```



## Multiplication, Division



- Special registers: 10, hi
- 32 × 32 multiplication, 64 bit result
  - mult \$s0, \$s1
  - Result in {hi, lo}
- 32-bit division, 32-bit quotient, remainder
  - div \$s0, \$s1
  - Quotient in 10
  - Remainder in hi
- Moves from lo/hi special registers
  - mflo \$s2
  - mfhi \$s3



## Branching



- Execute instructions out of sequence
- Types of branches:
  - Conditional
    - branch if equal (beq)
    - branch if not equal (bne)

### - Unconditional

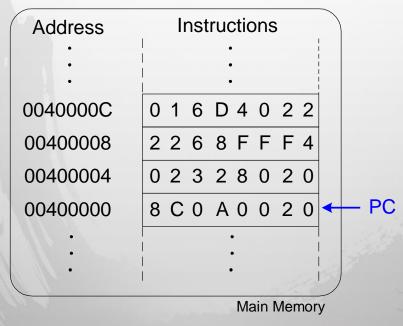
- jump (j)
- jump register (jr)
- jump and link (jal)



# Review: The Stored Program

As	sembl	y Code	)	Machine Code	
lw	\$t2,	32 (\$0	0)	0x8C0A0020	
add	\$s0,	\$s1,	\$s2	0x02328020	
addi	\$t0,	\$s3,	-12	0x2268FFF4	
sub	\$t0,	\$t3,	\$t5	0x016D4022	

#### **Stored Program**





# Conditional Branching (beq)

```
# MIPS assembly

addi $$0, $0, 4  # $$0 = 0 + 4 = 4

addi $$1, $0, 1  # $$1 = 0 + 1 = 1

$$1  $$1, $$1, 2  # $$1 = 1 << 2 = 4

beq $$0, $$1, target # branch is taken

addi $$1, $$1, 1  # not executed

sub $$1, $$1, $$0  # not executed

target:

add $$1, $$1, $$0  # $$1 = 4 + 4 = 8
```

Labels indicate instruction location. They can't be reserved words and must be followed by colon (:)



## The Branch Not Taken (bne)



### # MIPS assembly

```
addi $$0, $0, 4  # $$0 = 0 + 4 = 4 addi $$1, $0, 1  # $$1 = 0 + 1 = 1 $$1 $$1, $$1, 2  # $$1 = 1 << 2 = 4 addi $$1, $$1, $$1, $$1  # $$1 = 4 + 1 = 5 addi $$1, $$1, $$1, $$20  # $$1 = 5 - 4 = 1
```

### target:

add \$s1, \$s1, \$s0 #\$s1 = 1 + 4 = 5



# Unconditional Branching (†)



### # MIPS assembly

\$s0, \$0, 4 addi \$s1, \$0, 1 addi target \$s1, \$s1, 2 sra \$s1, \$s1, 1 addi sub \$s1, \$s1, \$s0

# \$s0 = 4# \$s1 = 1# jump to target # not executed # not executed # not executed

### target:

add



# Unconditional Branching (jr

```
# MIPS assembly
0x00002000 addi $s0, $0, 0x2010
0x00002004 jr $s0
0x00002008 addi $s1, $0, 1
0x0000200C sra $s1, $s1, 2
0x00002010 lw $s3, 44($s1)
```

jr is an R-type instruction.

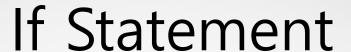


# Summary



Mnemonic	Туре	Operation	
and, or, xor, nor	R	Logical operation with registers	
andi, ori, xori	Ī	Logical operation with an immediate	
sll, srl	R	Logical shift	
sra	R	Arithmetic shift	
sllv, srlv	R	Variable logical shift	
srav	R	Variable arithmetic shift	
lui	I	Load upper immediate	
mult, div	R	Multiplication, division	
beq, bne	I	Conditional branch	
j	J	Unconditional branch	
jr	R	Unconditional branch	







### C Code

$$f = f - i;$$

### MIPS assembly code

```
\# $s0 = f, $s1 = g, $s2 = h
\# $s3 = i, $s4 = j
```



### If Statement



#### C Code

### MIPS assembly code

```
# $s0 = f, $s1 = g, $s2 = h
# $s3 = i, $s4 = j

bne $s3, $s4, L1
add $s0, $s1, $s2

L1: sub $s0, $s0, $s3
```

Assembly tests opposite case (i != j) of high-level code (i == j)



### If/Else Statement



### C Code

### MIPS assembly code

```
\# $s0 = f, $s1 = g, $s2 = h
\# $s3 = i, $s4 = j
```



### If/Else Statement



#### C Code

### MIPS assembly code



### While Loops



#### C Code

```
// determines the power \# \$s0 = pow, \$s1 = x
// of x such that 2^{x} = 128
int pow = 1;
int x = 0:
while (pow != 128) {
pow = pow * 2;
 x = x + 1;
```

### MIPS assembly code

Assembly tests for the opposite case (pow == 128) of the C code (pow != 128).



### While Loops



#### C Code

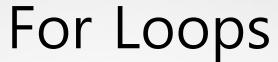
```
// determines the power \# \$s0 = pow, \$s1 = x
// of x such that 2^{x} = 128
int pow = 1;
int x = 0:
while (pow != 128) {
pow = pow * 2;
 x = x + 1;
```

### MIPS assembly code

```
addi $s0, $0, 1
       add $s1, $0, $0
       addi $t0, $0, 128
while: beg $s0, $t0, done
       sll $s0, $s0, 1
       addi $s1, $s1, 1
       i while
done:
```

Assembly tests for the opposite case (pow == 128) of the C code (pow != 128).







for (initialization; condition; loop operation)
 statement

- initialization: executes before the loop begins
- condition: is tested at the beginning of each iteration
- loop operation: executes at the end of each iteration
- statement: executes each time the condition is met







### C Code

```
// add the numbers from 0 to 9 \# $s0 = i, $s1 = sum
int sum = 0;
int i;
for (i=0; i!=10; i = i+1) {
sum = sum + i;
```

### MIPS assembly code







#### C Code

```
// add the numbers from 0 to 9 # $s0 = i, $s1 = sum
int sum = 0;
int i;
for (i=0; i!=10; i = i+1) {
sum = sum + i;
```

#### MIPS assembly code

```
addi $s1, $0, 0
      add $s0, $0, $0
      addi $t0, $0, 10
for: beq $s0, $t0, done
      add $s1, $s1, $s0
      addi $s0, $s0, 1
      i for
done:
```







#### C Code

```
// add the powers of 2 from 1 \# $s0 = i, $s1 = sum
// to 100
int sum = 0;
int i;
for (i=1; i < 101; i = i*2) {
sum = sum + i;
```

#### MIPS assembly code





#### C Code

```
// add the powers of 2 from 1 # $s0 = i, $s1 = sum
// to 100
int sum = 0;
int i;
for (i=1; i < 101; i = i*2) { loop:
sum = sum + i;
```

#### MIPS assembly code

```
addi $s1, $0, 0
addi $s0, $0, 1
addi $t0, $0, 101
slt $t1, $s0, $t0
beq $t1, $0, done
add $s1, $s1, $s0
sll $s0, $s0, 1
i loop
```

done:

$$t1 = 1$$
 if  $i < 101$ 



## Arrays



- Access large amounts of similar data
- Index: access each element
- Size: number of elements



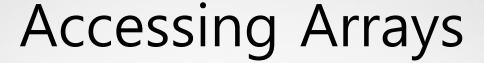
# Arrays



- 5-element array
- Base address = 0x12348000 (address of first element, array[0])
- First step in accessing an array: load base address into a register

0x12340010	array[4]
0x1234800C	array[3]
0x12348008	array[2]
0x12348004	array[1]
0x12348000	array[0]







```
// C Code
  int array[5];
  array[0] = array[0] * 2;
  array[1] = array[1] * 2;

# MIPS assembly code
# array base address = $s0 (0x12348000)
```



# Accessing Arrays



```
// C Code
  int array[5];
  array[0] = array[0] * 2;
   array[1] = array[1] * 2;
# MIPS assembly code
\# array base address = $s0 (0x12348000)
  lui $s0, 0x1234
                               # 0x1234 in upper half of $S0
  ori $s0, $s0, 0x8000
                               # 0x8000 in lower half of $s0
 lw $t1, 0($s0)
                              # $t1 = array[0]
                               # $t1 = $t1 * 2
  sll $t1, $t1, 1
     $t1, 0($s0)
                               # array[0] = $t1
  SW
 lw $t1, 4($s0)
                               # $t1 = array[1]
  sll $t1, $t1, 1
                               # $t1 = $t1 * 2
      $t1, 4($s0)
                                \# array[1] = $t1
  SW
```



# Arrays using For Loops



```
// C Code
  int array[1000];
  int i;

for (i=0; i < 1000; i = i + 1)
    array[i] = array[i] * 8;

# MIPS assembly code
# $s0 = array base address, $s1 = i</pre>
```



# Arrays Using For Loops

sll \$t1, \$t1, 3

addi \$s1, \$s1, 1

loop



# \$t1 = array[i] \* 8

# i = i + 1

# repeat

sw \$t1, 0(\$t0) # array[i] = array[i] \* 8

```
# MIPS assembly code
// C Code
                         \# $s0 = array base address, $s1 = i
  int array[1000];
  int i;
                         # initialization code
                          for (i=0; i < 1000; i = i
                          ori $s0, $s0, 0xF000 # $s0 = 0x23B8F000
  + 1)
                         addi $s1, $0, 0 # i = 0
       array[i] = array[i]
  * 8;
                          addi $t2, $0, 1000 # $t2 = 1000
                         loop:
                          slt $t0, $s1, $t2  # i < 1000?
                          beg $t0, $0, done # if not then done
                                               # $t0 = i * 4 (byte offset)
                          sll $t0, $s1, 2
                          add $t0, $t0, $s0  # address of array[i]
                          lw $t1, 0($t0) # $t1 = array[i]
```

done:

### **ASCII** Code



- American Standard Code for Information Interchange
- Each text character has unique byte value
  - For example, S = 0x53, a = 0x61, A = 0x41
  - Lower-case and upper-case differ by 0x20 (32)







#	Char	#	Char	#	Char	#	Char	#	Char	#	Char
20	space	30	0	40	æ	50	Р	60	,	70	р
21	!	31	1	41	A	51	Q	61	a	71	q
22		32	2	42	В	52	R	62	Ь	72	r
23	#	33	3	43	С	53	S	63	С	73	s
24	\$	34	4	44	D	54	Т	64	d	74	t
25	%	35	5	45	Ε	55	U	65	е	75	u
26	&	36	6	46	F	56	٧	66	f	76	v
27	,	37	7	47	G	57	W	67	g	77	W
28	(	38	8	48	Н	58	Х	68	h	78	х
29	)	39	9	49	I	59	Υ	69	i	79	у
2A	*	3A	:	4A	J	5A	Z	6A	j	7A	z
2B	+	3B	:	4B	K	5B	[	6B	k	7B	{
2C	,	3C	<	4C	L	5C	\	6C	1	7C	
2D	-	3D	=	4D	М	5D	]	6D	m	7D	}
2E		3E	>	4E	N	5E	^	6E	n	7E	~
2F	/	3F	?	4F	0	5F	_	6F	0		



## **Function Calls**



- Caller: calling function (in this case, main)
- Callee: called function (in this case, sum)

#### C Code

```
void main()
{
  int y;
  y = sum(42, 7);
  ...
}
int sum(int a, int b)
{
  return (a + b);
}
```



## **Function Conventions**



#### Caller:

- passes arguments to callee
- jumps to callee

#### Callee:

- performs the function
- returns result to caller
- returns to point of call
- must not overwrite registers or memory needed by caller



# MIPS Function Conventions

- KOREA UNIVERSITY 1905
- Call Function: jump and link (jal)
- Return from function: jump register (jr)
- **Arguments**: \$a0 \$a3
- Return value: \$√0



## **Function Calls**



#### C Code

```
int main() {
    simple();
    a = b + c;
}

void simple() {
    return;
}
```

#### MIPS assembly code

```
0x00400200 main: jal simple
0x00400204 add $s0, $s1, $s2
...

0x00401020 simple: jr $ra
```

void means that simple doesn't return a value



## **Function Calls**



#### C Code

```
int main() {
    simple();
    a = b + c;
}

void simple() {
    return;
}
```

#### MIPS assembly code

```
0x00400200 main: jal simple
0x00400204 add $s0, $s1, $s2
...

0x00401020 simple: jr $ra
```

```
jal: jumps to simple $ra = PC + 4 = 0x00400204
```

**jr \$ra**: jumps to address in \$ra (0x00400204)



- MIPS conventions:
- Argument values: \$a0 \$a3
- Return value: \$√0



#### C Code

```
int main()
 int y;
  y = diffofsums(2, 3, 4, 5); // 4 arguments
int diffofsums (int f, int g, int h, int i)
  int result;
  result = (f + g) - (h + i);
                               // return value
  return result;
```



```
MIPS assembly code
# $s0 = y
main:
  addi $a0, $0, 2  # argument 0 = 2
  addi $a1, $0, 3  # argument 1 = 3
  addi $a2, $0, 4  # argument 2 = 4
  addi $a3, $0, 5  # argument 3 = 5
  jal diffofsums # call Function
  add $s0, $v0, $0 # y = returned value
  . . .
# $s0 = result
diffofsums:
  add $t0, $a0, $a1 # <math>$t0 = f + g
  add $t1, $a2, $a3 # <math>$t1 = h + i
  sub $s0, $t0, $t1 # result = (f + g) - (h + i)
  add $v0, $s0, $0  # put return value in $v0
                     # return to caller
  jr $ra
```



#### MIPS assembly code

```
# $s0 = result
diffofsums:
  add $t0, $a0, $a1  # $t0 = f + g
  add $t1, $a2, $a3  # $t1 = h + i
  sub $s0, $t0, $t1  # result = (f + g) - (h + i)
  add $v0, $s0, $0  # put return value in $v0
  jr $ra  # return to caller
```

- diffofsums overwrote 3 registers: \$t0, \$t1, \$s0
- diffofsums can use stack to temporarily store registers

### The Stack



- Memory used to temporarily save variables
- Like stack of dishes, last-infirst-out (LIFO) queue
- Expands: uses more memory when more space needed
- Contracts: uses less memory when the space is no longer needed





### The Stack



- Grows down (from higher to lower memory addresses)
- Stack pointer: \$sp points to top of the stack

Address	Data		Address	Data	
7FFFFFC	12345678	\$sp	7FFFFFC	12345678	1/6
7FFFFF8	120 10070	Ψορ	7FFFFF8	AABBCCDD	War.
7FFFFF4			7FFFFFF4	11223344	<b>←</b> \$sp
7FFFFF0			7FFFFF0		
					160
· // · // //			137	2 1910	

# How Functions use the Stack

- Called functions must have no unintended side effects
- But diffofsums overwrites 3 registers: \$t0, \$t1, \$s0

```
# MIPS assembly
# $s0 = result
diffofsums:
   add $t0, $a0, $a1  # $t0 = f + g
   add $t1, $a2, $a3  # $t1 = h + i
   sub $s0, $t0, $t1  # result = (f + g) - (h + i)
   add $v0, $s0, $0  # put return value in $v0
   jr $ra  # return to caller
```

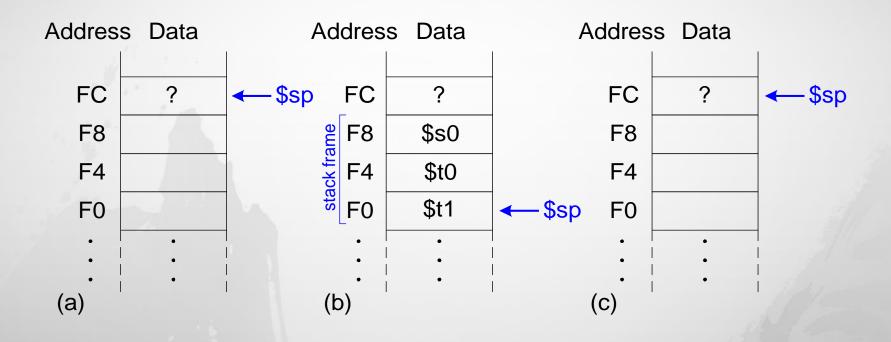


# Storing Register Values on the Stack

```
# $s0 = result
diffofsums:
 addi $sp, $sp, -12 # make space on stack
                    # to store 3 registers
 sw $s0, 8($sp) # save $s0 on stack
 sw $t0, 4($sp) # save $t0 on stack
 sw $t1, 0($sp) # save $t1 on stack
 add $t0, $a0, $a1 # $t0 = f + g
 add $t1, $a2, $a3 # $t1 = h + i
     $s0, $t0, $t1 # result = (f + g) - (h + i)
 sub
 add $v0, $s0, $0 # put return value in $v0
 lw $t1, 0($sp) # restore $t1 from stack
 lw $t0, 4($sp) # restore $t0 from stack
 lw $s0, 8($sp) # restore $s0 from stack
 addi $sp, $sp, 12 # deallocate stack space
                    # return to caller
 jr $ra
```



# The stack during diffofsums Cal









Preserved	Nonpreserved			
Callee-Saved	Caller-Saved			
\$s0-\$s7	\$t0-\$t9			
\$ra	\$a0-\$a3			
\$sp	\$v0-\$v1			
stack above \$sp	stack below \$sp			







#### Fill the blanks

main:

```
addi $a0, $0, 1
 addi $a1, $0, 2
 jal func
 add $s0, $v0, $0
func:
 or $t0, $a0, $a1
 addi $s0, $t0, 4
 add $v0, $t0, $s0
 jr
       $ra
```



## Multiple Function Calls



```
proc1:
  addi $sp, $sp, -4  # make space on stack
  sw $ra, 0($sp)  # save $ra on stack
  jal proc2
  ...
  lw $ra, 0($sp)  # restore $s0 from stack
  addi $sp, $sp, 4  # deallocate stack space
  jr $ra  # return to caller
```







#### Fill the blanks

```
main:
    addi $a0, $0, 1
    addi $a1, $0, 2
    jal func
    add $s0, $v0, $0
    ...
```

```
func:
       $t0, $a0, $a1
 or
 addi $s0, $t0, 4
 jal func2
 and $s1, $0, $v0
 add $v0, $v0, $s1
 jr $ra
func2:
 addi $t0, $0, 0
 addi $v0, $t0, 4
 jr $ra
```



## Recursive Function Call



#### **High-level code**

```
int factorial(int n) {
  if (n <= 1)
    return 1;
  else
    return (n * factorial(n-1));
}</pre>
```



## Recursive Function Call



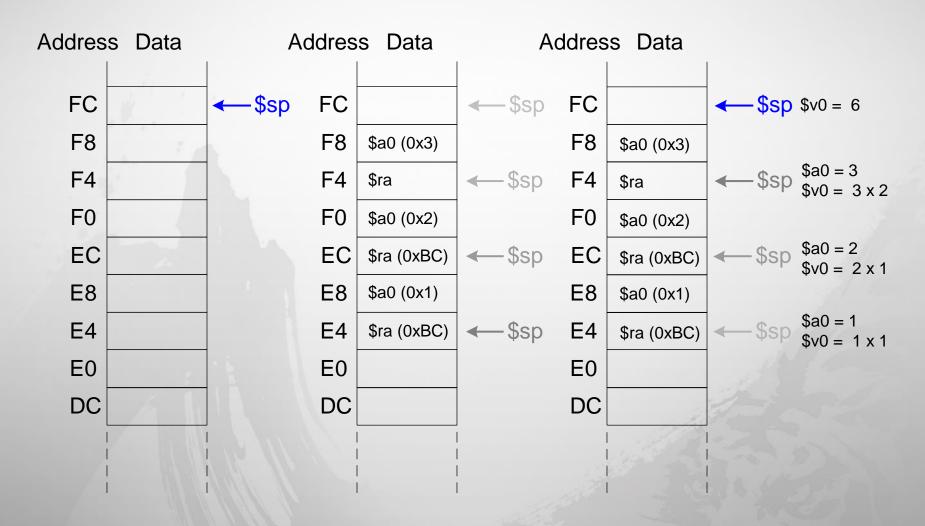
#### MIPS assembly code

```
0x90 factorial: addi $sp, $sp, -8 # make room
              sw $a0, 4($sp) # store $a0
0x94
              sw $ra, 0($sp) # store $ra
0x98
0x9C
              addi $t0, $0, 2
0xA0
              slt $t0, $a0, $t0 # a <= 1 ?
0xA4
              beg $t0, $0, else # no: go to else
0xA8
              addi $v0, $0, 1  # yes: return 1
              addi $sp, $sp, 8 # restore $sp
0xAC
              jr $ra # return
0xB0
         else: addi $a0, $a0, -1 # n = n - 1
0xB4
              jal factorial # recursive call
0xB8
              lw $ra, 0($sp) # restore $ra
0xBC
0xC0
              lw $a0, 4($sp) # restore $a0
              addi $sp, $sp, 8 # restore $sp
0xC4
              mul $v0, $a0, $v0 # n * factorial(n-1)
0xC8
0xCC
              jr $ra
                          # return
```



# Stack During Recursive Call







## Function Call Summary



#### Caller

- Put arguments in \$a0-\$a3
- Save any needed registers (\$ra, maybe \$t0-t9)
- jal callee
- Restore registers
- Look for result in \$v0

#### Callee

- Save registers that might be disturbed (\$s0-\$s7)
- Perform function
- Put result in \$v0
- Restore registers
- jr \$ra



# Addressing Modes



## How do we address the operands?

- Register Only
- Immediate
- Base Addressing
- PC-Relative
- Pseudo Direct



# Addressing Modes



### **Register Only**

- Operands found in registers
  - Example: add \$s0, \$t2, \$t3
  - Example: sub \$t8, \$s1, \$0

#### **Immediate**

- 16-bit immediate used as an operand
  - **Example:** addi \$s4, \$t5, -73
  - Example: ori \$t3, \$t7, 0xFF



# Addressing Modes



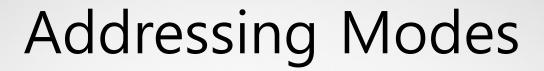
### **Base Addressing**

Address of operand is:

base address + sign-extended immediate

- Example: lw \$s4, 72(\$0)
  - address = \$0 + 72
- Example: sw \$t2, -25(\$t1)
  - address = \$t1 25







#### **PC-Relative Addressing**

#### **Assembly Code**

#### Field Values

beq	\$t0,	\$0,	else
(beq	\$t0,	\$0,	3)

op	rs	rt	ımm		200
4	8	0		3	
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits



## Addressing Modes



#### **Pseudo-direct Addressing**

 $0 \times 0040005C$ 

jal

sum

**0x004000A0** sum: add

\$v0, \$a0, \$a1

JTA 0000 0000 0100 0000 0000 0000 1010 0000 (0x004000A0)

26-bit addr 0000 0000 0100 0000 0000 0000 1010 0000 (0x0100028)

Field Values

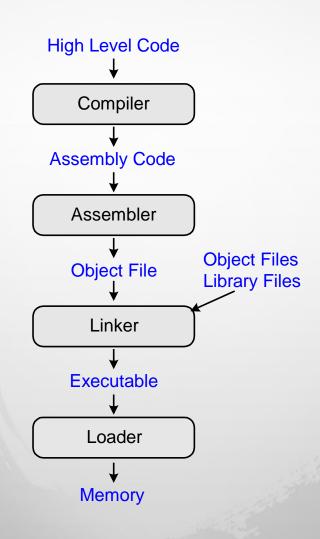
**Machine Code** 

ор	imm		
3	/	0x0100028	
6 bits	26 bits		

ор	addr	
000011	00 0001 0000 0000 0000 0010 1000	(0x0C100028)
6 bits	26 bits	



## How to Compile & Run a Program





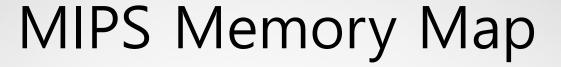
## What is Stored in Memory?

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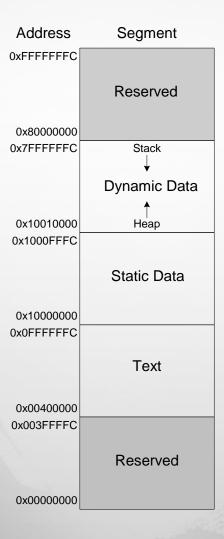
- Instructions (also called text)
- Data
  - Global/static: allocated before program begins
  - Dynamic: allocated within program

- How big is memory?
  - At most  $2^{32}$  = 4 gigabytes (4 GB)
  - From address 0x00000000 to 0xFFFFFFFF











## Example Program: C Code

```
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```

```
int f, g, y; // global
int main(void)
 f = 2;
 q = 3;
 y = sum(f, g);
 return y;
int sum(int a, int b) {
 return (a + b);
```



## Example Program: MIPS Assembly

```
int f, g, y; // global
int main (void)
 f = 2;
 q = 3;
 y = sum(f, g);
  return y;
int sum(int a, int b) {
  return (a + b);
```

```
.data
f:
g:
у:
.text
main:
 addi $sp, $sp, -4 # stack frame
 sw $ra, 0($sp) # store $ra
 addi $a0, $0, 2 # $a0 = 2
 sw $a0, f # f = 2
 addi $a1, $0, 3  # $a1 = 3
 sw $a1, g # g = 3
 jal sum # call sum
 sw $v0, y # y = sum()
 lw $ra, 0($sp) # restore $ra
 addi $sp, $sp, 4 # restore $sp
                 # return to OS
 jr $ra
sum:
 add $v0, $a0, $a1 # $v0 = a + b
     $ra # return
 jr
```



# Example Program: Symbol Table

Symbol	Address
f	0x10000000
g	0x10000004
У	0x10000008
main	0x00400000
sum	0x0040002C



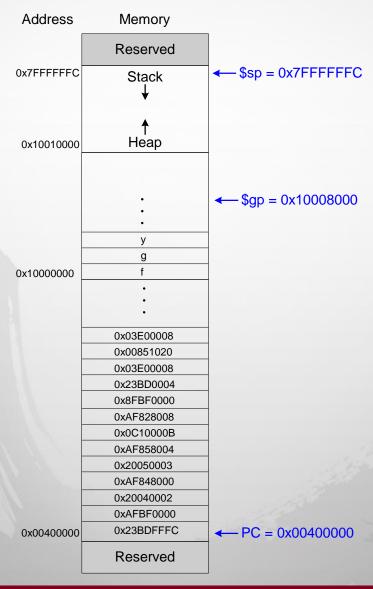
# Example Program: Executable

Executable file header	Text Size	Data Size	
	0x34 (52 bytes)	0xC (12 bytes)	
Text segment	Address	Instruction	
	0x00400000	0x23BDFFFC	addi S
1.0	0x00400004	0xAFBF0000	sw S
	0x00400008	0x20040002	addi \$
	0x0040000C	0xAF848000	sw S
	0x00400010	0x20050003	addi \$
	0x00400014	0xAF858004	sw S
	0x00400018	0x0C10000B	jal (
	0x0040001C	0xAF828008	sw S
	0x00400020	0x8FBF0000	lw S
	0x00400024	0x23BD0004	addi \$
	0x00400028	0x03E00008	jr \$
	0x0040002C	0x00851020	add \$
	0x00400030	0x03E00008	jr \$
Data segment	Address	Data	
	0x10000000	f	136
	0x10000004	g	5 (8)
	0x10000008	У	

addi \$sp, \$sp, -4
sw \$ra, 0 (\$sp)
addi \$a0, \$0, 2
sw \$a0, 0x8000 (\$gp)
addi \$a1, \$0, 3
sw \$a1, 0x8004 (\$gp)
jal 0x0040002C
sw \$v0, 0x8008 (\$gp)
lw \$ra, 0 (\$sp)
addi \$sp, \$sp, -4
jr \$ra
add \$v0, \$a0, \$a1
jr \$ra



# Example Program: In Memory





### Odds & Ends



- Pseudoinstructions
- Exceptions
- Signed and unsigned instructions
- Floating-point instructions



### Pseudoinstructions



Pseudoinstruction	MIPS Instructions
li \$s0, 0x1234AA77	lui \$s0, 0x1234
	ori \$s0, 0xAA77
clear \$t0	add \$t0, \$0, \$0
move \$s1, \$s2	add \$s2, \$s1, \$0
nop	sll \$0, \$0, 0

### Exceptions



- Unscheduled function call to exception handler
- Caused by:
  - Hardware, also called an *interrupt*, e.g., keyboard
  - Software, also called *traps*, e.g., undefined instruction
- When exception occurs, the processor:
  - Records the cause of the exception
  - Jumps to exception handler (at instruction address 0x80000180)
  - Returns to program



### **Exception Registers**



- Not part of register file
  - Cause: Records cause of exception
  - EPC (Exception PC): Records PC where exception occurred
- EPC and Cause: part of Coprocessor 0
- Move from Coprocessor 0
  - -mfc0 \$t0, EPC
  - Moves contents of EPC into \$t0



## **Exception Causes**



Exception	Cause
Hardware Interrupt	0x0000000
System Call	0x00000020
Breakpoint / Divide by 0	0x00000024
Undefined Instruction	0x00000028
Arithmetic Overflow	0x00000030



## **Exception Flow**



- Processor saves cause and exception PC in Cause and EPC
- Processor jumps to exception handler (0x80000180)
- Exception handler:
  - Saves registers on stack
  - Reads Cause register
     mfc0 \$t0, Cause
  - Handles exception
  - Restores registers
  - Returns to program
     mfc0 \$k0, EPC
     jr \$k0



## Signed & Unsigned Instructions

- Addition and subtraction
- Multiplication and division
- Set less than



### Addition & Subtraction



- Signed: add, addi, sub
  - Same operation as unsigned versions
  - But processor takes exception on overflow
- Unsigned: addu, addiu, subu
  - Doesn't take exception on overflow

Note: addiu sign-extends the immediate



## Multiplication & Division



- Signed: mult, div
- Unsigned: multu, divu



### Set Less Than



- Signed: slt, slti
- Unsigned: sltu, sltiu

Note: sltiu sign-extends the immediate before comparing it to the register



#### Loads



#### Signed:

- Sign-extends to create 32-bit value to load into register
- Load halfword: 1h
- Load byte: 1b

#### Unsigned:

- Zero-extends to create 32-bit value
- Load halfword unsigned: lhu
- Load byte: 1bu

## Floating-Point Instructions



- Floating-point coprocessor (Coprocessor
   1)
- 32 32-bit floating-point registers (\$f0-\$f31)
- Double-precision values held in two floating point registers
  - e.g., \$f0 and \$f1, \$f2 and \$f3, etc.
  - Double-precision floating point registers: \$f0,
     \$f2, \$f4, etc.



## Floating-Point Instructions



Name	Register Number	Usage
\$fv0 - \$fv1	0, 2	return values
\$ft0 - \$ft3	4, 6, 8, 10	temporary variables
\$fa0 - \$fa1	12, 14	Function arguments
\$ft4 - \$ft8	16, 18	temporary variables
\$fs0 - \$fs5	20, 22, 24, 26, 28, 30	saved variables



## F-Type Instruction Format



- Opcode =  $17 (010001_2)$
- Single-precision:
  - $cop = 16 (010000_2)$
  - add.s, sub.s, div.s, neg.s, abs.s, etc.
- Double-precision:
  - $cop = 17 (010001_2)$
  - add.d, sub.d, div.d, neg.d, abs.d, etc.
- 3 register operands:
  - fs, ft: source operands
  - fd: destination operands

#### F-Type

op	cop	ft	fs	fd	funct
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

## Floating-Point Branches



- Set/clear condition flag: fpcond
  - Equality: c.seq.s, c.seq.d
  - Less than: c.lt.s, c.lt.d
  - Less than or equal: c.le.s, c.le.d
- Conditional branch
  - bclf: branches if fpcond is FALSE
  - bclt: branches if fpcond is TRUE
- Loads and stores
  - lwc1: lwc1 \$ft1, 42(\$s1)
  - swc1: swc1 \$fs2, 17(\$sp)