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ABSTRACT

We present characterization of a lock-in amplifier based on a field programmable gate array capable of demodulation at up to 50 MHz. The system exhibits 90 nV/$\sqrt{}$Hz of input noise at an optimum demodulation frequency of 500 kHz. The passband has a full-width half-maximum of 2.6 kHz for modulation frequencies above 100 kHz. Our code is open source and operates on a commercially available platform.

I. INTRODUCTION

The lock-in amplifier (LIA) is an invaluable tool in scientific instrumentation[1] allowing the extraction of weak signals from noisy backgrounds, even where the amplitude of the noise is much greater than the signal.[2] First described in 1941, early LIAs were based on heaters, thermocouples, and transformers.[3] More modern LIAs have been fully digital[4–7] or implemented on field programmable gate array (FPGA) devices,[8–14] which are able to exceed the performance of their analog counterparts.[15] However, the cost of modern LIAs may prove prohibitive, particularly in cases where large numbers of input channels are required. By employing Red Pitaya hardware, we are able to define an open-source LIA solution that is comparable with considerably more costly approaches.

Characterized by a wide dynamic range and the ability to extract signal from noisy environments,[16] LIAs are phase sensitive detectors[17] due to their operating principles. A reference signal in the form of a sinusoidal wave is generated either internally by the LIA itself, along with a cosinusoidal wave, or externally by some other sources that can also be manipulated to form a cosinusoidal reference. This reference is multiplied by the input signal[18] that carries the desired data modulated at the reference frequency.[19] A low pass filter is then used before outputting the signal. In this way, the LIA amplifies and outputs the component of the input signal that is at the reference frequency, attenuating noise at other frequencies.[20] Components out of phase with the sine reference will also be attenuated due to orthogonality of the sine and cosine functions of equal frequency,[21] and hence, the LIA is considered phase sensitive.[22] Components in phase with the sine function will result in a nonzero value in the X output, while those in phase with the cosine function will produce a nonzero value in the Y output. X and Y can be combined by $R = \sqrt{X^2 + Y^2}$ to provide a magnitude value,[23] while phase $\phi = \arctan \frac{Y}{X}$.

FPGAs offer easily implementable microcircuitry design via the use of hardware description language (HDL) such as Verilog or VHDL. A broad range of applications can be realized using these devices,[24] including LIAs without recourse to detailed knowledge of microelectronics.[25]

The Red Pitaya STEMlab 125-14 is a single board computer (SBC) with an integrated FPGA in the form of a Xilinx Zynq 7010 SoC,[26] allowing for the implementation of reprogrammable microarchitecture that would otherwise necessitate dedicated hardware. The reprogrammability[27] of this FPGA makes it applicable for the LIA functionality described here and allows for further expansion and modification by end users. Two DC coupled analog inputs are available in the form of user selectable ±1 V or ±20 V, 125 MS/s analog-to-digital converters (ADCs—Linear Technologies LTC2145CUP-14[28]) with an input impedance/capacitance of 1 MΩ/10 pF.

In this article, we detail an LIA which we have implemented on the STEMlab's FPGA chip, along with open source[29] operational and data transfer software developed specifically for this application.

We demonstrate that this device shares many capabilities with more expensive alternatives such as a sweepable internal signal generator, single or dual input/output modes, wave form control, and the ability to increase the number of available inputs and outputs by interfacing across multiple STEMlab units.

Comparison is made with the Zurich Instruments HF2LI LIA, which is specified for operation up to 50 MHz demodulation frequency.[30] While an extensive software application is provided with the HF2LI, the open source nature and readily available software and hardware of the LIA presented here allow for an attractive option where cost is a consideration. Research into low-cost FPGA based LIAs has produced a number of alternatives,[25] including high resolution designs operating at up to 6 MHz demodulation,[31,32] and simulations have been presented for a high frequency LIA based on the Red Pitaya STEMlab.[33] Typically, FPGA LIAs have been developed with specific experimental objectives.[13,14,34] The STEMlab is the basis for a range of related measurement instrumentation from PyRPL, including an LIA.[35–37] A low cost FPGA-based LIA has also been developed which operates at a low demodulation frequency,[38] and FPGA-based LIAs have been compared with analog devices in terms of signal accuracy.[39] However, we believe that this article is the first to characterize a high frequency, open source LIA. The open source code may lead to a range of future uses in research, education, and industry.

II. METHODS

A. Hardware and software

The FPGA system design and implementation was performed using software provided by the manufacturer of the FPGA, Xilinx. A simplified version of the design circuitry block diagram can be seen in Fig. 1. Signals received by the ADCs are passed to the processing blocks where they are multiplied by the reference signal [which is generated internally by direct digital synthesis (DDS)] and filtered using a single pole infinite impulse response (IIR) filter. The resulting output is written to the SBC's random access memory (RAM) via the FPGA's memory interface block. This data is then written to a ramdisk file also contained within the STEMlab's RAM, alleviating high read/write workloads which were observed to cause critical failures of the SD card. The data are also passed to the on-board digital-to-analog converters (DACs) along with the reference signal that is used to modulate the desired signal. This reference can be extracted via the DAC output for external use.

Data retrieval from the STEMlab to a host computer can be achieved via the DACs that are provided with SubMiniature version A (SMA) connections for output to an oscilloscope. These DACs have 14-bit resolution combined with 125 MS/s data rate. Non-offset, digital amplification of up to 2000 times the raw output is available. However, noise introduced by the DACs makes the output undesirable in cases where small changes in signal intensity are to be detected. Alternatively, data may be transferred to a host personal computer (PC) via file transfer from the STEMlab's RAM. This produces low noise data but can only be performed on the entirety of the LIA's allocated storage space of approximately 65 megabytes (MB). While this process may last for tens of seconds, all data (X, Y, R, and ϕ) for both output channels are received simultaneously. Further limitations include the inability to operate using an external lock-in reference, cross talk that can occur between the two input channels and no facility for subtraction of channels (e.g., A-B). Due to the programmable nature of the STEMlab, end users are able to implement their own data transfer methods, which may be shown to alleviate some or all of these limitations.

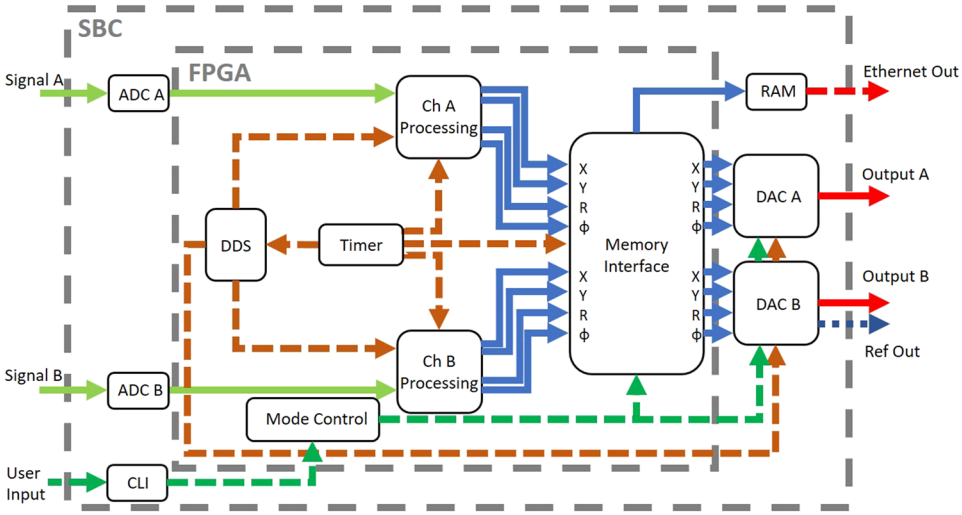

FIG. 1. Simplified schematic of the circuitry layout on the Red Pitaya lock-in amplifier FPGA. Signals (solid green arrows) are received at channel processing, where they are multiplied by a reference signal generated in the direct digital synthesis (DDS) block, which takes time data (dashed brown arrows) from the timer and distributes it as a reference. After multiplication, data are passed through a single pole infinite impulse response (IIR) filter, currently limited to single order. Filtered data (solid blue arrows) are then passed to the memory allocation block and subsequently to the digital to analog converters (DACs) and are converted to analog data (solid red arrows) and passed out to the user or saved to the SBC RAM where they can be accessed via Ethernet (dashed red arrow). The reference signal is extracted from the DACs in analog form (dashed blue arrow). Operating parameters and modes are set by the user (dashed green arrows) via the command line interface (CLI) that communicates with the mode control block on the FPGA.

While the FPGA is responsible for signal processing and data transfer, parameter setting takes place on the STEMlab's Linux SBC. This device is packaged along with the FPGA on the STEMlab board, allowing the user to operate the Red Pitaya LIA (RePLIA) or any other custom FPGA application entirely using the STEMlab itself. Parameter setting and system control are performed using C and Python codes written specifically for use with the LIA. These codes may be accessed via secure shell (SSH) or a terminal emulator but, in practice, are accessed via a Java-based graphical user interface (GUI) on a client computer that allows the user to largely ignore the STEMlab's Linux element. This open-source GUI allows for the setting of all available RePLIA parameters.

B. Characterization methodology

Data were extracted from both LIAs via Ethernet connection. In the case of the RePLIA aboard the STEMlab, this avoided noise from its DACs which were found to increase noise by up to three orders of magnitude.

Noise for both LIAs during operation was measured at various demodulation frequencies with no input signal present and with a constant amplitude signal produced with an Agilent N5172B EXG vector signal generator. Similarly, noise was measured while varying the time constant of the LIAs with the demodulation frequency fixed at the value determined to be the least noisy by the previous method. As with the input noise, these data are presented after a fast Fourier transform (FFT).

Passbands for each LIA at various demodulation frequencies were obtained by applying a constant amplitude signal at the specified demodulation frequency. This signal was then combined with a sweep between the minimum and maximum frequencies passing through the demodulation frequency, with a sweep time of 10 s.

1. Zurich instruments HF2LI

The HF2LI provides a built in input noise measurement protocol. The experimental conditions detailed in the HF2LI user notes were replicated,[30] and the input noise was measured. Noise was collected while the inputs were terminated for periods of 1, 10, and 100 s. This noise was then subjected to a FFT, and the noise level was assessed and compared with the manufacturer's stated input noise level of 5 nV/$\sqrt{\text{Hz}}$ at 1 MHz demodulation for the output frequencies greater than 10 kHz.[40]

2. Red Pitaya lock-in amplifier

Optimal operational parameters were deduced by examining the output of the RePLIA at varying demodulation frequencies and time constants. The optima chosen were those which resulted in the lowest output noise level. This behavior was examined both with an applied signal and with the terminated inputs. The RePLIA maintains capability over a wide range of demodulation frequencies (10 kHz–50 MHz), which were also characterized, but figures are quoted with respect to optimal parameters unless otherwise stated.

III. RESULTS

Figure 2 shows input noise spectral density for both LIAs at 1 s, 10 s, and 100 s collection periods. Increasing collection time t was expected to produce a $\sqrt{t}$ decrease in noise. Both LIAs remained within close agreement of this prediction after a 100 s collection time [Fig. 2(c)]. Noise levels were obtained by taking an average of baselined data from each LIA at the relevant collection time. In Fig. 2(a), the data for 1 s of collection time has been zero padded, by adding 4 s worth of zeros, to reduce the width of the frequency bins. These averages produce figures of 89, 21, and 6 nV for the RePLIA for the collection times of 1, 10, and 100 s, respectively, corresponding to the

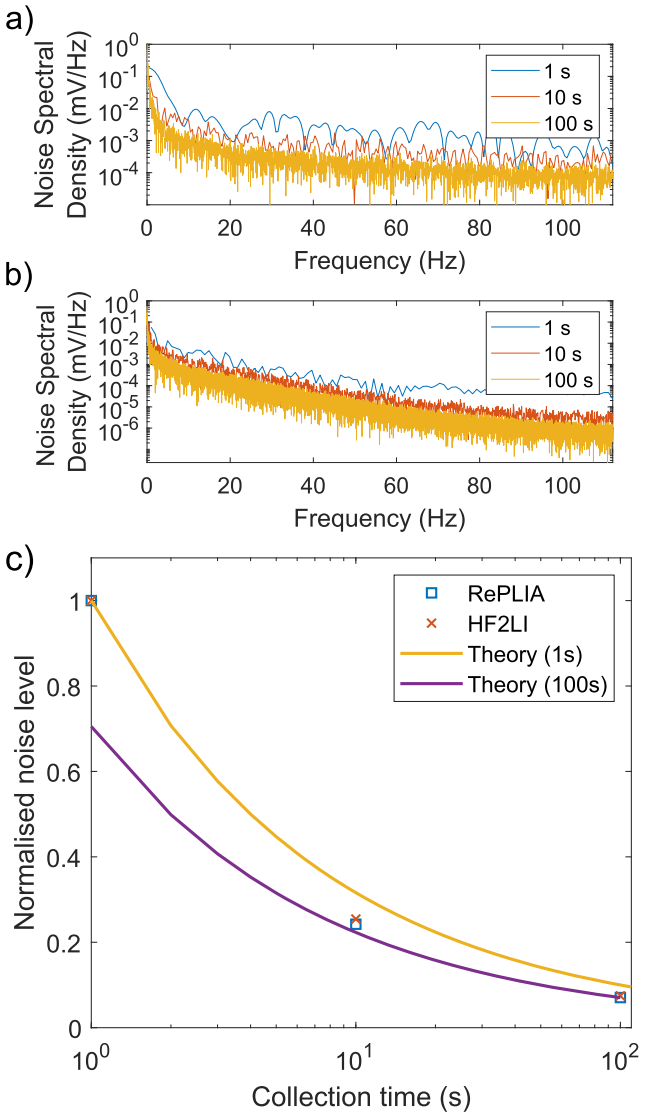

FIG. 2. Noise spectral density from (a) RePLIA at 500 kHz demodulation with a 1 ms time constant (with 1 s data zero padded) and (b) HF2LI at 1 MHz demodulation and 700 μs time constant at 1 s, 10 s, and 100 s collection times (output data are R for both channels). (c) Noise level decays with an increased collection time close to the predicted $\sqrt{t}$ relationship (top trace) calculated based on the noise measured after 1 s of collection. The lower trace indicates theoretical values back calculated from the 100 s data point.

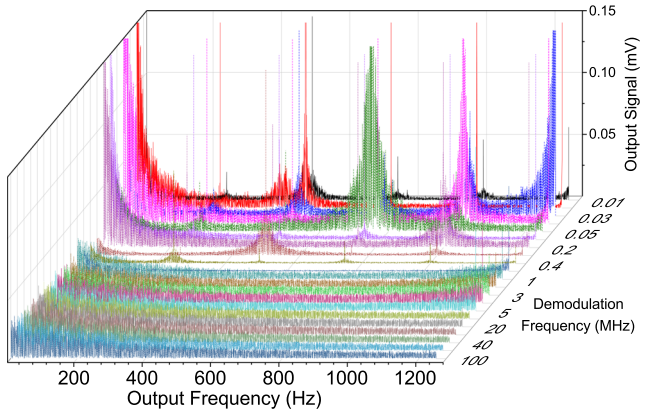

FIG. 3. FFTs of terminated input data, extracted via file transfer, at various RePLIA demodulation frequencies with 100 s collection time. Two distinct noise regimes seem to exist, with demodulation frequencies above 100 kHz producing significantly lower noise. Time constants were varied depending on the demodulation frequency (see Appendixes A and B). Note that low frequency and high intensity data have been cropped for visual clarity.

sensitivities of 89, 66, and 60 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$. When the RePLIA was operated using the conditions stipulated for measurement of the HF2LI input noise, the noise levels are 131, 133, and 130 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$. This shows that the optimal operating parameters for the HF2LI differ from those appropriate to the RePLIA. It should be noted that the manufacturer specified sampling rate for the HF2LI limits the span of the FFT output to 120 Hz. Frequencies beyond this limit can be found in the HF2LI's user manual in section 8.4 on page 665.[30] A wider output frequency plot for the RePLIA can be found in Appendixes A and B (Fig. 13).

The noise spectrum for the HF2LI [Fig. 2(b)] shows greater noise below 80 Hz and lower noise at higher output frequencies. By contrast, the RePLIA shows a higher level of noise that is largely steady up to 120 Hz [Fig. 2(a)] output frequency.

Figure 3 shows FFTs of the RePLIA output collected for 100 s at a range of demodulation frequencies, with time constants optimized for the relevant demodulation period (see Appendixes A and B). There is a marked difference in noise at demodulation frequencies below 100 kHz, although above this threshold the noise is roughly constant.

Output from the RePLIA digital-to-analog converters (DACs) was also produced (see Appendixes A and B), showing a constant noise level at frequencies below 100 kHz. Although this noise level is several orders of magnitude greater than that incurred in data extracted via the Ethernet connection, this may be an acceptable trade-off in certain cases. This consistency suggests that noise inherent to the DACs is the limiting factor when obtaining data using this method, although this noise can be reduced as described in Ref. 28. Signal-to-noise as measured at the DACs increases with an increase in the DAC multipliers, plateauing toward saturation of the RePLIA's outputs (see Fig. 7 in Appendixes A and B).

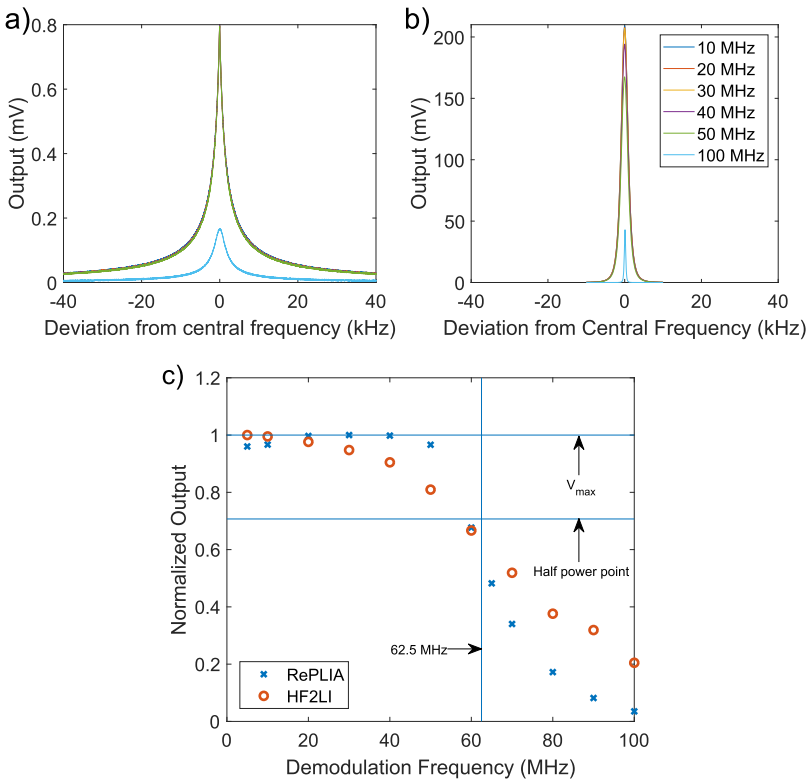

FIG. 4. Output of the frequency sweep for MHz demodulation frequencies for the (a) RePLIA and (b) HF2LI. (c) Maximum output voltage of the RePLIA plotted against the demodulation frequency, showing the half power point. Note that the RePLIA has a sampling rate of 125 MHz.

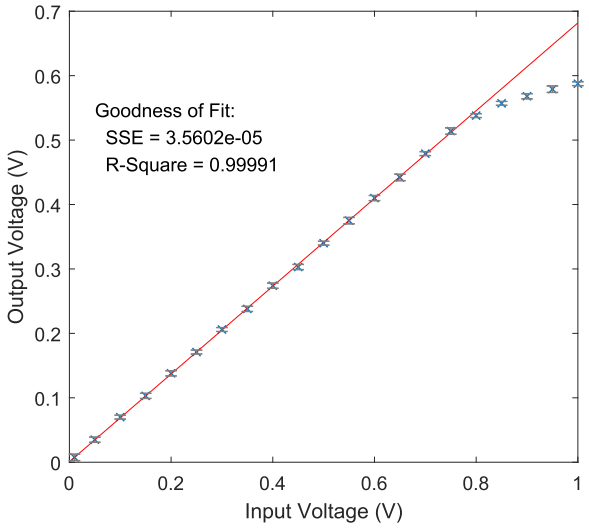

FIG. 5. Demodulated RePLIA output against the input voltage, operating at 500 kHz demodulation for a ±1 V input range. Solid red line is a linear fit of the 0–0.7 V linear region.

Figures 4(a) and 4(b) show the shape of LIA passbands when modulating at varying frequencies with time constants optimized for each frequency. The HF2LI demonstrates a narrower passband with less transmission at unwanted frequencies. These passbands are shown to be approximately Lorentzian in line shape with a full-width half-maxima of 2.6 kHz for demodulation frequencies above 100 kHz (see Appendixes A and B), and they begin to reduce in intensity above 30 MHz demodulation with the HF2LI, whereas the output is consistent up to 50 MHz demodulation with the RePLIA. Figure 5(c) shows the normalized output at megahertz demodulation frequencies for both LIAs. The half power point is indicated ($\frac{V_{max}}{\sqrt{2}}$, where V_{max} is the peak voltage output), which for the RePLIA is encountered at a demodulation frequency of around 60 MHz, which is close to half of the device's 125 MHz sample rate, as can be expected from the Nyquist sampling theorem.[41]

Linearity of the output relative to the input is demonstrated in Fig. 5. Input voltages were varied, and the resultant DAC output voltage were measured for both the ±1 V and ±20 V input ranges. Linearity is observed over ±700 mV and ±1100 mV, respectively. Outside these regions, the STEMlab's input, having only 14 bits, introduces significant nonlinearities, as does the improper impedance matching of the RePLIA's inputs.

IV. CONCLUSIONS

The RePLIA performs lock-in amplification at frequencies up to 50 MHz, with an input noise level of 90 nV/$\sqrt{}$Hz. The respective figures from the Zurich Instruments HF2LI (50 MHz demodulation with 5 nV/$\sqrt{}$Hz input noise) show that the FPGA LIA detailed in this article is an open source alternative.

ACKNOWLEDGMENTS

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APPENDIX A: OPERATIONAL NOTES

The RePLIA was operated in a dual channel input mode with the output producing amplitude data. These data were collected at a rate of 20 ksamples/s. It is important to note that in setting a sample rate, the actual rate per sample will be $^1/_8$ of that set, as the set rate includes one sample per output channel per time increment (2 input channels comprising R, X, Y, and ϕ for each input channel). This sample rate is dependent on both the system being measured and the hardware over which data are transmitted but can be set by the user to any rate within the sample rate range of

TABLE I. Experimental parameters used for the measurement of HF2LI input noise, as detailed in manufacturer's instructions.

HF2LI input noise settings		
Setting	Parameter	Value
Signal input	Range	10 mV
	AC	On
	Diff	Off
	50 Ω	On
Demodulator low-pass filter	Bandwidth 3 dB	100 Hz
	Order	4
Oscillator	Frequency	1 MHz
Signal output	Switch	Off

TABLE II. Time constants τ for RePLIA at various demodulation frequencies. The central column contains the minimum usable time constant and the right-hand column details the actual time constants used which were determined by ensuring a near-Lorentzian passband at the relevant demodulation frequency. Note that this table is not exhaustive and longer/shorter time constants may be used.

Time constants (τ)		
F_{mod} (MHz)	τ_{min} (ms)	τ (ms)
0.001	10	100
0.01	1	100
0.1	0.1	10
0.5	2×10^{-2}	1
1	1×10^{-2}	1
10	1×10^{-3}	1
100	1×10^{-4}	0.1

the STEMlab, although this sample rate may ultimately affect the accuracy of resultant signals. When obtaining data via the DAC outputs, collection has been performed by a Pico Technology Picoscope 4424 digital oscilloscope. The Picoscope and DAC outputs were also used when determining the time constants for the RePLIA. Data extracted via the RePLIA's Ethernet port were converted to millivolt values by dividing the actual numerical value by 2.1×10^6, a conversion factor that was determined by comparing the Ethernet values with the corresponding values produced at the DACs with no DAC multiplication applied.

The Zurich Instruments HF2LI was operated according to the instructions laid out in section 3.5 of the HF2 User Manual,[30] using the parameters in Table I.

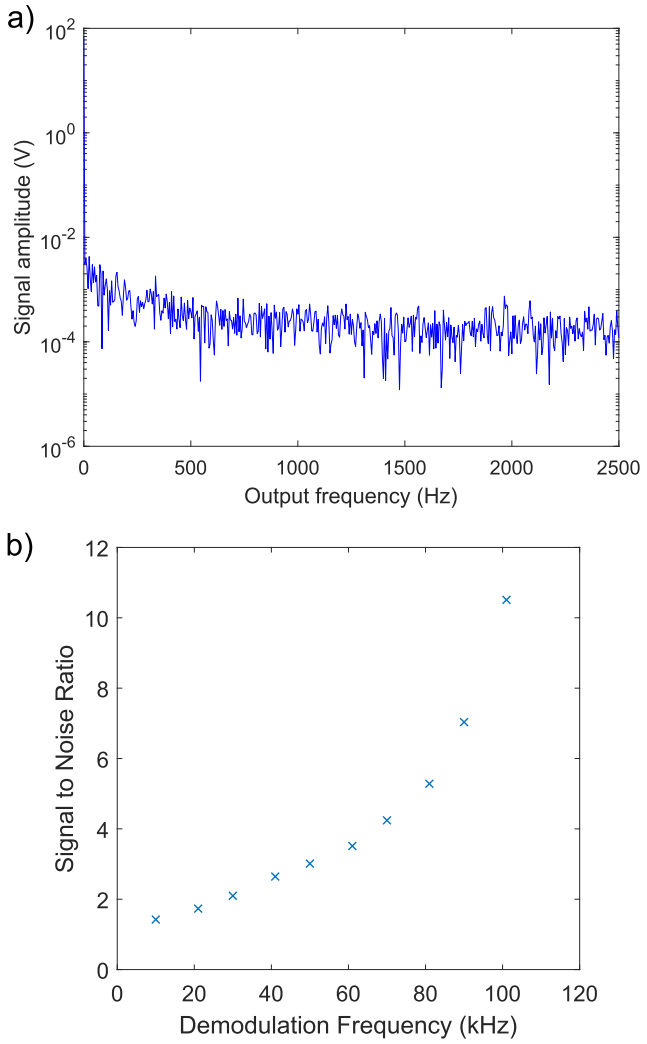

FIG. 6. (a) FFT of 10 kHz demodulation data taken from the RePLIA's DAC outputs, demonstrating significantly greater noise than the data taken from the Ethernet output. (b) Output signal to noise ratio from the DAC outputs improves dramatically with demodulation frequency throughout lower frequency ranges due to the increased signal.

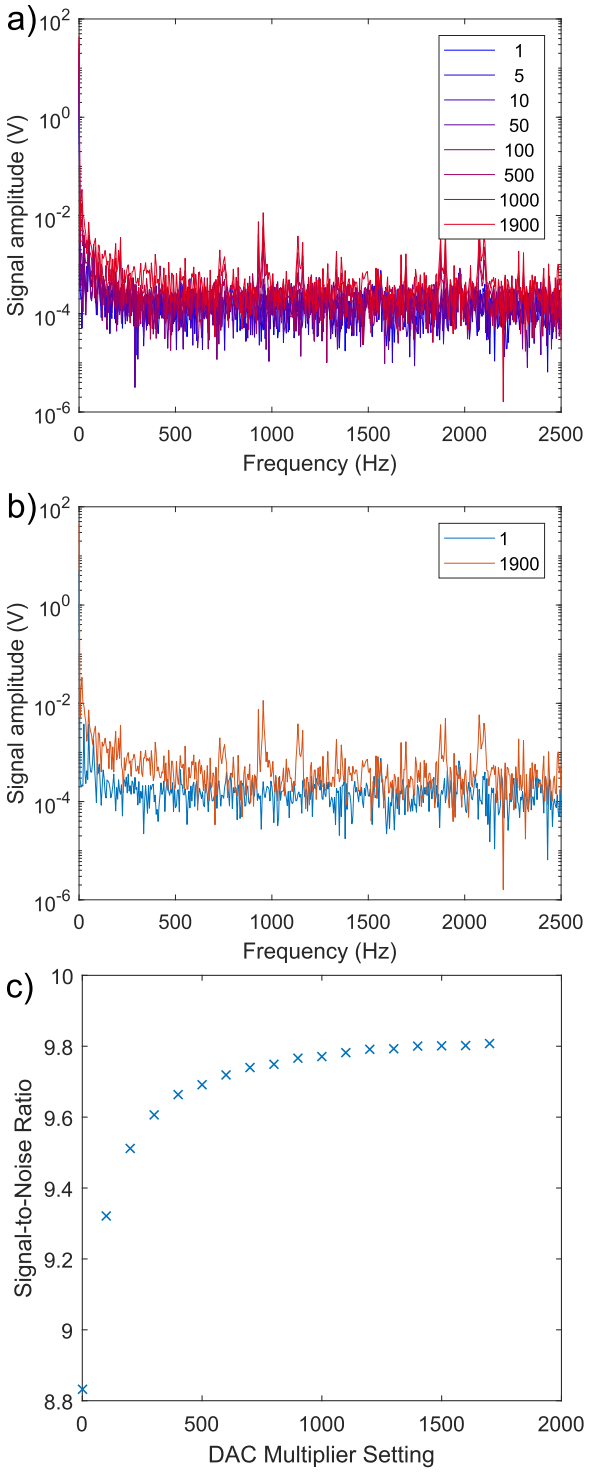

FIG. 7. FFTs of RePLIA input noise at varying DAC multiplier settings (a) with extremes only plotted for clarity (b). (c) The signal to noise ratio at the RePLIA's digital-to-analog outputs increases with a larger DAC multiplier. However, even small signals can lead to saturation of these outputs. Data are obtained at 500 kHz demodulation frequency and a 10 ms time constant.

The time constants detailed in Table II were used for measurements made with the RePLIA. For frequencies in between those listed, the time constant corresponding to the lower frequency was used. Minimum time constants τ_{min} have been determined by $\tau_{min} = 10/f_{mod}$, where f_{mod} is the demodulation frequency. This ensures that for a given time constant, 10 modulation periods or more elapse during the time constant. The actual time constants used were chosen based on the line shape of passbands as seen in Fig. 5(a) in the main text. Time constants were made as large as possible without distortion of the Lorentzian line shape of these passbands.

Figure 6(a) shows an FFT of the terminated input data at 10 kHz. These data were extracted from the digital-to-analog converters (DACs), with the noise level indicating that the DACs themselves are the most significant source of noise. Contrasting this with Fig. 3, where we see that without DAC noise, the varying demodulation frequency causes a distinct change to noise levels. Figure 7(b) demonstrates an increase in the output signal to noise ratio with increasing demodulation frequency.

Figure 7(a) shows the effect on an FFT while varying the DAC amplification multiplier, with the extremes in this range shown in Fig. 7(b). There is no significant difference in noise level between these extremes. Although Fig. 7(c) shows that an increase in the DAC multiplier does improve the signal-to-noise ratio, care should be taken not to saturate the STEMlab's 1 V maximum output.

Figure 8 demonstrates the effect of the time constant on the shape of the passband for a given demodulation frequency, with 500 kHz used as an example. Excessively long time constants produce a narrower passband at the expense of line shape; fringes

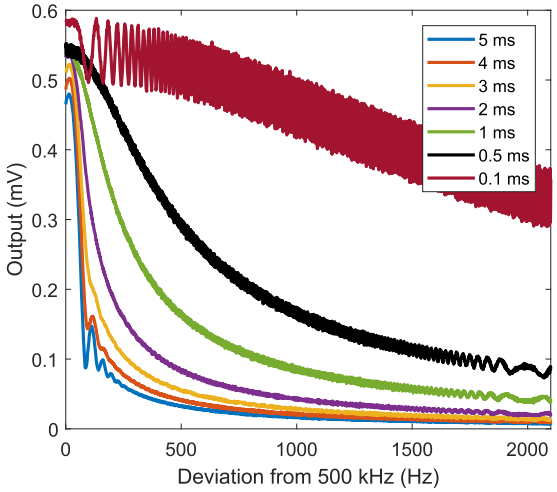

FIG. 8. The effect of the time constant setting on the resulting passband. An 80 kHz sweep over 10 s through the demodulation frequency of 500 kHz at varying time constants results in distortion of the passband. Longer time constants result in fringes in the unwanted frequency regions, and shorter time constants result in excessive acceptance of unwanted frequencies. For 500 kHz, a time constant of 1 ms was chosen as a suitable compromise. The small section of the sweep output shown above shows only the part of the passband affected by the time constant.

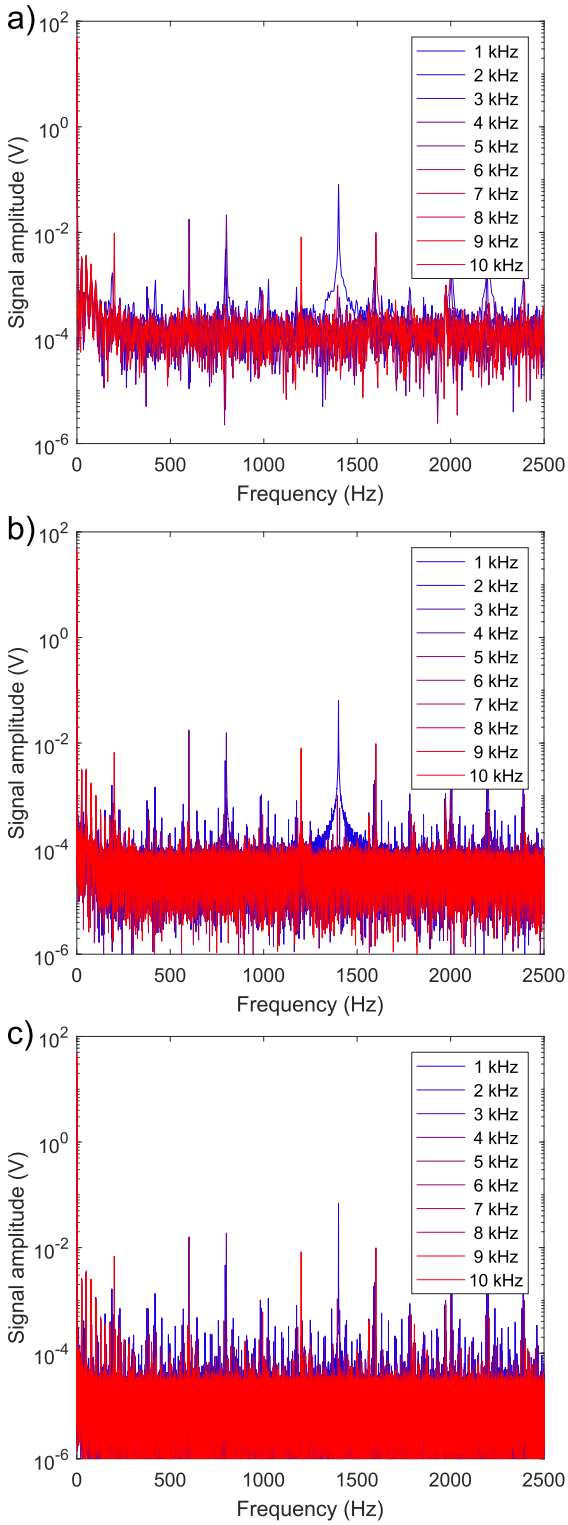

FIG. 9. Low frequency (1–10 kHz) FFTs of RePLIA input noise from (a) 1 s, (b) 10 s, and (c) 100 s of DAC data. Frequency-specific spikes are common at a low demodulation frequency.

appear at output frequencies close to but greater than the demodulation frequency, leading to the distortion of output signals. Shorter time constants produce a more consistent line shape at the cost of passband linewidth. Further to this, extremely short time constants (below those detailed in Table II) are unable to detect changes on time scales appropriate to the demodulation frequency. In terms of software, the time constant can be set to any value above 9×10^{-6} s. However, appropriate setting of the time constant is necessary to ensure the correct representation of output signals, and an understanding of the physical nature of systems being measured is also necessary for accurate results.

Figure 9 shows FFTs of low demodulation frequency data at varying collection times. Certain frequency elements are evident throughout, which are not evident at higher demodulation frequencies. These components are visible in data extracted both via the DACs and via the STEMlab's Ethernet port.

Figure 10 shows the effect of time constant on noise. Although noise decreases with longer time constants, signal distortions as seen in Fig. 8 limit the choice of time constant used.

Figure 11 shows the measured 10 MHz passband of both the RePLIA and HF2LI along with a Lorentzian fit of the data, demonstrating a rough conformation with such a line shape. These data give a full-width half-maximum of 2.6 kHz for the RePLIA and 2 kHz for the HF2LI. Figures 8 and 9 both contain artifacts arising from the single order filter. Increasing the order of the filter may reduce the prominence of these features, although experiments with the HF2LI suggest that such benefits may be marginal.

Higher noise at lower frequencies, as seen in Fig. 3, is consistent with flicker noise of the input stage, as demonstrated in Fig. 12, in that it is of the form of $1/f$.

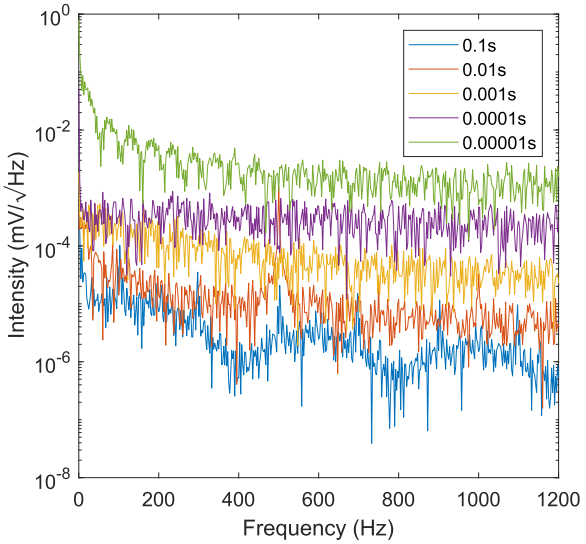

FIG. 10. FFTs of noise at varying time constant at a demodulation frequency of 500 kHz. Note that the 0.00 001 s trace is below the minimum time constant as detailed in Table II.

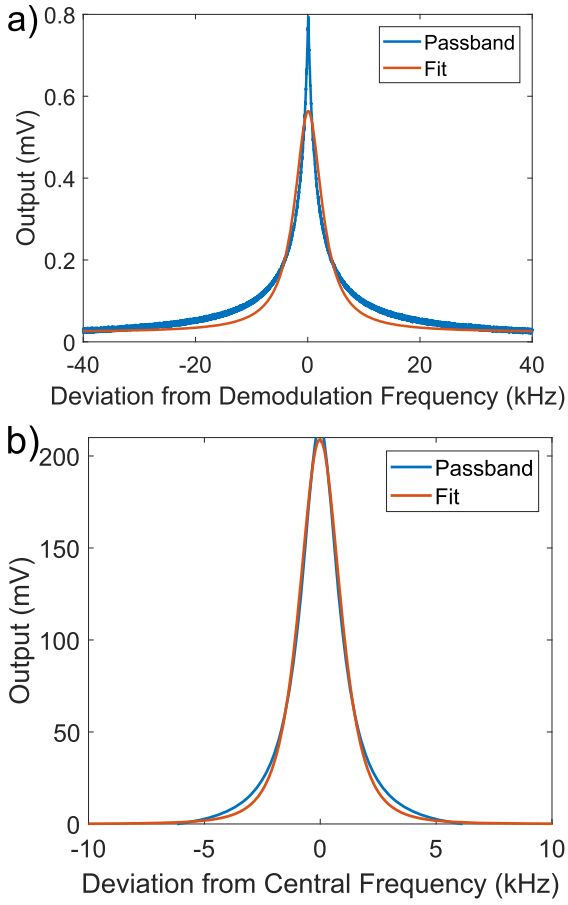

FIG. 11. (a) RePLIA and (b) HF2LI 10 MHz passbands with Lorentzian fits with 2.6 kHz and 2 kHz linewidths, respectively. Note that the x-axes cover different ranges for these data.

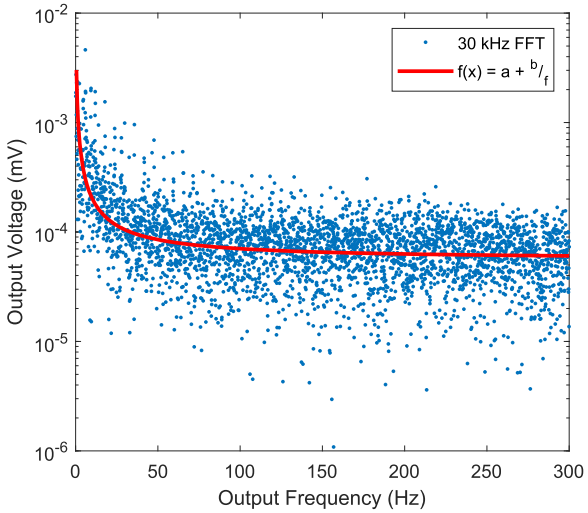

FIG. 12. FFT of the signal demodulated at 30 kHz, with a fit of $f(x) = a + b \cdot 1/f$, where $a = 5.6 \times 10^{-5}$, $b = 0.001$, consistent with flicker noise of the board.

APPENDIX B: HARDWARE AND SOFTWARE NOTES

Largely, the RePLIA is limited by the factors introduced by the STEMlab's hardware and software. The maximum sample rate of the demodulated signal corresponds to the output sample rate of the STEMlab (125 MS/s) when using the DAC outputs. However, this sampling rate is limited instead by the network connection when extracting data via the Ethernet adapter.

Mathematical operations such as $A_{out} = A_{in} - B_{in}$ have not been implemented at the current time, although this is entirely plausible by adding such functionality within the FPGA code.

Power consumption for the RePLIA is 4 W when idle and <6 W during lock-in operation.

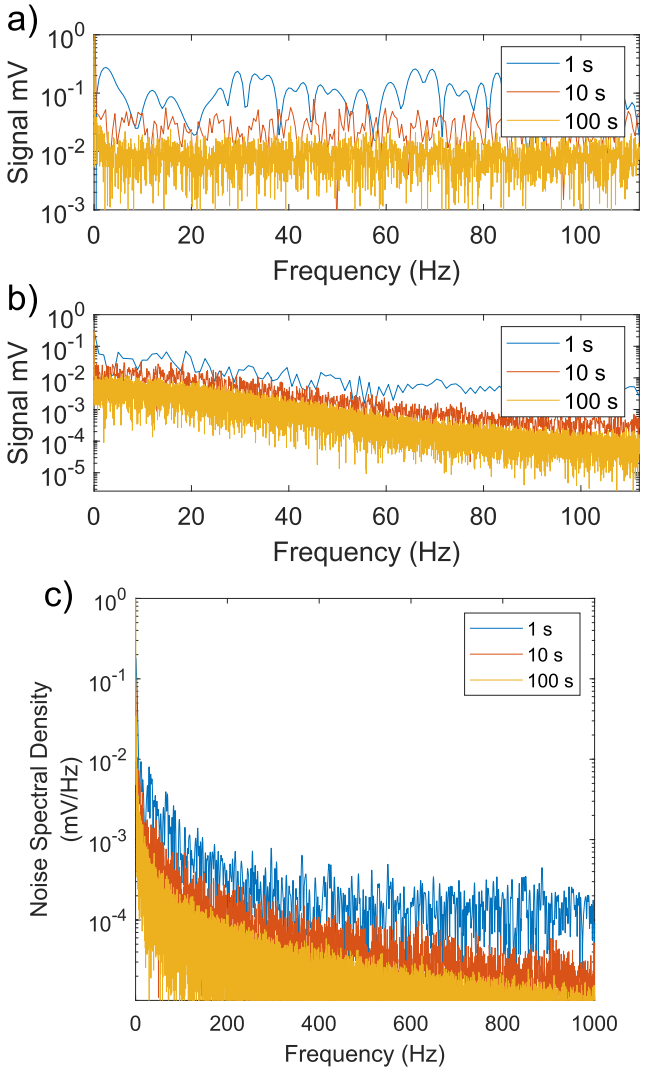

FIG. 13. FFTs of noise data from (a) RePLIA at 500 kHz demodulation with a 1 ms time constant (with 1 s data zero padded) and (b) HF2LI at 1 MHz demodulation and 700 μs time constant, at 1 s (blue), 10 s (red), and 100 s (yellow) collection time (output data is R for both channels). (c) Noise spectral density of the RePLIA at the above input parameters with a wider output frequency spectrum than in Fig. 2.

Cross talk between input channels results in a signal 0.3% of the input signal amplitude reflected in the secondary input. The output voltage range is limited by the board to ±1 V.

Figure 13 represents the same data as Fig. 2 in the main text, but as plain FFTs of noise data as opposed to noise spectral density.

The RePLIA has been used for magnetometry using an ensemble of nitrogen vacancy centers in diamond. We intend to apply this technique to magnetocardiography, where it would be preferable to use approximately 200 sensors, requiring 100 dual channel lock-in amplifiers.[42]

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