A Genaralized Multi-Frequency Impedance Matching Technique

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***Abstract*— This paper describes a generalized multi-frequency impedance transformer capable of providing concurrent matching at arbitrary number of frequencies. A frequency dependent complex load (FDCL) has been considered but the scheme is applicable for real loads as well. The exact analysis of the proposed design results in closed form equations with many independent free variables to cater to the wide range of FDCLs. The proposed theory is validated through a prototype fabricated on Rogers RO5880, with permittivity of 2.2, and working at 0.9/1.8/2.1/2.9 GHz. The good agreement between measured and the EM simulated results validate the proposed technique.**

I. Introduction

A multi-frequency impedance matching network is a key component in majority of the multi-frequency RF/microwave components [1]. The literature is replete with reports on dual-frequency impedance transformers (DBITs) [2]-[7]. Some of these are useful for real load impedances [5], [7] whereas the others considered frequency dependent complex loads (FDCLs). Furthermore, [8] can be used for tri-frequency impedance matching for real load impedance; a systematic approach to design tri-frequency matching network valid for either type of loads was reported in [9]. All of the above mentioned design works at the number of frequencies they were intended for i.e. two and three, and they cannot be extended to higher number of frequencies. Two important works for multi-frequency impedance transformation technique were reported in [10]-[11]. Theoretically, there is no limitation on the number of frequencies that can be considered in [10]. However, design equation becomes more complicated as the number of frequencies is increased. In addition, [10] is valid for lumped elements that are not of much use at higher frequencies. On the other hand, formulations reported in [11] are not in closed form, and always require some optimization and search algorithm to arrive at a solution.

This paper, therefore, proposes a generalized technique to synthesize and design multi-frequency impedance matching network using distributed elements. Essentially, it builds upon the generic tri-frequency matching network reported in [9]. However, that approach cannot be directly extended to multi-frequency scenario, especially due to the use of open-circuited-short-circuited (OCSC) stub combination. An OCSC formulated as in [9] cannot work for more than two frequencies. This paper outlines the necessary modifications to facilitate such design. A quad-frequency matching network is

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Fig. 1. Block level illustration of the proposed scheme.

analyzed, designed and fabricated to illustrate the underlying concepts; theoretically, there is no limitation on the number of frequencies or the type of load in the proposed technique. The exact analytical solution is provided to calculate the design parameters such as characteristic impedance and electrical length of the transmission lines and no optimization algorithm is required for a valid solution. The subsequent sections elaborate on the theoretical postulations and the prototype development followed by discussion on achieved results.

II. The Proposed Impedance Transformer

To illustrate higher level working of the proposed multi-frequency matching technique, a block diagram is shown in Fig. 1. Z_0 and Z_L are the source and the load impedances. The dual-band impedance transformer (DBIT) establishes matching at the first two frequencies. Next, a dual-to-tri-band transformer (DTBT) is incorporated that establishes matching at the third frequency without affecting matching already achieved at the previous two frequencies. More details of DTBT can be referred from [9]. Similarly, a tri-to-quad-band transformer (TQBT) is used to achieve matching at the fourth frequency, and the TQBT must not disturb the matching already established at the previous three frequencies. It is apparent from this description that the scheme can be extended

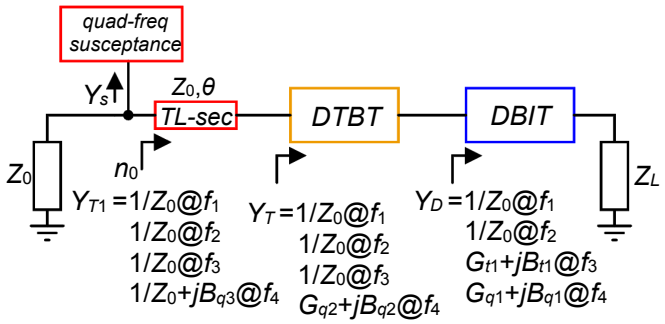

Fig. 2. Proposed quad-frequency impedance matching network.

to a penta-frequency impedance transformer by incorporating a quad-to-penta-band transformer (QPBT), and so on. Thus, theoretically, there is no restriction on the number of frequencies over which the proposed scheme can work.

A. Proposed Quad-Frequency Matching Network

The proposed quad-frequency impedance matching network is shown in Fig. 2. It is apparent from Fig. 2 that the proposed quad-frequency impedance transformer is a series connection of a dual-band impedance transformer (DBIT) [6], a dual-to-tri-band transformer (DTBT) [9], a transmission line (TL)-section", and a quad-frequency susceptance. As the load is frequency dependent, it is assumed to have distinct values at each frequency, namely, $Z_L = R_1 + jX_1$ @ f_1, $Z_L = R_2 + jX_2$ @ f_2, $Z_L = R_3 + jX_3$ @ f_3, and $Z_L = R_4 + jX_4$ @ f_4, and $f_1 < f_2 < f_3 < f_4$. Y_D represents the input admittance looking into the DBIT. Since, DBIT establishes matching at f_1 and f_2, therefore $Y_D = 1/Z_0$ @$f_1$and @f_2. Y_D, in general, will have some complex value $G_{t1}+jB_{t1}$ @f_3 and $G_{q1}+jB_{q1}$ @f_4. Similar comments can be made about Y_T and Y_{T1}−the input admittances looking into the DTBT and the TL-section, respectively. It must be noted that the TL-section and the quad-frequency susceptance constitutes the TQBT. Since, $Y_T = 1/Z_0$ @f_1, @f_2 and @f_3, therefore, the characteristic impedance of TL-section is selected as Z_0. Because of this choice matching is not disturbed at the first three frequencies. Moreover, the electrical length of the TL-section, θ @f_4, is determined such that $\mathrm{Re}(Y_{T1}) = 1/Z_0$ @f_4. Since, admittances sum at a junction, the imaginary part of Y_{T1} ($=B_{q3}$) is to be cancelled at node n_0 using a susceptance, Ys. The susceptance must be a quad-frequency susceptance such that it adds zero susceptance at the first three frequencies, and $-jB_{q3}$ @f_4.

The schematic to realize a quad-frequency susceptance is shown in Fig. 3. This network is also used in multi-frequency DC-feed design [12]. In Fig. 3, the quad-frequency susceptance comprises of four cascaded L-networks for four frequency bands [12]. Each L-network constitutes of a transmission line (TL) section along with a quarter wavelength open stub. The terms "Z_{it}" and "θ_i" is the characteristic impedance and electrical length of the ith TL section, where as "Z_{is}" and "θ_{is}" is the characteristic impedance and the electrical length of the i^{th} stub, with i=1, 2, 3, 4. All these electrical lengths are defined at the respective frequencies.

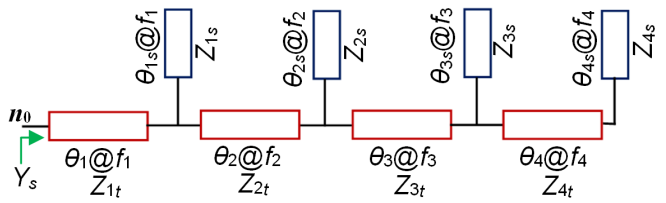

Fig. 3. The quad-frequency susceptance.

Now, the first three sections of the quad-frequency susceptance have been designed in such a way that it provides zero admittance looking into the node n_0 at three frequencies f_1, f_2, and f_3, that is, $Y_s = 0$ @f_1, @f_2 and @f_3. Subsequently, the fourth L-network has been added to get the admittance term Y_s, expressed in (3), to cancel the imaginary part of Y_{T1}. The last two TL-sections in Fig. 3 can be combined together and the simplified expressions are given below.

$$Z_{4t} = Z_{4s} \tag{1}$$

and

$$\theta_{4t} = \theta_4 + \theta_{4s} \tag{2}$$

$$Y_s\big|_{f4} = jY_{1t} * \left[\frac{\tan(a_4 * 90) * (Y_{1s} + Y_{1t}) + Y_{2t} * \frac{A}{B}}{Y_{1t} - Y_{is} * \tan^2(a_4 * 90) - Y_{2t} * \tan(a_4 * 90) * \frac{A}{B}}\right] \tag{3}$$

Where, $a_i = f_i/f_1$, $Y_{is} = 1/Z_{is}$, and $Y_{it} = 1/Z_{it}$ for $i = \{1, 2, 3, 4\}$. The terms A and B in (3) are given by expressions (4) and (5), mentioned at the bottom of this page.

III. Design Procedure

A simplified sequence of design steps for the proposed matching network are summarized as follows:

1) **Step-I:** For a given load impedance, calculate the parameters of the DBIT. The calculations are referred from [6] here. This design should be validated through simulation.
2) **Step-II:** Design a tri-band impedance transformer [9]. Then validate the design again through simulation.
3) **Step-III:** Add a transmission line possessing characteristics impedance equal to the source impedance and with a variable electrical length. The electrical length must be varied in order to bring the real part of $Y_{T1}(=G_{q2})$ equal to $1/Z_0$. Calculate the imaginary part of Y_T at f_4.
4) **Step-IV:** Design the first three sections of quad-frequency susceptance based on the technique used for multi-frequency DC feed network [12] and it must provide open at f_1, f_2, and f_3. Validate the design through simulation.
5) **Step-V:** Add 4th L-network to the quad-frequency susceptance and calculate Z_{4t} and θ_{4T} from (1). Evalaute Y_{in} @ f_4 from (3) and set Y_{in} @ $f_4 = -jB_{q3}$. It is now important to note that Z_{4t} or θ_{4t} are also essentially a free variable here and this provides the proposed technique an additional degree of freedom.

IV. Design Example and Discussion

A design example is considered here for four frequencies as follows: f_1= 0.9 GHz, f_2=1.8 GHz, f_3=2.1 GHz, and f_4=2.9 GHz. A frequency dependent complex load is synthesized using a

$$A = Y_{2s} * \tan\left(\frac{a_4}{a_2} * 90\right) + Y_{2t} * \tan\left(\frac{a_4}{a_2} * \theta_2\right) + Y_{3t} * \left[\frac{Y_{4t} * \tan\theta_4 + y_{3s} * \tan\left(\frac{a_4}{a_3} * 90\right) + Y_{3t} * \tan\left(\frac{a_4}{a_3} * \theta_3\right)}{Y_{3t} - Y_{4t} * \tan\theta_4 * \tan\left(\frac{a_4}{a_3} * \theta_3\right) - Y_{3s} * \tan\left(\frac{a_4}{a_3} * 90\right) * \tan\left(\frac{a_4}{a_3} * \theta_3\right)}\right] \tag{4}$$

$$B = Y_{2t} - Y_{2s} * \tan\left(\frac{a_4}{a_2} * \theta_2\right) * \tan\left(\frac{a_4}{a_2} * 90\right) - Y_{3t} * \tan\left(\frac{a_4}{a_2} * \theta_2\right) * \left[\frac{Y_{4t} * \tan\theta_4 + Y_{3s} * \tan\left(\frac{a_4}{a_3} * 90\right) + Y_{3t} * \tan\left(\frac{a_4}{a_3} * \theta_3\right)}{Y_{3t} - Y_{4t} * \tan\theta_4 * \tan\left(\frac{a_4}{a_3} * \theta_3\right) - Y_{3s} * \tan\left(\frac{a_4}{a_3} * 90\right) * \tan\left(\frac{a_4}{a_3} * \theta_3\right)}\right] \tag{5}$$

length of line and an SMD resistor. Variation of the real and imaginary parts of this FDCL is shown in Fig. 4, and it is found that Z_L= 43.97 + *j*22.39 @f_1, 57.62 + *j*45.73 @f_2, 65.71 + *j*53.43 @f_3, and 101.59 + *j*68.17 @f_4.

As explained in Section III, the first step is to design DBIT and DTBT, which can be referred from [6], [9].Their schematics are shown in Fig. 5. The electrical lengths and the characteristics impedances of the various transmission line sections of DBIT and DTBT are given in Table I. For clarity, it is reemphasized that the DBIT provides matching at the first two frequencies, f_1 and f_2. Values of Y_D at the third and fourth frequency, that is, G_{t1}+*j*B_{t1} @f_3 and G_{q1}+*j*B_{q1} @f_4 are found to be as mentioned in Table II. The value at the third frequency is used to design DTBT that establishes matching at the third frequency [9]. Inclusion of DTBT provides matching at the first three frequencies of f_1, f_2, and f_3. DTBT transforms G_{q1}+*j*B_{q1} @f_4 into G_{q2}+*j*B_{q2} @f_4. It is apparent from Table III that real part of Y_T@f_4 (=G_{q2}) is not equal to $1/Z_0$=0.02.

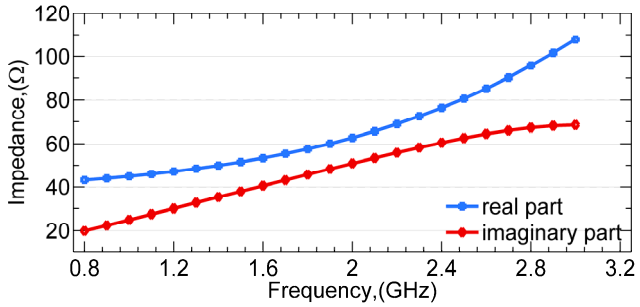

Fig. 4. Variation of the load impedance (Z_L) with frequency.

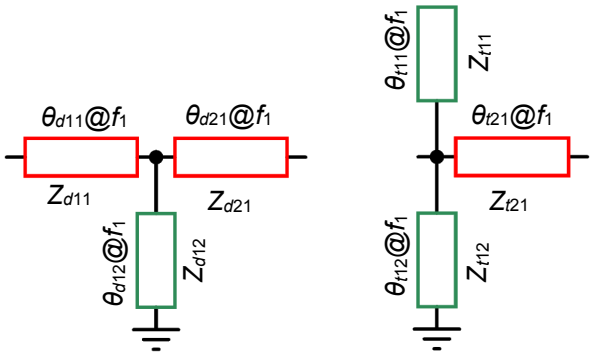

Fig. 5. Schematics of DBIT [6] and DTBT[9] used in this paper.

TABLE I. DESIGN PARAMETERS OF DBIT AND DTBT

Network	Impedance	value(Ω)	Electrical length	value(°) @f_1
DBIT	Z_{d11}	99	θ_{d11}	60
	Z_{d12}	65.51	θ_{d12}	120
	Z_{d21}	89.43	θ_{d21}	39.18
DTBT	Z_{t11}	65.8	θ_{d11}	60
	Z_{t21}	21.93	θ_{d12}	60
	Z_{t11}	50	θ_{d21}	45.5

TABLE II. ADMITTANCE Y_D

Frequency	Y_D
2.1 GHz	0.003294 + *j*0.001802
2.9 GHz	0.009929 + *j*0.019631

TABLE III. ADMITTANCE Y_T AND Y_{T1}

Frequency	Y_T	Y_{T1}
2.9 GHz	0.001211 + *j*0.010543	0.02 + *j*0.08750

TABLE IV. DESIGN PARAMETERS OF QUAD-BAND SUSCEPTANCE

Impedance	value(Ω)	Electrical length	value(°)
Z_{1t}	60	θ_1	90 @ f_1
Z_{2t}	60	θ_2	45 @f_1
Z_{3t}	60	θ_3	68.91 @f_1
Z_{1s}	100	θ_{1s}	90 @f_1
Z_{2s}	100	θ_{2s}	90 @f_2
Z_{3s}	100	θ_{3s}	90 @ f_3
Z_{4t}= Z_{4s}	60	θ_{4T}	14.09 @f_1

A transmission line of 50 Ω is therefore added from the source side whose electrical length, θ, can be found using tuning feature available in the Keysight ADS to get the input impedance equal to 50 Ω. Alternatively, formula of input impedance could also be invoked to find the electrical analytically as follows:

$$Y_A = \frac{1}{Z_0} * \frac{Z_0 + j(1/Y_T) * \tan\theta}{(1/Y_T) + jZ_0 * \tan\theta} \tag{6}$$

$$\mathrm{Re}(Y_A) = 0.02 \tag{7}$$

The above equations can be solved to evaluate θ. It must be noted that the value of Y_T in (6) corresponds to f4 and it can be read from Table III.

The electrical length of 50 Ω TL-section is calculated as θ =32.768° @ f_1. Now, at the input of TL-section the impedance is matched at three frequencies while at fourth frequency the admittance (Y_{T1}) is calculated and given in Table III. The imaginary part of Y_{T1} as given in Table III is used to design the quad-frequency stub is designed. More details of quad-frequency stub design can be obtained from [12]. The values of various line impedances and electrical lengths are tabulated in Table IV.

The following two points must be clear from above descriptions:

1) There is no limitation on the number of frequency bands. For example, extension to penta-frequency matching would require addition of a 50Ω TL-section and a quad-to-penta-band transformer (QPBT). A QPBT can be designed as a special case of multi-frequency DC-feed outlined in [12].
2) There is no limitation on type of load. In fact, as pointed out in [9], the type of load depends on the type of the

DBIT used in multi-frequency matching network. If the DBIT could handle an FDCL, the multi-frequency matching network will work for FDCL. If the DBIT can work for a real load, the multi-frequency matching network will work for real loads.

V. Simulation and Measurement Results

Based on the design example outlined in the previous section, a prototype is fabricated on the Rogers RO5880 substrate with ϵ_r = 2.2, tanδ = 0.0009 and substrate thickness of 1.575mm. The copper cladding of the laminate is 35µm on both the sides.

The prototype is shown in Fig. 6. The final design is achieved after optimizations in the Keysight ADS simulation tool due to several junction discontinuities present in the design. The measurement results are compared with the EM simulations and are depicted in Fig. 7. It can be observed that the EM and measured results are in good agreement. A slight deviation on the response can be attributed to the optimizations done to address the discontinuities in the design, and due to anomaly in the resistor models.

A comparison of the proposed design technique with the previously reported designs is presented in Table V. It is apparent that the proposed scheme helps overcome many limitations of state-of-the-art designs.

VI. Conclusion

A simple and systematic design approach to design a novel quad-frequency impedance transformer with closed form design equations is reported. The technique has been validate through a prototype developed on RO5880 substrate. It can be said that this technique could be extended to penta-band or beyond by utilizing additional sections of L-networks. However, this will come at a price of increased board size. Moreover, there is no restriction on the type of load to be considered.

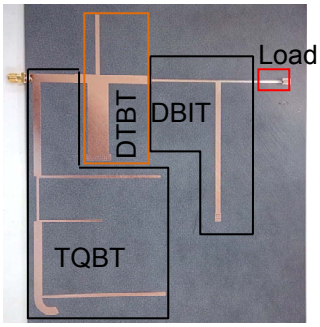

Fig. 6. The fabricated quad-frequency impedance transformer on RO5880.

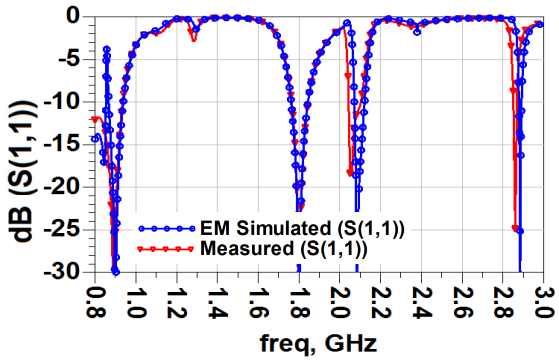

Fig. 7. EM simulated and measured return loss.

TABLE V. Comparison with previous designs

Ref.	Frequency Bands	Type of Load	Lumped/Distributed
[3]	2	FDCL	Distributed
[8]	3	Real	Distributed
[9]	3	Both	Distributed
[10]	multi	FDCL	Lumped
[11]	multi	FDCL	Distributed
This Work	multi	Both	Distributed

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