

Thuvaragan Sooriyakumaran

ENGINEERING UNDERGRAD · DESIGNER · DEVELOPER

[✉️](mailto:thuvaragan28@gmail.com) [👤](https://github.com/thuvasooriya) [🔗](https://www.linkedin.com/in/thuvasooriya/) [@thuvasooriya](https://twitter.com/thuvasooriya) [📅](#) Last updated: 2025-11-04

From planet earth, loves to integrate art, science and technology to create a smile in the face of others. Moderate experience in systems programming, robotics, digital design, algorithms, and performance optimization.

Complimentary experience in web development, cross-platform app development, audio manipulation, and graphics manipulation. Currently obsessed with modular robotics, RISC-V IP design, open-source toolchains, and devops of corresponding workflows.

Projects

Qwen3-0.6B inference pipeline on custom RV32IM core in FPGA

DVCON 25 - INDIA: 1ST RUNNER'S UP

- Research and Implementation project for DVCON25 to design a novel resource efficient accelerator IP for a custom RV32IM core
- Ran whole inference pipeline of Qwen3-0.6B with Q8 quantization and custom token embeddings

ViT Accelerator IP for a custom RISC-V core in FPGA

DVCON 24 - INDIA

- Research and Implementation project for DVCON24 to design a novel ViT accelerator IP for a custom RISC-V core
- Selected in the 20 teams from >100 teams in Stage 1

Image segmentation research and evaluation for bin-picking

SEMESTER 4 GROUP PROJECT

- Extensive literary review and recreation of image segmentation and CNN model papers in python
- Development of simple gripper mechanism and associated PCB for testing
- Extensive testing, benchmarking and documentation

Smart plug product research and development

SEMESTER 2 GROUP PROJECT, SHORT COURSE GROUP PROJECT

- Smart plug with remote control through LAN and WAN, developed around ESP32-S3 micro controller
- Another smart plug design and implementation was followed as part of a short course

STM32 two-wheeled line follower robot with simple manipulator

SEMESTER 3 GROUP PROJECT

- Prototyped, designed and implemented a robot that is capable of following white, colored lines
- Custom arm mechanism was designed and integrated to achieve required object manipulation

Portable doctor companion device with SBC

MECHA 23 - 2ND RUNNER UP

- Integrating ECG monitor and SpO₂ sensor with machine learning to make screening process easier for doctors
- Orange-Pi Zero 2W SBC is used with custom Linux to integrate monitoring, web-server and prediction algorithms

Maze Solving Micromouse

ROBOFEST 24

- Maze Solving micromouse using STM32F411 microcontroller.
- Participated in RoboFest 24, Research on 2nd prototype ongoing.

Analog ECG monitor PCB development

SEMESTER 3 GROUP PROJECT

Semester 5 Group Projects

DEMONSTRATED AS PER CORRESPONDING MODULES

- RISC-V RV32I pipeline-processor research and implementation
- Single Precision FPU IP research and implementation
- Robot manipulator with 4 DOF

Semester 7 Group Projects

IN PROGRESS AS PER MODULE REQUIREMENTS

- ROS2 Labs and cross-platform testing
- BitSerial Bus implementation with 3 masters and 3 slaves
- MNIST Co-Processor-Accelerator IP implementation
- Promoter Analysis

[👤](#) [🔗](#) [📅](#) [thuvasooriya/ip_gemma](#)

May 2025 - Sep 2025

[👤](#) [🔗](#) [📅](#) [thuvasooriya/vit-malware-detector](#)

May 2024 - Sep 2024

[👤](#) [🔗](#) [📅](#) [mora-bprs/sam-model](#)

March 2024 - June 2024

[👤](#) [🔗](#) [📅](#) [thuvasooriya/pluggu](#)

Mar 2023 - May 2023

[👤](#) [🔗](#) [📅](#) [team-itro/sem3slrc](#)

Aug 2023 - Dec 2023

[👤](#) [🔗](#) [📅](#) [biosense-ai/biosense-ai-web-server](#)

Aug 2023 - Oct 2023

[👤](#) [🔗](#) [📅](#) [team-itro/kitro](#)

Sep 2024 - Dec 2024

Aug 2023 - Oct 2023

Sep 2024 - Dec 2024

Sep 2025 - Present

Skills

Programming C/C++, System{Verilog}, Python, TypeScript, Zig, Rust, Lua, Nix

Languages English, Tamil, Sinhala, Japanese, French

Tools KiCAD / Altium Designer, Vivado / Verilator, ROS, SolidWorks, MATLAB

Achievements

Lead Deputy Batch Representative, Engineering Faculty, University of Moratuwa,
Senior(Head) Prefect, 2020, Jaffna Hindu College

Awards Right To Information Act, National Debate - 1st Place, Tamil, Team Lead,
All Island Senior Dialog Drama - 3rd Place

Education

BSc. in Engineering - Electronics and Telecommunication

Colombo, SriLanka

UNIVERSITY OF MORATUWA | CURRENT CGPA - 3.715

2021 - Present

Chartered Global Management Accounting (CGMA)

Colombo, SriLanka

ACHIEVERS LANKA | CERTIFICATE LEVEL COMPLETED

2021 - Present

Embedded Product Design for IoT

Colombo, SriLanka

SHORT COURSE BY ENTC DEPARTMENT UoM WITH SKILLSURF.LK

Aug 2023 - Nov 2023

- PCB design, firmware development, enclosure design in OnShape, end 2 end connectivity in web dashboard

System {Verilog} for ASIC/FPGA Design & Simulation

Colombo, SriLanka

SHORT COURSE BY ENTC DEPARTMENT UoM WITH SKILLSURF.LK

Jan 2023 - May 2023

- Assignment 3 - ASIC flow report for MVM UART using SAED 32nm EDK & Synopsys design compiler
- Assignment 4 - FPGA implementation and demo of MVM UART

Full Stack Web Development (MERN Stack)

Jaffna, SriLanka

UKI CODING SCHOOL - DIGITAL COHORT 1

Feb 2021 - July 2021

Secondary Education

Jaffna, SriLanka

JAFFNA HINDU COLLEGE | G.C.E. OL - 9A | G.C.E. AL - 3A

2011 - 2020

Experience

Research Assistant - Internship

Remote - Singapore

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING (SCSE), NTU

2024 Dec - 2025 Jul

- C99 Bundle adjustment implementation
- Implementation and comparision of QEMU, LiteX-Sim, Chipyard, and ZCU-102 compilation and workflows
- Literary review of Vector processing options for Rocket core
- ARM core and Rocket core shared memory implementation of SLAM workflow

Junior Graphic Designer

Jaffna, SriLanka

MATHI COLOURS PRINTERS

2020 - 2021

Digital Marketing Assistant

Jaffna, SriLanka

ECOSTEEM PVT. LTD.

2021

References

Dr. Ranga Rodrigo

ranga@uom.lk

B.Sc. ENG. HONS. (MORATUWA), M.E.Sc. (WESTERN, CANADA), PH.D. (WESTERN, CANADA), SMIEEE

SENIOR LECTURER, UNIVERSITY OF MORATUWA

Senthilmaran Ratnam

senthilmaran@gmail.com

PRINCIPAL, JAFFNA HINDU COLLEGE | LLB LAW HONS.