

# Haowen Tan

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## EDUCATION

### University of Michigan (Dual-Degree program)

*Bachelor of Engineering in Computer Engineering, Minor in Math*

Ann Arbor, MI

Sep 2022 – May 2024

### Shanghai Jiaotong University (Dual-Degree program)

*Bachelor of Engineering in Electrical and Computer Engineering*

Shanghai

Sep 2020 – Aug 2022

## RELATED PROJECTS

### P6 Processor | *SystemVerilog, Verdi, RISC-V*

Feb 2023 – Present

- Developed an out of order processor based on P6 architecture
- Implemented modules and Built own testcases with System Verilog
- Used Verdi to debug

### 8-bit Dual-Mode Ripple-Carry Adder | *Cadence Virtuoso*

Nov 2022 – Dec 2022

- Developed a Dual-Mode Ripple-Carry Adder on MOSFET level
- Implemented the mirror adder, registers and muxes with MOSFET circuits
- Used vector file to validate the circuit functionalities

### Projects on Basys 3 FPGA board | *Verilog, Xilinx Vivado*

May 2022 – Aug 2022

- A two-digit timer that counts the seconds from 00 to 59 and displays the digits using the seven segment displays
- Keypad scanner reads the keys from a 4-by-4 keypad and displays the corresponding hexadecimal value on an SSD
- A digital system with two modes. One mode it rolls student ID across the four SSDs, the other behaves as a simple calculator

## TECHNICAL SKILLS

**Languages:** SystemVerilog/Verilog, C/C++, MATLAB, LaTeX, JavaScript

**Developer Tools:** Git, VS Code/Visual Studio, Cadence Virtuoso, Xilinx Vivado, OrCAD, Multisim, Solidworks

**Systems:** Windows+WSL, Linux

**Platforms:** Bitbucket, GitHub

## EXPERIENCE

### Undergraduate Research Assistant

*Shanghai Jiaotong University*

Dec 2021 – Feb 2022

*UM-SJTU Joint Institute Lab*

- Developed Ultra-wideband (UWB) device for distance exploration
- Used C language to implement functions for DW1000 device (from Decawave)

## HONOR

**Fall 2022 Dean's Honor List (University of Michigan)**