BST A1000 GMAC Register Description

V 0.1

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修订记录

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1	V0.1		2022-01-05	文档初始版本	无

注： 1. 文档每一次修订时必须填写完整修订记录；.
2. 第一次编写该模板，原因与备注科填写“无”.

目　　录

1 Product Introduction

BST A1000 GMAC Peripheral Register Description

GMAC address domain:

0:3000:0000	0:300F:FFFF	1M	GMAC0
0:3010:0000	0:301F:FFFF	1M	GMAC1

2 Register Description

2.1 EQOS_DMA

Module Name	EQOS_DMA
Sub Module Name	
Data Width	32
Address Width	32
Base Address	0x0

2.1.1 EQOS_DMA_R_DMA_MODE

Access Type: RW

Address Offset: 0x1000

Name	Access	Bit Range	Reset value	Description
RESERVED_31_18	R	[31:18]	0x0	Reserved. Value After Reset: 0x0
INTM	R/W	[17:16]	0x0	Interrupt Mode This field defines the interrupt mode of DWC_ether_qos. The behavior of the following outputs changes depending on the following settings: sbd_perch_tx_intr_o[] (Transmit Per Channel Interrupt) sbd_perch_rx_intr_o[] (Receive Per Channel Interrupt) sbd_intr_o (Common Interrupt) It also changes the behavior of the RI/TI bits in the DMA_CH0_Status.

				00: sbd_perch_* are pulse signals for each TX/RX packet transfer completion events (irrespective of whether corresponding interrupts are enabled) for which IOC bits are enabled in descriptor. sbd_intr_o is also asserted when corresponding interrupts are enabled and cleared only when software clears the corresponding RI/TI status bits. 01: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. 10: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. However, the signal is asserted again if the same event occurred again before it was cleared. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. 11: Reserved For more details please refer Table "DWC_ether_qos Transfer Complete Interrupt Behavior".Values: 0x0 (MODE0): See above description 0x1 (MODE1): See above description 0x2 (MODE2): See above description 0x3 (RSVD): Reserved Value After Reset: 0x0
RESERVED_15	R	[15:15]	0x0	

				Reserved. Value After Reset: 0x0
RESERVED	R	[14:9]	0x0	Reserved Field: Yes
DSPW	R/W	[8:8]	0x0	Descriptor Posted Write When this bit is set to 0, the descriptor writes are always non-posted. When this bit is set to 1, the descriptor writes are non-posted only when IOC (Interrupt on completion) is set in last descriptor, otherwise the descriptor writes are always posted.Values: 0x0 (DISABLE): Descriptor Posted Write is disabled 0x1 (ENABLE): Descriptor Posted Write is enabled Value After Reset: 0x0
RESERVED_7_5	R	[7:5]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[4:1]	0x0	Reserved Field: Yes
SWR	R/W	[0:0]	0x0	Software Reset When this bit is set, the MAC and the DMA controller reset the logic and all internal registers of the DMA, MTL, and MAC. This bit is automatically cleared after the reset operation is complete in all DWC_ether_qos clock domains. Before reprogramming any DWC_ether_qos register, a value of zero should be read in this bit. This bit must be read at least 4 CSR clock cycles after it is written to 1. Note: The reset operation is complete only when all resets in all active clock domains are de-asserted. Therefore, it is essential that all PHY inputs clocks (applicable for the selected PHY interface) are present for software reset completion. The time to complete the software reset operation depends on the frequency of the slowest active clock. Access restriction applies. Setting 1 sets.

				Self-cleared. Setting 0 has no effect.Values: 0x0 (DISABLE): Software Reset is disabled 0x1 (ENABLE): Software Reset is enabled Value After Reset: 0x0 Testable: untestable

2.1.2 EQOS_DMA_R_DMA_SYSBUS_MODE

Access Type: RW

Address Offset: 0x1004

Name	Access	Bit Range	Reset value	Description
EN_LPI	R/W	[31:31]	0x0	Enable Low Power Interface (LPI) When set to 1, this bit enables the LPI mode supported by the EQOS-AXI configuration and accepts the LPI request from the AXI System Clock controller. When set to 0, this bit disables the LPI mode and always denies the LPI request from the AXI System Clock controller.Values: 0x0 (DISABLE): Low Power Interface (LPI) is disabled 0x1 (ENABLE): Low Power Interface (LPI) is enabled Value After Reset: 0x0
RESERVED	R	[30:30]	0x0	Reserved Field: Yes
RESERVED_29_Y	R	[29:28]	0x0	Reserved. Value After Reset: 0x0
WR_OSR_LMT	R/W	[27:24]	0x1	AXI Maximum Write Outstanding Request Limit This value limits the maximum outstanding request on the AXI write interface. Maximum outstanding requests = WR_OSR_LMT + 1 Note:

				Bit 26 is reserved if DWC_ETHER_QOS_AXI_MAX_WR_REQ = 4 Bit 27 is reserved if DWC_ETHER_QOS_AXI_MAX_WR_REQ!= 16 Value After Reset: 0x1
RESERVED_23_Y	R	[23:20]	0x0	Reserved. Value After Reset: 0x0
RD_OSR_LMT	R/W	[19:16]	0x1	AXI Maximum Read Outstanding Request Limit This value limits the maximum outstanding request on the AXI read interface. Maximum outstanding requests = RD_OSR_LMT + 1 Note: Bit 18 is reserved if parameter DWC_ETHER_QOS_AXI_MAX_RD_REQ = 4 Bit 19 is reserved if parameter DWC_ETHER_QOS_AXI_MAX_RD_REQ!= 16 Value After Reset: 0x1
RESERVED	R	[15:14]	0x0	Reserved Field: Yes
ONEKBBE	R/W	[13:13]	0x0	1 KB Boundary Crossing Enable for the EQOS-AXI Master When set, the burst transfers performed by the EQOS-AXI master do not cross 1 KB boundary. When reset, the burst transfers performed by the EQOS-AXI master do not cross 4 KB boundary.Values: 0x0 (DISABLE): 1 KB Boundary Crossing for the EQOS-AXI Master Beats is disabled 0x1 (ENABLE): 1 KB Boundary Crossing for the EQOS-AXI Master Beats is enabled

				Value After Reset: 0x0
AAL	R/W	[12:12]	0x0	Address-Aligned Beats When this bit is set to 1, the EQOS-AXI or EQOS-AHB master performs address-aligned burst transfers on Read and Write channels.Values: 0x0 (DISABLE): Address-Aligned Beats is disabled 0x1 (ENABLE): Address-Aligned Beats is enabled Value After Reset: 0x0
EAME	R/W	[11:11]	0x0	Enhanced Address Mode Enable. When this bit is set to 1, the DMA master enables the enhanced address mode (40-bit or 48-bit addressing mode). In this mode, the DMA engine uses either the 40- or 48-bit address, depending on the configuration.Values: 0x0 (DISABLE): Enhanced Address Mode is disabled 0x1 (ENABLE): Enhanced Address Mode is enabled Value After Reset: 0x0
AALE	R/W	[10:10]	0x0	Automatic AXI LPI enable When set to 1, enables the AXI master to enter into LPI state when there is no activity in the DWC_ether_qos for number of system clock cycles programmed in the LPIEI field of AXI_LPI_Entry_Interval register.Values: 0x0 (DISABLE): Automatic AXI LPI is disabled 0x1 (ENABLE): Automatic AXI LPI is enabled Value After Reset: 0x0

RESERVED_9_8	R	[9:8]	0x0	Reserved. Value After Reset: 0x0
BLEN256	R/W	[7:7]	0x0	AXI Burst Length 256 When this bit is set to 1, the EQOS-AXI master can select a burst length of 256 on the AXI interface.Values: 0x0 (DISABLE): No effect 0x1 (ENABLE): AXI Burst Length 256 Value After Reset: 0x0
BLEN128	R/W	[6:6]	0x0	AXI Burst Length 128 When this bit is set to 1, the EQOS-AXI master can select a burst length of 128 on the AXI interface.Values: 0x0 (DISABLE): No effect 0x1 (ENABLE): AXI Burst Length 128 Value After Reset: 0x0
BLEN64	R/W	[5:5]	0x0	AXI Burst Length 64 When this bit is set to 1, the EQOS-AXI master can select a burst length of 64 on the AXI interface.Values: 0x0 (DISABLE): No effect 0x1 (ENABLE): AXI Burst Length 64 Value After Reset: 0x0
BLEN32	R/W	[4:4]	0x0	AXI Burst Length 32 When this bit is set to 1, the EQOS-AXI master can

				select a burst length of 32 on the AXI interface.Values: 0x0 (DISABLE): No effect 0x1 (ENABLE): AXI Burst Length 32 Value After Reset: 0x0
BLEN16	R/W	[3:3]	0x0	AXI Burst Length 16 When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 16 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect.Values: 0x0 (DISABLE): No effect 0x1 (ENABLE): AXI Burst Length 16 Value After Reset: 0x0
BLEN8	R/W	[2:2]	0x0	AXI Burst Length 8 When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 8 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect.Values: 0x0 (DISABLE): No effect 0x1 (ENABLE): AXI Burst Length 8 Value After Reset: 0x0
BLEN4	R/W	[1:1]	0x0	AXI Burst Length 4 When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 4 on the AXI interface. When the FB bit is set to 0, setting this bit has no

				effect.Values: 0x0 (DISABLE): No effect 0x1 (ENABLE): AXI Burst Length 4 Value After Reset: 0x0
FB	R/W	[0:0]	0x0	Fixed Burst Length When this bit is set to 1, the EQOS-AXI master initiates burst transfers of specified lengths as given below. Burst transfers of fixed burst lengths as indicated by the BLEN256, BLEN128, BLEN64, BLEN32, BLEN16, BLEN8, or BLEN4 field Burst transfers of length 1 When this bit is set to 0, the EQOS-AXI master initiates burst transfers that are equal to or less than the maximum allowed burst length programmed in Bits[7:1].Values: 0x0 (DISABLE): Fixed Burst Length is disabled 0x1 (ENABLE): Fixed Burst Length is enabled Value After Reset: 0x0

2.1.3 EQOS_DMA_R_DMA_INTERRUPT_STATUS

Access Type: RW

Address Offset: 0x1008

Name	Access	Bit Range	Reset value	Description
RESERVED_31_18	R	[31:18]	0x0	Reserved. Value After Reset: 0x0
MACIS	R	[17:17]	0x0	MAC Interrupt Status

				This bit indicates an interrupt event in the MAC. To reset this bit to 1'b0, the software must read the corresponding register in the MAC to get the exact cause of the interrupt and clear its source.Values: 0x0 (INACTIVE): MAC Interrupt Status not detected 0x1 (ACTIVE): MAC Interrupt Status detected Value After Reset: 0x0
MTLIS	R	[16:16]	0x0	MTL Interrupt Status This bit indicates an interrupt event in the MTL. To reset this bit to 1'b0, the software must read the corresponding register in the MTL to get the exact cause of the interrupt and clear its source.Values: 0x0 (INACTIVE): MTL Interrupt Status not detected 0x1 (ACTIVE): MTL Interrupt Status detected Value After Reset: 0x0
RESERVED_15_8	R	[15:8]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[7:4]	0x0	Reserved Field: Yes
DC3IS	R	[3:3]	0x0	DMA Channel 3 Interrupt Status This bit indicates an interrupt event in DMA Channel 3. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 3 to get the exact cause of the interrupt and clear its source.Values: 0x0 (INACTIVE): DMA Channel 3 Interrupt Status not detected 0x1 (ACTIVE): DMA Channel 3 Interrupt Status

				detected Value After Reset: 0x0
DC2IS	R	[2:2]	0x0	DMA Channel 2 Interrupt Status This bit indicates an interrupt event in DMA Channel 2. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 2 to get the exact cause of the interrupt and clear its source.Values: 0x0 (INACTIVE): DMA Channel 2 Interrupt Status not detected 0x1 (ACTIVE): DMA Channel 2 Interrupt Status detected Value After Reset: 0x0
DC1IS	R	[1:1]	0x0	DMA Channel 1 Interrupt Status This bit indicates an interrupt event in DMA Channel 1. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 1 to get the exact cause of the interrupt and clear its source.Values: 0x0 (INACTIVE): DMA Channel 1 Interrupt Status not detected 0x1 (ACTIVE): DMA Channel 1 Interrupt Status detected Value After Reset: 0x0
DC0IS	R	[0:0]	0x0	DMA Channel 0 Interrupt Status This bit indicates an interrupt event in DMA Channel 0. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 0 to get the exact cause of the interrupt and clear its source.Values:

				0x0 (INACTIVE): DMA Channel 0 Interrupt Status not detected 0x1 (ACTIVE): DMA Channel 0 Interrupt Status detected Value After Reset: 0x0

2.1.4 EQOS_DMA_R_DMA_DEBUG_STATUS0

Access Type: RW

Address Offset: 0x100c

Name	Access	Bit Range	Reset value	Description
TPS2	R	[31:28]	0x0	DMA Channel 2 Transmit Process State This field indicates the Tx DMA FSM state for Channel 2. The MSB of this field always returns 0. This field does not generate an interrupt.Values: 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued) 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor) 0x2 (RUN_WS): Running (Waiting for status) 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)) 0x4 (TSTMP_WS): Timestamp write state 0x5 (RSVD): Reserved for future use 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow) 0x7 (RUN_CTD): Running (Closing Tx Descriptor)

				Value After Reset: 0x0
RPS2	R	[27:24]	0x0	DMA Channel 2 Receive Process State This field indicates the Rx DMA FSM state for Channel 2. The MSB of this field always returns 0. This field does not generate an interrupt.Values: 0x0 (STOP): Stopped (Reset or Stop Receive Command issued) 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor) 0x2 (RSVD): Reserved for future use 0x3 (RUN_WRP): Running (Waiting for Rx packet) 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable) 0x5 (RUN_CRD): Running (Closing the Rx Descriptor) 0x6 (TSTMP): Timestamp write state 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory) Value After Reset: 0x0
TPS1	R	[23:20]	0x0	DMA Channel 1 Transmit Process State This field indicates the Tx DMA FSM state for Channel 1. The MSB of this field always returns 0. This field does not generate an interrupt.Values: 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued) 0x1 (RUN_FTTD): Running (Fetching Tx Transfer

				Descriptor) 0x2 (RUN_WS): Running (Waiting for status) 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)) 0x4 (TSTMP_WS): Timestamp write state 0x5 (RSVD): Reserved for future use 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow) 0x7 (RUN_CTD): Running (Closing Tx Descriptor) Value After Reset: 0x0
RPS1	R	[19:16]	0x0	DMA Channel 1 Receive Process State This field indicates the Rx DMA FSM state for Channel 1. The MSB of this field always returns 0. This field does not generate an interrupt.Values: 0x0 (STOP): Stopped (Reset or Stop Receive Command issued) 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor) 0x2 (RSVD): Reserved for future use 0x3 (RUN_WRP): Running (Waiting for Rx packet) 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable) 0x5 (RUN_CRD): Running (Closing the Rx Descriptor) 0x6 (TSTMP): Timestamp write state

				0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory) Value After Reset: 0x0
TPS0	R	[15:12]	0x0	DMA Channel 0 Transmit Process State This field indicates the Tx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt.Values: 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued) 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor) 0x2 (RUN_WS): Running (Waiting for status) 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)) 0x4 (TSTMP_WS): Timestamp write state 0x5 (RSVD): Reserved for future use 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow) 0x7 (RUN_CTD): Running (Closing Tx Descriptor) Value After Reset: 0x0
RPS0	R	[11:8]	0x0	DMA Channel 0 Receive Process State This field indicates the Rx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt.Values:

				0x0 (STOP): Stopped (Reset or Stop Receive Command issued) 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor) 0x2 (RSVD): Reserved for future use 0x3 (RUN_WRP): Running (Waiting for Rx packet) 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable) 0x5 (RUN_CRD): Running (Closing the Rx Descriptor) 0x6 (TSTMP): Timestamp write state 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory) Value After Reset: 0x0
RESERVED_7_2	R	[7:2]	0x0	Reserved. Value After Reset: 0x0
AXRHSTS	R	[1:1]	0x0	AXI Master Read Channel Status When high, this bit indicates that the read channel of the AXI master is active, and it is transferring the data.Values: 0x0 (INACTIVE): AXI Master Read Channel Status not detected 0x1 (ACTIVE): AXI Master Read Channel Status detected Value After Reset: 0x0
AXWHSTS	R	[0:0]	0x0	

				AXI Master Write Channel When high, this bit indicates that the write channel of the AXI master is active, and it is transferring data.Values: 0x0 (INACTIVE): AXI Master Write Channel or AHB Master Status not detected 0x1 (ACTIVE): AXI Master Write Channel or AHB Master Status detected Value After Reset: 0x0

2.1.5 EQOS_DMA_R_DMA_DEBUG_STATUS1

Access Type: RW

Address Offset: 0x1010

Name	Access	Bit Range	Reset value	Description
RESERVED	R	[31:8]	0x0	Reserved Field: Yes
TPS3	R	[7:4]	0x0	DMA Channel 3 Transmit Process State This field indicates the Tx DMA FSM state for Channel 3. The MSB of this field always returns 0. This field does not generate an interrupt.Values: 0x0 (STOP): Stopped (Reset or Stop Transmit Command issued) 0x1 (RUN_FTTD): Running (Fetching Tx Transfer Descriptor) 0x2 (RUN_WS): Running (Waiting for status) 0x3 (RUN_RDS): Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)) 0x4 (TSTMP_WS): Timestamp write state 0x5 (RSVD): Reserved for future use 0x6 (SUSPND): Suspended (Tx Descriptor Unavailable

				or Tx Buffer Underflow) 0x7 (RUN_CTD): Running (Closing Tx Descriptor) Value After Reset: 0x0
RPS3	R	[3:0]	0x0	DMA Channel 3 Receive Process State This field indicates the Rx DMA FSM state for Channel 3. The MSB of this field always returns 0. This field does not generate an interrupt.Values: 0x0 (STOP): Stopped (Reset or Stop Receive Command issued) 0x1 (RUN_FRTD): Running (Fetching Rx Transfer Descriptor) 0x2 (RSVD): Reserved for future use 0x3 (RUN_WRP): Running (Waiting for Rx packet) 0x4 (SUSPND): Suspended (Rx Descriptor Unavailable) 0x5 (RUN_CRD): Running (Closing the Rx Descriptor) 0x6 (TSTMP): Timestamp write state 0x7 (RUN_TRP): Running (Transferring the received packet data from the Rx buffer to the system memory) Value After Reset: 0x0

2.1.6 EQOS_DMA_R_AXI4_TX_AR_ACE_CONTROL

Access Type: RW

Address Offset: 0x1020

Name	Access	Bit Range	Reset value	Description
RESERVED_31_22	R	[31:22]	0x0	Reserved. Value After Reset: 0x0

THD	R/W	[21:20]	0x0	Transmit DMA First Packet Buffer This field is used to drive ardomain_o[1:0] signal when Transmit DMA is accessing First Buffer of the Packet (First valid buffer with FD being set in the TDES3 of the Descriptor). Value After Reset: 0x0
THC	R/W	[19:16]	0x0	Transmit DMA First Packet Buffer This field is used to drive arcache_o[3:0] signal when Transmit DMA is accessing First Buffer of the Packet (First valid buffer with FD being set in the TDES3 of the Descriptor).. Value After Reset: 0x0
RESERVED_15_14	R	[15:14]	0x0	Reserved. Value After Reset: 0x0
TED	R/W	[13:12]	0x0	Transmit DMA Extended Packet Buffer This field is used to drive ardomain_o[1:0] signal when Transmit DMA is accessing the extended buffers (when packet is distributed across multiple buffers). Value After Reset: 0x0
TEC	R/W	[11:8]	0x0	Transmit DMA Extended Packet Buffer This field is used to drive arcache_o[3:0] signal when Transmit DMA is accessing the extended buffers (when packet is distributed across multiple buffers). Value After Reset: 0x0
RESERVED_7_6	R	[7:6]	0x0	Reserved. Value After Reset: 0x0
TDRD	R/W	[5:4]	0x0	Transmit DMA Read Descriptor Domain Control This field is used to drive ardomain_o[1:0] signal when Transmit DMA engines access the

				Descriptor. Value After Reset: 0x0
TDRC	R/W	[3:0]	0x0	Transmit DMA Read Descriptor Cache Control This field is used to drive arcache_o[3:0] signal when Transmit DMA engines access the Descriptor. Value After Reset: 0x0

2.1.7 EQOS_DMA_R_AXI4_RX_AW_ACE_CONTROL

Access Type: RW

Address Offset: 0x1024

Name	Access	Bit Range	Reset value	Description
RESERVED_31_30	R	[31:30]	0x0	Reserved. Value After Reset: 0x0
RDD	R/W	[29:28]	0x0	Receive DMA Buffer Domain Control This field is used to drive the awdomain_o[1:0] signal when Receive DMA is accessing the Buffer when Header and payload are NOT separated. Value After Reset: 0x0
RDC	R/W	[27:24]	0x0	Receive DMA Buffer Cache Control This field is used to drive awcache_o[3:0] signal when Receive DMA is accessing the Buffer when Header and payload are NOT separated. Value After Reset: 0x0
RESERVED_23_22	R	[23:22]	0x0	Reserved. Value After Reset: 0x0
RHD	R/W	[21:20]	0x0	Receive DMA Header Domain Control This field is used to drive awdomain_o[1:0] and signal when Receive DMA is accessing the header Buffer when Header and payload are separated. Value After Reset: 0x0
RHC	R/W	[19:16]	0x0	Receive DMA Header Cache Control This field is used to drive awcache_o[3:0] and signal when Receive DMA is accessing the header

				Buffer when Header and payload are separated. Value After Reset: 0x0
RESERVED_15_14	R	[15:14]	0x0	Reserved. Value After Reset: 0x0
RPD	R/W	[13:12]	0x0	Receive DMA Payload Domain Control This field is used to drive awdomain_o[1:0] signal when Receive DMA is accessing the Payload Buffer when Header and payload are separated. Value After Reset: 0x0
RPC	R/W	[11:8]	0x0	Receive DMA Payload Cache Control This field is used to drive awcache_o[3:0] signal when Receive DMA is accessing the Payload Buffer when Header and payload are separated. Value After Reset: 0x0
RESERVED_7_6	R	[7:6]	0x0	Reserved. Value After Reset: 0x0
RDWD	R/W	[5:4]	0x0	Receive DMA Write Descriptor Domain Control This field is used to drive awdomain_o[1:0] signal when Receive DMA accesses the Descriptor. Value After Reset: 0x0
RDWC	R/W	[3:0]	0x0	Receive DMA Write Descriptor Cache Control This field is used to drive awcache_o[3:0] signal when Receive DMA accesses the Descriptor. Value After Reset: 0x0

2.1.8 EQOS_DMA_R_AXI4_TXRX_AWAR_ACE_CONTROL

Access Type: RW

Address Offset: 0x1028

Name	Access	Bit Range	Reset value	Description
RESERVED_31_23	R	[31:23]	0x0	Reserved. Value After Reset: 0x0
WRP	R/W	[22:20]	0x0	DMA Write Protection control This field is used to drive awprot_m_o[2:0] signal

				on the AXI Write Channel. Value After Reset: 0x0
RESERVED_19	R	[19:19]	0x0	Reserved. Value After Reset: 0x0
RDP	R/W	[18:16]	0x0	DMA Read Protection control This field is used to drive arprot_m_o[2:0] signal during all read requests. Value After Reset: 0x0
RESERVED_15_14	R	[15:14]	0x0	Reserved. Value After Reset: 0x0
RDRD	R/W	[13:12]	0x0	Receive DMA Read Descriptor Domain control This field is used to drive ardomain_o[1:0] signal when Receive DMA engines read the Descriptor. Value After Reset: 0x0
RDRC	R/W	[11:8]	0x0	Receive DMA Read Descriptor Cache control This field is used to drive arcache_o[3:0] signal when Receive DMA engines read the Descriptor. Value After Reset: 0x0
RESERVED_7_6	R	[7:6]	0x0	Reserved. Value After Reset: 0x0
TDWD	R/W	[5:4]	0x0	Transmit DMA Write Descriptor Domain control This field is used to drive awdomain_o[1:0] signal when Transmit DMA write to the Descriptor. Value After Reset: 0x0
TDWC	R/W	[3:0]	0x0	Transmit DMA Write Descriptor Cache control This field is used to drive awcache_o[3:0] signal when Transmit DMA writes to the Descriptor. Value After Reset: 0x0

2.1.9 EQOS_DMA_R_AXI_LPI_ENTRY_INTERVAL

Access Type: RW

Address Offset: 0x1040

Name	Access	Bit Range	Reset value	Description

RESERVED_31_4	R	[31:4]	0x0	Reserved. Value After Reset: 0x0
LPIEI	R/W	[3:0]	0x0	LPI Entry Interval Contains the number of system clock cycles, multiplied by 64, to wait for an activity in the DWC_ether_qos to enter into the AXI low power state 0 indicates 64 clock cycles Value After Reset: 0x0

2.1.10 EQOS_DMA_R_DMA_TBS_CTRL

Access Type: RW

Address Offset: 0x1050

Name	Access	Bit Range	Reset value	Description
FTOS	R/W	[31:8]	0x0	Fetch Time Offset The value in units of 256 nanoseconds, that has to be deducted from the Launch time to compute the Fetch Time. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value. Value After Reset: 0x0
RESERVED_7	R	[7:7]	0x0	Reserved. Value After Reset: 0x0
FGOS	R/W	[6:4]	0x0	Fetch GSN Offset The number GSN slots that must be deducted from the Launch GSN to compute the Fetch GSN. Value valid only when FTOV is set. Value After Reset: 0x0
RESERVED_3_1	**R**	[3:1]	0x0	Reserved. Value After Reset: 0x0
FTOV	R/W	[0:0]	0x0	Fetch Time Offset Valid When set indicates the FTOS field is valid. When not set, indicates the Fetch Offset is not valid and the

				DMA engine can fetch the frames from host memory without any time restrictions.Values: 0x0 (INVALID): Fetch Time Offset is invalid 0x1 (VALID): Fetch Time Offset is valid Value After Reset: 0x0

2.1.11 EQOS_DMA_R_DMA_SAFETY_INTERRUPT_STATUS

Access Type: RW

Address Offset: 0x1080

Name	Access	Bit Range	Reset value	Description
MCSIS	R	[31:31]	0x0	MAC Safety Uncorrectable Interrupt Status Indicates a uncorrectable Safety related Interrupt is set in the MAC module. MAC_DPP_FSM_Interrupt_Status register should be read when this bit is set, to get the cause of the Safety Interrupt in MAC.Values: 0x0 (INACTIVE): MAC Safety Uncorrectable Interrupt Status not detected 0x1 (ACTIVE): MAC Safety Uncorrectable Interrupt Status detected Value After Reset: 0x0
RESERVED_30	R	[30:30]	0x0	Reserved. Value After Reset: 0x0
MSUIS	R	[29:29]	0x0	MTL Safety Uncorrectable error Interrupt Status This bit indicates an uncorrectable error interrupt event in MTL. To get exact cause of the interrupt the software should read the MTL_Safety_Interrupt_Status register.Values: 0x0 (INACTIVE): MTL Safety Uncorrectable error Interrupt Status not detected

				0x1 (ACTIVE): MTL Safety Uncorrectable error Interrupt Status detected Value After Reset: 0x0
MSCIS	R	[28:28]	0x0	MTL Safety Correctable error Interrupt Status This bit indicates a correctable error interrupt event in MTL. To get exact cause of the interrupt the software should read the MTL_Safety_Interrupt_Status register.Values: 0x0 (INACTIVE): MTL Safety Correctable error Interrupt Status not detected 0x1 (ACTIVE): MTL Safety Correctable error Interrupt Status detected Value After Reset: 0x0
RESERVED_27_2	R	[27:2]	0x0	Reserved. Value After Reset: 0x0
DEUIS	R	[1:1]	0x0	DMA ECC Uncorrectable error Interrupt Status This bit indicates an interrupt event in the DMA ECC safety feature. To get the exact cause of the interrupt the application should read the DMA_ECC_Interrupt_Status register.Values: 0x0 (INACTIVE): DMA ECC Uncorrectable error Interrupt Status not detected 0x1 (ACTIVE): DMA ECC Uncorrectable error Interrupt Status detected Value After Reset: 0x0
DECIS	R	[0:0]	0x0	DMA ECC Correctable error Interrupt Status This bit indicates an interrupt event in the DMA ECC

				safety feature. To get the exact cause of the interrupt the application should read the DMA_ECC_Interrupt_Status register.Values: 0x0 (INACTIVE): DMA ECC Correctable error Interrupt Status not detected 0x1 (ACTIVE): DMA ECC Correctable error Interrupt Status detected Value After Reset: 0x0

2.2 EQOS_DMA_CH0

Module Name	EQOS_DMA_CH0
Sub Module Name	
Data Width	32
Address Width	32
Base Address	0x0

2.2.1 EQOS_DMA_CH0_R_DMA_CH(#I)_CONTROL(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x1100

Name	Access	Bit Range	Reset value	Description
RESERVED_31_25	R	[31:25]	0x0	Reserved. Value After Reset: 0x0
SPH	R/W	[24:24]	0x0	Split Headers When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected.Values:

				0x0 (DISABLE): Split Headers feature is disabled 0x1 (ENABLE): Split Headers feature is enabled Value After Reset: 0x0
RESERVED_23_21	R	[23:21]	0x0	Reserved. Value After Reset: 0x0
DSL	R/W	[20:18]	0x0	Descriptor Skip Length This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous. Value After Reset: 0x0
RESERVED_17	R	[17:17]	0x0	Reserved. Value After Reset: 0x0
PBLX8	R/W	[16:16]	0x0	8xPBL mode When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH(#i)_Tx_Control and Bits[21:16] in DMA_CH(#i)_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value.Values: 0x0 (DISABLE): 8xPBL mode is disabled 0x1 (ENABLE): 8xPBL mode is enabled Value After Reset: 0x0
RESERVED_15_14	R	[15:14]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[13:0]	0x0	Reserved Field: Yes

2.2.2 EQOS_DMA_CH0_R_DMA_CH(#I)_TX_CONTROL(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x1104

Name	Access	Bit Range	Reset value	Description
RESERVED_31_29	R	[31:29]	0x0	Reserved. Value After Reset: 0x0
EDSE	R/W	[28:28]	0x0	Enhanced Descriptor Enable When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes.Values: 0x0 (DISABLE): Enhanced Descriptor is disabled 0x1 (ENABLE): Enhanced Descriptor is enabled Value After Reset: 0x0
TQOS	R/W	[27:24]	0x0	Transmit QOS. This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Tx Channel0. Value After Reset: 0x0
RESERVED_23	R	[23:23]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[22:22]	0x0	Reserved Field: Yes
TXPBL	R/W	[21:16]	0x0	Transmit Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the

				following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32. Value After Reset: 0x0
IPBL	R/W	[15:15]	0x0	Ignore PBL Requirement When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL might use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it might block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer.Values: 0x0 (DISABLE): Ignore PBL Requirement is disabled 0x1 (ENABLE): Ignore PBL Requirement is enabled Value After Reset: 0x0
RESERVED	R	[14:12]	0x0	Reserved Field: Yes
RESERVED_11_5	R	[11:5]	0x0	Reserved. Value After Reset: 0x0
OSF	R/W	[4:4]	0x0	Operate on Second Packet

				When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained.Values: 0x0 (DISABLE): Operate on Second Packet disabled 0x1 (ENABLE): Operate on Second Packet enabled Value After Reset: 0x0
RESERVED	R	[3:1]	0x0	Reserved Field: Yes
ST	R/W	[0:0]	0x0	Start or Stop Transmission Command When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program

				DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state.Values: 0x0 (STOP): Stop Transmission Command 0x1 (START): Start Transmission Command Value After Reset: 0x0 Testable: untestable

2.2.3 EQOS_DMA_CH0_R_DMA_CH(#I)_RX_CONTROL(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x1108

Name	Access	Bit Range	Reset value	Description
RPF	R/W	[31:31]	0x0	Rx Packet Flush. When this bit is set to 1, then DWC_ether_qos automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the DWC_ether_qos not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This might in turn cause head-of-line blocking in the corresponding RxQueue. Note: The stopping of packet flow from a Rx DMA Channel to the application by setting RPF works only when there is one-to-one mapping of Rx Queue to Rx DMA channels. In Dynamic mapping mode, setting RPF bit in any DMA_CH(#i)_Rx_Control register might flush packets from unintended Rx Queues which are destined to the stopped Rx DMA

				Channel.Values: 0x0 (DISABLE): Rx Packet Flush is disabled 0x1 (ENABLE): Rx Packet Flush is enabled Value After Reset: 0x0
RESERVED_30_28	R	[30:28]	0x0	Reserved. Value After Reset: 0x0
RQOS	R/W	[27:24]	0x0	Rx AXI4 QOS. This field is used to drive arqos_m_o[3:0] or awqos_m_o[3:0] output signals for all transactions of DMA Rx Channel0. Value After Reset: 0x0
RESERVED_23	R	[23:23]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[22:22]	0x0	Reserved Field: Yes
RXPBL	R/W	[21:16]	0x0	Receive Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ(#i)_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width

				configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32. Value After Reset: 0x0
RESERVED_15	R	[15:15]	0x0	Reserved. Value After Reset: 0x0
RBSZ_13_Y	R/W	[14:4]	0x0	Receive Buffer size High RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_x_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width). Value After Reset: 0x0
RBSZ_X_0	R	[3:1]	0x0	Receive Buffer size Low RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO). Value After Reset: 0x0
SR	R/W	[0:0]	0x0	Start or Stop Receive When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. The DMA tries to acquire descriptor from either of the following positions:

				The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state.Values: 0x0 (STOP): Stop Receive 0x1 (START): Start Receive Value After Reset: 0x0 Testable: untestable

2.2.4 EQOS_DMA_CH0_R_DMA_CH(#I)_TXDESC_LIST_HADDRESS(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x1110

Name	Access	Bit Range	Reset value	Description
RESERVED_31_Y	R	[31:8]	0x0	Reserved. Value After Reset: 0x0
TDESHA	R/W	[7:0]	0x0	Start of Transmit List

				This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list. Value After Reset: 0x0

2.2.5 EQOS_DMA_CH0_R_DMA_CH(#I)_TXDESC_LIST_ADDRESS(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x1114

Name	Access	Bit Range	Reset value	Description
TDESLA	R/W	[31:3]	0x0	Start of Transmit List This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration Value After Reset: 0x0 Testable: untestable
RESERVED_LSB	R	[2:0]	0x0	Reserved. Value After Reset: 0x0

2.2.6 EQOS_DMA_CH0_R_DMA_CH(#I)_RXDESC_LIST_HADDRESS(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x1118

Name	Access	Bit Range	Reset value	Description
RESERVED_31_Y	R	[31:8]	0x0	Reserved. Value After Reset: 0x0
RDESHA	R/W	[7:0]	0x0	Start of Receive List

				This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list. Value After Reset: 0x0

2.2.7 EQOS_DMA_CH0_R_DMA_CH(#I)_RXDESC_LIST_ADDRESS(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x111C

Name	Access	Bit Range	Reset value	Description
RDESLA	R/W	[31:3]	0x0	Start of Receive List This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration Value After Reset: 0x0 Testable: untestable
RESERVED_LSB	R	[2:0]	0x0	Reserved. Value After Reset: 0x0

2.2.8 EQOS_DMA_CH0_R_DMA_CH(#I)_TXDESC_TAIL_POINTER(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x1120

Name	Access	Bit Range	Reset value	Description
TDTP	R/W	[31:3]	0x0	Transmit Descriptor Tail Pointer This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer

				registers. The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration Value After Reset: 0x0
RESERVED_LSB	R	[2:0]	0x0	Reserved. Value After Reset: 0x0

2.2.9 EQOS_DMA_CH0_R_DMA_CH(#I)_RXDESC_TAIL_POINTER(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x1128

Name	Access	Bit Range	Reset value	Description
RDTP	R/W	[31:3]	0x0	Receive Descriptor Tail Pointer This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration Value After Reset: 0x0
RESERVED_LSB	R	[2:0]	0x0	Reserved. Value After Reset: 0x0

2.2.10 EQOS_DMA_CH0_R_DMA_CH(#I)_TXDESC_RING_LENGTH(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x112C

Name	Access	Bit	Reset	Description

		Range	value	
RESERVED_31_10	R	[31:10]	0x0	Reserved. Value After Reset: 0x0
TDRL	R/W	[9:0]	0x0	Transmit Descriptor Ring Length This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. Synopsys recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9. Value After Reset: 0x0

2.2.11 EQOS_DMA_CH0_R_DMA_CH(#I)_RXDESC_RING_LENGTH(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x1130

Name	Access	Bit Range	Reset value	Description
RESERVED_31_10	R	[31:10]	0x0	Reserved. Value After Reset: 0x0
RDRL	R/W	[9:0]	0x0	Receive Descriptor Ring Length This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9. Value After Reset: 0x0

2.2.12 EQOS_DMA_CH0_R_DMA_CH(#I)_INTERRUPT_ENABLE(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x1134

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	

				Reserved. Value After Reset: 0x0
NIE	R/W	[15:15]	0x0	Normal Interrupt Summary Enable When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: Bit 0: Transmit Interrupt Bit 2: Transmit Buffer Unavailable Bit 6: Receive Interrupt Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled.Values: 0x0 (DISABLE): Normal Interrupt Summary is disabled 0x1 (ENABLE): Normal Interrupt Summary is enabled Value After Reset: 0x0
AIE	R/W	[14:14]	0x0	Abnormal Interrupt Summary Enable When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: Bit 1: Transmit Process Stopped Bit 7: Rx Buffer Unavailable Bit 8: Receive Process Stopped Bit 9: Receive Watchdog Timeout Bit 10: Early Transmit Interrupt

				Bit 12: Fatal Bus Error Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled.Values: 0x0 (DISABLE): Abnormal Interrupt Summary is disabled 0x1 (ENABLE): Abnormal Interrupt Summary is enabled Value After Reset: 0x0
CDEE	R/W	[13:13]	0x0	Context Descriptor Error Enable When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled.Values: 0x0 (DISABLE): Context Descriptor Error is disabled 0x1 (ENABLE): Context Descriptor Error is enabled Value After Reset: 0x0
FBEE	R/W	[12:12]	0x0	Fatal Bus Error Enable When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled.Values: 0x0 (DISABLE): Fatal Bus Error is disabled 0x1 (ENABLE): Fatal Bus Error is enabled Value After Reset: 0x0

ERIE	R/W	[11:11]	0x0	Early Receive Interrupt Enable When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled.Values: 0x0 (DISABLE): Early Receive Interrupt is disabled 0x1 (ENABLE): Early Receive Interrupt is enabled Value After Reset: 0x0
ETIE	R/W	[10:10]	0x0	Early Transmit Interrupt Enable When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled.Values: 0x0 (DISABLE): Early Transmit Interrupt is disabled 0x1 (ENABLE): Early Transmit Interrupt is enabled Value After Reset: 0x0
RWTE	R/W	[9:9]	0x0	Receive Watchdog Timeout Enable When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled.Values: 0x0 (DISABLE): Receive Watchdog Timeout is disabled 0x1 (ENABLE): Receive Watchdog Timeout is enabled

				Value After Reset: 0x0
RSE	R/W	[8:8]	0x0	Receive Stopped Enable When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled.Values: 0x0 (DISABLE): Receive Stopped is disabled 0x1 (ENABLE): Receive Stopped is enabled Value After Reset: 0x0
RBUE	R/W	[7:7]	0x0	Receive Buffer Unavailable Enable When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled.Values: 0x0 (DISABLE): Receive Buffer Unavailable is disabled 0x1 (ENABLE): Receive Buffer Unavailable is enabled Value After Reset: 0x0
RIE	R/W	[6:6]	0x0	Receive Interrupt Enable When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled.Values: 0x0 (DISABLE): Receive Interrupt is disabled 0x1 (ENABLE): Receive Interrupt is enabled Value After Reset: 0x0
RESERVED_5_3	R	[5:3]	0x0	

				Reserved. Value After Reset: 0x0
TBUE	R/W	[2:2]	0x0	Transmit Buffer Unavailable Enable When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled.Values: 0x0 (DISABLE): Transmit Buffer Unavailable is disabled 0x1 (ENABLE): Transmit Buffer Unavailable is enabled Value After Reset: 0x0
TXSE	R/W	[1:1]	0x0	Transmit Stopped Enable When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled.Values: 0x0 (DISABLE): Transmit Stopped is disabled 0x1 (ENABLE): Transmit Stopped is enabled Value After Reset: 0x0
TIE	R/W	[0:0]	0x0	Transmit Interrupt Enable When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled.Values: 0x0 (DISABLE): Transmit Interrupt is disabled 0x1 (ENABLE): Transmit Interrupt is enabled Value After Reset: 0x0

2.2.13 EQOS_DMA_CH0_R_DMA_CH(#I)_RX_INTERRUPT_WATCHDOG_TIMER(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x1138

Name	Access	Bit Range	Reset value	Description
RESERVED_31_18	R	[31:18]	0x0	Reserved. Value After Reset: 0x0
RWTU	R/W	[17:16]	0x0	Receive Interrupt Watchdog Timer Count Units This fields indicates the number of system clock cycles corresponding to one unit in RWT field. 2'b00: 256 2'b01: 512 2'b10: 1024 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles. Value After Reset: 0x0 Testable: untestable
RESERVED_15_8	R	[15:8]	0x0	Reserved. Value After Reset: 0x0
RWT	R/W	[7:0]	0x0	Receive Interrupt Watchdog Timer Count This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set

				and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet. Value After Reset: 0x0 Testable: untestable

2.2.14 EQOS_DMA_CH0_R_DMA_CH(#I)_SLOT_FUNCTION_CONTROL_STATUS(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x113C

Name	Access	Bit Range	Reset value	Description
RESERVED_31_20	R	[31:20]	0x0	Reserved. Value After Reset: 0x0
RSN	R	[19:16]	0x0	Reference Slot Number This field gives the current value of the reference slot number in the DMA. It is used for slot comparison. Value After Reset: 0x0 Testable: untestable
SIV	R/W	[15:4]	0x7c	Slot Interval Value This field controls the period of the slot interval in which the TxDMA fetches the scheduled packets. A value of 0 specifies the slot interval of 1 us while the maximum value 4095 specifies the slot interval of 4096us. The default/reset value is 0x07C which corresponds to slot interval of 125us Value After Reset: 0x7c
RESERVED_3_2	R	[3:2]	0x0	Reserved. Value After Reset: 0x0
ASC	R/W	[1:1]	0x0	Advance Slot Check When set, this bit enables the DMA to fetch the data from the buffer when the slot number (SLOTNUM) programmed in the Tx descriptor is equal to the reference slot number given in the RSN field

				or ahead of the reference slot number by up to two slots This bit is applicable only when the ESC bit is set.Values: 0x0 (DISABLE): Advance Slot Check is disabled 0x1 (ENABLE): Advance Slot Check is enabled Value After Reset: 0x0
ESC	R/W	[0:0]	0x0	Enable Slot Comparison When set, this bit enables the checking of the slot numbers programmed in the Tx descriptor with the current reference given in the RSN field. The DMA fetches the data from the corresponding buffer only when the slot number is equal to the reference slot number or ahead of the reference slot number by one slot When reset, this bit disables the checking of the slot numbers. The DMA fetches the data immediately after the descriptor is processed. Note: The UFO (UDP Fragmentation over IPv4)/TSO/USO should not be enabled along with TBS/AVB Slot number check. The UFO/TSO/USO involves multiple packets/segments/fragments transmission for single packet received from application and the slot number check are applicable for fetching of only first segment/fragment. As a result it might be difficult for software to specify slot number for subsequent packets.Values: 0x0 (DISABLE): Slot Comparison is disabled

				0x1 (ENABLE): Slot Comparison is enabled Value After Reset: 0x0

2.2.15 EQOS_DMA_CH0_R_DMA_CH(#I)_CURRENT_APP_TXDESC(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x1144

Name	Access	Bit Range	Reset value	Description
CURTDESAPTR	R	[31:0]	0x0	Application Transmit Descriptor Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset. Value After Reset: 0x0

2.2.16 EQOS_DMA_CH0_R_DMA_CH(#I)_CURRENT_APP_RXDESC(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x114C

Name	Access	Bit Range	Reset value	Description
CURRDESAPTR	R	[31:0]	0x0	Application Receive Descriptor Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset. Value After Reset: 0x0

2.2.17 EQOS_DMA_CH0_R_DMA_CH(#I)_CURRENT_APP_TXBUFFER_H(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x1150

Name	Access	Bit Range	Reset value	Description
RESERVED_31_Y	R	[31:8]	0x0	Reserved. Value After Reset: 0x0
CURTBUFAPTRH	R	[7:0]	0x0	Application Transmit Buffer Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset. Value After Reset: 0x0

2.2.18 EQOS_DMA_CH0_R_DMA_CH(#I)_CURRENT_APP_TXBUFFER(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x1154

Name	Access	Bit Range	Reset value	Description
CURTBUFAPTR	R	[31:0]	0x0	Application Transmit Buffer Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset. Value After Reset: 0x0

2.2.19 EQOS_DMA_CH0_R_DMA_CH(#I)_CURRENT_APP_RXBUFFER_H(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x1158

Name	Access	Bit Range	Reset value	Description
RESERVED_31_Y	R	[31:8]	0x0	Reserved. Value After Reset: 0x0
CURRBUFAPTRH	R	[7:0]	0x0	Application Receive Buffer Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset. Value After Reset: 0x0

2.2.20 EQOS_DMA_CH0_R_DMA_CH(#I)_CURRENT_APP_RXBUFFER(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x115C

Name	Access	Bit Range	Reset value	Description
CURRBUFAPTR	R	[31:0]	0x0	Application Receive Buffer Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset. Value After Reset: 0x0

2.2.21 EQOS_DMA_CH0_R_DMA_CH(#I)_STATUS(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x1160

Name	Access	Bit Range	Reset value	Description

RESERVED_31_22	R	[31:22]	0x0	Reserved. Value After Reset: 0x0
REB	R	[21:19]	0x0	Rx DMA Error Bits This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. Bit 21 1'b1: Error during data transfer by Rx DMA 1'b0: No Error during data transfer by Rx DMA Bit 20 1'b1: Error during descriptor access 1'b0: Error during data buffer access Bit 19 1'b1: Error during read transfer 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt. Value After Reset: 0x0 Testable: untestable
TEB	R	[18:16]	0x0	Tx DMA Error Bits This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. Bit 18 1'b1: Error during data transfer by Tx DMA 1'b0: No Error during data transfer by Tx DMA

				Bit 17 1'b1: Error during descriptor access 1'b0: Error during data buffer access Bit 16 1'b1: Error during read transfer 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt. Value After Reset: 0x0 Testable: untestable
NIS	R/W	[15:15]	0x0	Normal Interrupt Summary Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: Bit 0: Transmit Interrupt Bit 2: Transmit Buffer Unavailable Bit 6: Receive Interrupt Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.Values: 0x0 (INACTIVE): Normal Interrupt Summary status not detected

				0x1 (ACTIVE): Normal Interrupt Summary status detected Value After Reset: 0x0 Testable: untestable
AIS	R/W	[14:14]	0x0	Abnormal Interrupt Summary Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: Bit 1: Transmit Process Stopped Bit 7: Receive Buffer Unavailable Bit 8: Receive Process Stopped Bit 10: Early Transmit Interrupt Bit 12: Fatal Bus Error Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.Values: 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected 0x1 (ACTIVE): Abnormal Interrupt Summary status detected Value After Reset: 0x0

				Testable: untestable
CDE	R/W	[13:13]	0x0	Context Descriptor Error This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.Values: 0x0 (INACTIVE): Context Descriptor Error status not detected 0x1 (ACTIVE): Context Descriptor Error status detected Value After Reset: 0x0 Testable: untestable
FBE	R/W	[12:12]	0x0	Fatal Bus Error This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.Values: 0x0 (INACTIVE): Fatal Bus Error status not detected 0x1 (ACTIVE): Fatal Bus Error status detected Value After Reset: 0x0 Testable: untestable
ERI	R/W	[11:11]	0x0	Early Receive Interrupt

				This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.Values: 0x0 (INACTIVE): Early Receive Interrupt status not detected 0x1 (ACTIVE): Early Receive Interrupt status detected Value After Reset: 0x0 Testable: untestable
ETI	R/W	[10:10]	0x0	Early Transmit Interrupt This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.Values: 0x0 (INACTIVE): Early Transmit Interrupt status not detected

				0x1 (ACTIVE): Early Transmit Interrupt status detected Value After Reset: 0x0 Testable: untestable
RWT	R/W	[9:9]	0x0	Receive Watchdog Timeout This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received.Values: 0x0 (INACTIVE): Receive Watchdog Timeout status not detected 0x1 (ACTIVE): Receive Watchdog Timeout status detected Value After Reset: 0x0 Testable: untestable
RPS	R/W	[8:8]	0x0	Receive Process Stopped This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.Values: 0x0 (INACTIVE): Receive Process Stopped status not detected 0x1 (ACTIVE): Receive Process Stopped status detected Value After Reset: 0x0 Testable: untestable
RBU	R/W	[7:7]	0x0	Receive Buffer Unavailable This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot

				acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.Values: 0x0 (INACTIVE): Receive Buffer Unavailable status not detected 0x1 (ACTIVE): Receive Buffer Unavailable status detected Value After Reset: 0x0 Testable: untestable
RI	R/W	[6:6]	0x0	Receive Interrupt This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.Values: 0x0 (INACTIVE): Receive Interrupt status not detected 0x1 (ACTIVE): Receive Interrupt status detected Value After Reset: 0x0 Testable: untestable

RESERVED_5_3	R	[5:3]	0x0	Reserved. Value After Reset: 0x0
TBU	R/W	[2:2]	0x0	Transmit Buffer Unavailable This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.Values: 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected 0x1 (ACTIVE): Transmit Buffer Unavailable status detected Value After Reset: 0x0 Testable: untestable
TPS	R/W	[1:1]	0x0	Transmit Process Stopped This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.Values: 0x0 (INACTIVE): Transmit Process Stopped status not detected 0x1 (ACTIVE): Transmit Process Stopped status detected

				Value After Reset: 0x0 Testable: untestable
TI	R/W	[0:0]	0x0	Transmit Interrupt This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.Values: 0x0 (INACTIVE): Transmit Interrupt status not detected 0x1 (ACTIVE): Transmit Interrupt status detected Value After Reset: 0x0 Testable: untestable

2.2.22 EQOS_DMA_CH0_R_DMA_CH(#I)_MISS_FRAME_CNT(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x1164

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
MFCO	R	[15:15]	0x0	Overflow status of the MFC Counter When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): Miss Frame Counter overflow not occurred

				0x1 (ACTIVE): Miss Frame Counter overflow occurred Value After Reset: 0x0
RESERVED_14_11	R	[14:11]	0x0	Reserved. Value After Reset: 0x0
MFC	R	[10:0]	0x0	Dropped Packet Counters This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programing RPF field in DMA_CH${i}_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. Value After Reset: 0x0

2.2.23 EQOS_DMA_CH0_R_DMA_CH(#I)_RX_ERI_CNT(FORI=0;I<=3)

Access Type: RW

Address Offset: (0x0080*i)+0x116C

Name	Access	Bit Range	Reset value	Description
RESERVED_31_12	R	[31:12]	0x0	Reserved. Value After Reset: 0x0
ECNT	R	[11:0]	0x0	ERI Counter When ERIC bit of DMA_CH(#i)_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter is reset at the start of new packet. Value After Reset: 0x0

2.3 EQOS_MAC

Module Name	EQOS_MAC
Sub Module Name	
Data Width	32

Address Width	32
Base Address	0x0

2.3.1 EQOS_MAC_R_MAC_CONFIGURATION

Access Type: RW

Address Offset: 0x0

Name	Access	Bit Range	Reset value	Description
RESERVED	R	[31:31]	0x0	Reserved Field: Yes
SARC	R/W	[30:28]	0x0	Source Address Insertion or Replacement Control This field controls the source address insertion or replacement for all transmitted packets. Bit 30 specifies which MAC Address register (0 or 1) is used for source address insertion or replacement based on the values of Bits[29:28]: 2'b0x: The mti_sa_ctrl_i and ati_sa_ctrl_i input signals control the SA field generation. 2'b10: If Bit 30 is set to 0, the MAC inserts the content of the MAC Address 0 registers in the SA field of all transmitted packets. If Bit 30 is set to 1 and the Enable MAC Address Register 1 option is selected while configuring the core, the MAC inserts the content of the MAC Address 1 registers in the SA field of all transmitted packets. 2'b11: If Bit 30 is set to 0, the MAC replaces the content of the MAC Address 0 registers in the SA field of all transmitted packets. If Bit 30 is set to 1 and the MAC Address Register 1 is enabled, the MAC replaces the content of the MAC Address 1 registers in the SA field of all transmitted packets.

				Note: Changes to this field take effect only on the start of a packet. If you write to this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value. Values: 0x0 (SA_CTRL_IN): mti_sa_ctrl_i and ati_sa_ctrl_i input signals control the SA field generation 0x2 (MAC0_INS_SA): Contents of MAC Addr-0 inserted in SA field 0x3 (MAC0_REP_SA): Contents of MAC Addr-0 replaces SA field 0x6 (MAC1_INS_SA): Contents of MAC Addr-1 inserted in SA field 0x7 (MAC1_REP_SA): Contents of MAC Addr-1 replaces SA field Value After Reset: 0x0
IPC	R/W	[27:27]	0x0	Checksum Offload When set, this bit enables the IPv4 header checksum checking and IPv4 or IPv6 TCP, UDP, or ICMP payload checksum checking. When this bit is reset, the COE function in the receiver is disabled. The Layer 3 and Layer 4 Packet Filter and Enable Split Header features automatically selects the IPC Full Checksum Offload Engine on the Receive side. When any of these features are enabled, you must set the IPC bit.Values: 0x0 (DISABLE): IP header/payload checksum checking is disabled 0x1 (ENABLE): IP header/payload checksum checking is enabled

				Value After Reset: 0x0
IPG	R/W	[26:24]	0x0	Inter-Packet Gap These bits control the minimum IPG between packets during transmission. This range of minimum IPG is valid in full-duplex mode. In the half-duplex mode, the minimum IPG can be configured only for 64-bit times (IPG = 100). Lower values are not considered. When a JAM pattern is being transmitted because of backpressure activation, the MAC does not consider the minimum IPG. The above function (IPG less than 96 bit times) is valid only when EIPGEN bit in MAC_Ext_Configuration register is reset. When EIPGEN is set, then the minimum IPG (greater than 96 bit times) is controlled as per the description given in EIPG field in MAC_Ext_Configuration register.Values: 0x0 (IPG96): 96 bit times IPG 0x1 (IPG88): 88 bit times IPG 0x2 (IPG80): 80 bit times IPG 0x3 (IPG72): 72 bit times IPG 0x4 (IPG64): 64 bit times IPG 0x5 (IPG56): 56 bit times IPG 0x6 (IPG48): 48 bit times IPG 0x7 (IPG40): 40 bit times IPG Value After Reset: 0x0
GPSLCE	R/W	[23:23]	0x0	Giant Packet Size Limit Control Enable When this bit is set, the MAC considers the value in

				GPSL field in MAC_Ext_Configuration register to declare a received packet as Giant packet. This field must be programmed to more than 1,518 bytes. Otherwise, the MAC considers 1,518 bytes as giant packet limit. When this bit is reset, the MAC considers a received packet as Giant packet when its size is greater than 1,518 bytes (1522 bytes for tagged packet). The watchdog timeout limit, Jumbo Packet Enable and 2K Packet Enable have higher precedence over this bit, that is the MAC considers a received packet as Giant packet when its size is greater than 9,018 bytes (9,022 bytes for tagged packet) with Jumbo Packet Enabled and greater than 2,000 bytes with 2K Packet Enabled. The watchdog timeout, if enabled, terminates the received packet when watchdog limit is reached. Therefore, the programmed giant packet limit should be less than the watchdog limit to get the giant packet status.Values: 0x0 (DISABLE): Giant Packet Size Limit Control is disabled 0x1 (ENABLE): Giant Packet Size Limit Control is enabled Value After Reset: 0x0
S2KP	R/W	[22:22]	0x0	IEEE 802.3as Support for 2K Packets When this bit is set, the MAC considers all packets with up to 2,000 bytes length as normal packets. When the JE bit is not set, the MAC considers all received packets of size more than 2K bytes as Giant packets. When this bit is reset and the JE bit is not set, the MAC considers all received packets of size more than 1,518 bytes (1,522 bytes for tagged) as giant packets. For more information about how the setting of this bit and the JE bit impact the Giant packet status, see the Table, Gaint Packet Status based on S2KP and JE Bits. Note: When the JE bit is set, setting this bit has no effect on the giant packet status.Values:

				0x0 (DISABLE): Support upto 2K packet is disabled 0x1 (ENABLE): Support upto 2K packet is Enabled Value After Reset: 0x0
CST	R/W	[21:21]	0x0	CRC stripping for Type packets When this bit is set, the last four bytes (FCS) of all packets of Ether type (type field greater than 1,536) are stripped and dropped before forwarding the packet to the application. Note: For information about how the settings of the ACS bit and this bit impact the packet length, see the Table, Packet Length based on the CST and ACS Bits.Values: 0x0 (DISABLE): CRC stripping for Type packets is disabled 0x1 (ENABLE): CRC stripping for Type packets is enabled Value After Reset: 0x0
ACS	R/W	[20:20]	0x0	Automatic Pad or CRC Stripping When this bit is set, the MAC strips the Pad or FCS field on the incoming packets only if the value of the length field is less than 1,536 bytes. All received packets with length field greater than or equal to 1,536 bytes are passed to the application without stripping the Pad or FCS field. When this bit is reset, the MAC passes all incoming packets to the application, without any modification. Note: For information about how the settings of CST bit and this bit impact the packet length, see the Table, Packet Length based on the CST and ACS Bit .Values: 0x0 (DISABLE): Automatic Pad or CRC Stripping is disabled 0x1 (ENABLE): Automatic Pad or CRC Stripping is

				enabled Value After Reset: 0x0
WD	R/W	[19:19]	0x0	Watchdog Disable When this bit is set, the MAC disables the watchdog timer on the receiver. The MAC can receive packets of up to 16,383 bytes. When this bit is reset, the MAC does not allow more than 2,048 bytes (10,240 if JE is set high) of the packet being received. The MAC cuts off any bytes received after 2,048 bytes.Values: 0x0 (ENABLE): Watchdog is enabled 0x1 (DISABLE): Watchdog is disabled Value After Reset: 0x0
RESERVED	R	[18:18]	0x0	Reserved Field: Yes
JD	R/W	[17:17]	0x0	Jabber Disable When this bit is set, the MAC disables the jabber timer on the transmitter. The MAC can transfer packets of up to 16,383 bytes. When this bit is reset, if the application sends more than 2,048 bytes of data (10,240 if JE is set high) during transmission, the MAC does not send rest of the bytes in that packet.Values: 0x0 (ENABLE): Jabber is enabled 0x1 (DISABLE): Jabber is disabled Value After Reset: 0x0
JE	R/W	[16:16]	0x0	Jumbo Packet Enable When this bit is set, the MAC allows jumbo packets of 9,018 bytes (9,022 bytes for VLAN tagged packets) without reporting a giant packet error in the Rx packet

				status.Values: 0x0 (DISABLE): Jumbo packet is disabled 0x1 (ENABLE): Jumbo packet is enabled Value After Reset: 0x0
PS	R/W	[15:15]	0x0	Port Select This bit selects the Ethernet line speed. This bit, along with Bit 14, selects the exact line speed. In the 10/100 Mbps-only (always 1) or 1000 Mbps-only (always 0) configurations, this bit is read-only (RO) with appropriate value. In default 10/100/1000 Mbps configurations, this bit is read-write (R/W). The mac_speed_o[1] signal reflects the value of this bit.Values: 0x0 (M_1000_2500M): For 1000 or 2500 Mbps operations 0x1 (M_10_100M): For 10 or 100 Mbps operations Value After Reset: 0x0
FES	R/W	[14:14]	0x0	Speed This bit selects the speed mode. The mac_speed_o[0] signal reflects the value of this bit.Values: 0x0 (M_10_1000M): 10 Mbps when PS bit is 1 and 1 Gbps when PS bit is 0 0x1 (M_100_2500M): 100 Mbps when PS bit is 1 and 2.5 Gbps when PS bit is 0 Value After Reset: 0x0
DM	R	[13:13]	0x1	Duplex Mode When this bit is set, the MAC operates in the

				full-duplex mode in which it can transmit and receive simultaneously. This bit is RO with default value of 1'b1 in the full-duplex-only configurations.Values: 0x0 (HDUPLX): Half-duplex mode 0x1 (FDUPLX): Full-duplex mode Value After Reset: 0x1
LM	R/W	[12:12]	0x0	Loopback Mode When this bit is set, the MAC operates in the loopback mode at GMII or MII. The (G)MII Rx clock input (clk_rx_i) is required for the loopback to work properly. This is because the Tx clock is not internally looped back.Values: 0x0 (DISABLE): Loopback is disabled 0x1 (ENABLE): Loopback is enabled Value After Reset: 0x0
ECRSFD	R/W	[11:11]	0x0	Enable Carrier Sense Before Transmission in Full-Duplex Mode When this bit is set, the MAC transmitter checks the CRS signal before packet transmission in the full-duplex mode. The MAC starts the transmission only when the CRS signal is low. When this bit is reset, the MAC transmitter ignores the status of the CRS signal.Values: 0x0 (DISABLE): ECRSFD is disabled 0x1 (ENABLE): ECRSFD is enabled Value After Reset: 0x0
RESERVED	R	[10:8]	0x0	Reserved Field: Yes
RESERVED_7	R	[7:7]	0x0	

				Reserved. Value After Reset: 0x0
RESERVED	R	[6:4]	0x0	Reserved Field: Yes
PRELEN	R/W	[3:2]	0x0	Preamble Length for Transmit packets These bits control the number of preamble bytes that are added to the beginning of every Tx packet. The preamble reduction occurs only when the MAC is operating in the full-duplex mode.Values: 0x0 (M_7BYTES): 7 bytes of preamble 0x1 (M_5BYTES): 5 bytes of preamble 0x2 (M_3BYTES): 3 bytes of preamble 0x3 (RESERVED): Reserved Value After Reset: 0x0
TE	R/W	[1:1]	0x0	Transmitter Enable When this bit is set, the Tx state machine of the MAC is enabled for transmission on the GMII or MII interface. When this bit is reset, the MAC Tx state machine is disabled after it completes the transmission of the current packet. The Tx state machine does not transmit any more packets.Values: 0x0 (DISABLE): Transmitter is disabled 0x1 (ENABLE): Transmitter is enabled Value After Reset: 0x0
RE	R/W	[0:0]	0x0	Receiver Enable When this bit is set, the Rx state machine of the MAC is enabled for receiving packets from the GMII or MII interface. When this bit is reset, the MAC Rx state machine is disabled after it completes the reception of the current packet. The Rx state machine does not

				receive any more packets from the GMII or MII interface.Values: 0x0 (DISABLE): Receiver is disabled 0x1 (ENABLE): Receiver is enabled Value After Reset: 0x0

2.3.2 EQOS_MAC_R_MAC_EXT_CONFIGURATION

Access Type: RW

Address Offset: 0x4

Name	Access	Bit Range	Reset value	Description
RESERVED	R	[31:31]	0x0	Reserved Field: Yes
RESERVED_30	R	[30:30]	0x0	Reserved. Value After Reset: 0x0
EIPG	R/W	[29:25]	0x0	Extended Inter-Packet Gap The value in this field is applicable when the EIPGEN bit is set. This field (as Most Significant bits), along with IPG field in MAC_Configuration register, gives the minimum IPG greater than 96 bit times in steps of 8 bit times: {EIPG, IPG} 8'h00 - 104 bit times 8'h01 - 112 bit times 8'h02 - 120 bit times ---------- 8'hFF - 2144 bit times Value After Reset: 0x0
EIPGEN	R/W	[24:24]	0x0	Extended Inter-Packet Gap Enable When this bit is set, the MAC interprets EIPG field and IPG field in MAC_Configuration register together as minimum IPG greater than 96 bit times in steps of 8 bit times. When this bit is reset, the MAC ignores EIPG field and interprets IPG field in MAC_Configuration register as minimum IPG less than or equal to 96 bit times in steps of 8 bit times.

				Note: The extended Inter-Packet Gap feature must be enabled when operating in Full-Duplex mode only. There might be undesirable effects on back-pressure function and frame transmission if it is enabled in Half-Duplex mode.Values: 0x0 (DISABLE): Extended Inter-Packet Gap is disabled 0x1 (ENABLE): Extended Inter-Packet Gap is enabled Value After Reset: 0x0
RESERVED_23	R	[23:23]	0x0	Reserved. Value After Reset: 0x0
HDSMS	R/W	[22:20]	0x0	Maximum Size for Splitting the Header Data These bits indicate the maximum header size allowed for splitting the header data in the received packet.Values: 0x0 (M_64BYTES): Maximum Size for Splitting the Header Data is 64 bytes 0x1 (M_128BYTES): Maximum Size for Splitting the Header Data is 128 bytes 0x2 (M_256BYTES): Maximum Size for Splitting the Header Data is 256 bytes 0x3 (M_512BYTES): Maximum Size for Splitting the Header Data is 512 bytes 0x4 (M_1024BYTES): Maximum Size for Splitting the Header Data is 1024 bytes 0x5 (RSVD): Reserved Value After Reset: 0x0
RESERVED	R	[19:19]	0x0	Reserved Field: Yes

USP	R/W	[18:18]	0x0	Unicast Slow Protocol Packet Detect When this bit is set, the MAC detects the Slow Protocol packets with unicast address of the station specified in the MAC_Address0_High and MAC_Address0_Low registers. The MAC also detects the Slow Protocol packets with the Slow Protocols multicast address (01-80-C2-00-00-02). When this bit is reset, the MAC detects only Slow Protocol packets with the Slow Protocol multicast address specified in the IEEE 802.3-2015, Section 5.Values: 0x0 (DISABLE): Unicast Slow Protocol Packet Detection is disabled 0x1 (ENABLE): Unicast Slow Protocol Packet Detection is enabled Value After Reset: 0x0
SPEN	R/W	[17:17]	0x0	Slow Protocol Detection Enable When this bit is set, MAC processes the Slow Protocol packets (Ether Type 0x8809) and provides the Slow Protocol Sub-Type and Code fields in Rx status. When this bit is reset, the MAC forwards all error-free Slow Protocol packets to the application. The MAC considers such packets as normal Type packets.Values: 0x0 (DISABLE): Slow Protocol Detection is disabled 0x1 (ENABLE): Slow Protocol Detection is enabled Value After Reset: 0x0
DCRCC	R/W	[16:16]	0x0	Disable CRC Checking for Received Packets When this bit is set, the MAC receiver does not

				check the CRC field in the received packets. When this bit is reset, the MAC receiver always checks the CRC field in the received packets.Values: 0x0 (ENABLE): CRC Checking is enabled 0x1 (DISABLE): CRC Checking is disabled Value After Reset: 0x0
RESERVED_15_14	R	[15:14]	0x0	Reserved. Value After Reset: 0x0
GPSL	R/W	[13:0]	0x0	Giant Packet Size Limit If the received packet size is greater than the value programmed in this field in units of bytes, the MAC declares the received packet as Giant packet. The value programmed in this field must be greater than or equal to 1,518 bytes. Any other programmed value is considered as 1,518 bytes. For VLAN tagged packets, the MAC adds 4 bytes to the programmed value. When the Enable Double VLAN Processing option is selected, the MAC adds 8 bytes to the programmed value for double VLAN tagged packets. The value in this field is applicable when the GPSLCE bit is set in MAC_Configuration register. Value After Reset: 0x0

2.3.3 EQOS_MAC_R_MAC_PACKET_FILTER

Access Type: RW

Address Offset: 0x8

Name	Access	Bit Range	Reset value	Description
RA	R/W	[31:31]	0x0	Receive All When this bit is set, the MAC Receiver module passes all received packets to the application, irrespective of whether they pass the address filter or not. The result of the SA or DA filtering is updated (pass or fail) in the corresponding bit in the Rx Status Word.

				When this bit is reset, the Receiver module passes only those packets to the application that pass the SA or DA address filter.Values: 0x0 (DISABLE): Receive All is disabled 0x1 (ENABLE): Receive All is enabled Value After Reset: 0x0
RESERVED_30_22	R	[30:22]	0x0	Reserved. Value After Reset: 0x0
DNTU	R/W	[21:21]	0x0	Drop Non-TCP/UDP over IP Packets When this bit is set, the MAC drops the non-TCP or UDP over IP packets. The MAC forward only those packets that are processed by the Layer 4 filter. When this bit is reset, the MAC forwards all non-TCP or UDP over IP packets.Values: 0x0 (FWD): Forward Non-TCP/UDP over IP Packets 0x1 (DROP): Drop Non-TCP/UDP over IP Packets Value After Reset: 0x0
IPFE	R/W	[20:20]	0x0	Layer 3 and Layer 4 Filter Enable When this bit is set, the MAC drops packets that do not match the enabled Layer 3 and Layer 4 filters. If Layer 3 or Layer 4 filters are not enabled for matching, this bit does not have any effect. When this bit is reset, the MAC forwards all packets irrespective of the match status of the Layer 3 and Layer 4 fields.Values: 0x0 (DISABLE): Layer 3 and Layer 4 Filters are disabled 0x1 (ENABLE): Layer 3 and Layer 4 Filters are enabled

				Value After Reset: 0x0
RESERVED_19_17	R	[19:17]	0x0	Reserved. Value After Reset: 0x0
VTFE	R/W	[16:16]	0x0	VLAN Tag Filter Enable When this bit is set, the MAC drops the VLAN tagged packets that do not match the VLAN Tag. When this bit is reset, the MAC forwards all packets irrespective of the match status of the VLAN Tag.Values: 0x0 (DISABLE): VLAN Tag Filter is disabled 0x1 (ENABLE): VLAN Tag Filter is enabled Value After Reset: 0x0
RESERVED_15_11	R	[15:11]	0x0	Reserved. Value After Reset: 0x0
HPF	R/W	[10:10]	0x0	Hash or Perfect Filter When this bit is set, the address filter passes a packet if it matches either the perfect filtering or hash filtering as set by the HMC or HUC bit. When this bit is reset and the HUC or HMC bit is set, the packet is passed only if it matches the Hash filter.Values: 0x0 (DISABLE): Hash or Perfect Filter is disabled 0x1 (ENABLE): Hash or Perfect Filter is enabled Value After Reset: 0x0
SAF	R/W	[9:9]	0x0	Source Address Filter Enable When this bit is set, the MAC compares the SA field of the received packets with the values

				programmed in the enabled SA registers. If the comparison fails, the MAC drops the packet. When this bit is reset, the MAC forwards the received packet to the application with updated SAF bit of the Rx Status depending on the SA address comparison. Note: According to the IEEE specification, Bit 47 of the SA is reserved. However, in DWC_ether_qos, the MAC compares all 48 bits. The software driver should take this into consideration while programming the MAC address registers for SA.Values: 0x0 (DISABLE): SA Filtering is disabled 0x1 (ENABLE): SA Filtering is enabled Value After Reset: 0x0
SAIF	R/W	[8:8]	0x0	SA Inverse Filtering When this bit is set, the Address Check block operates in the inverse filtering mode for SA address comparison. If the SA of a packet matches the values programmed in the SA registers, it is marked as failing the SA Address filter. When this bit is reset, if the SA of a packet does not match the values programmed in the SA registers, it is marked as failing the SA Address filter.Values: 0x0 (DISABLE): SA Inverse Filtering is disabled 0x1 (ENABLE): SA Inverse Filtering is enabled Value After Reset: 0x0
PCF	R/W	[7:6]	0x0	Pass Control Packets These bits control the forwarding of all control packets (including unicast and multicast Pause packets).Values:

				0x0 (FLTR_ALL): MAC filters all control packets from reaching the application 0x1 (FW_XCPT_PAU): MAC forwards all control packets except Pause packets to the application even if they fail the Address filter 0x2 (FW_ALL): MAC forwards all control packets to the application even if they fail the Address filter 0x3 (FW_PASS): MAC forwards the control packets that pass the Address filter Value After Reset: 0x0
DBF	R/W	[5:5]	0x0	Disable Broadcast Packets When this bit is set, the AFM module blocks all incoming broadcast packets. In addition, it overrides all other filter settings. When this bit is reset, the AFM module passes all received broadcast packets.Values: 0x0 (ENABLE): Enable Broadcast Packets 0x1 (DISABLE): Disable Broadcast Packets Value After Reset: 0x0
PM	R/W	[4:4]	0x0	Pass All Multicast When this bit is set, it indicates that all received packets with a multicast destination address (first bit in the destination address field is '1') are passed. When this bit is reset, filtering of multicast packet depends on HMC bit.Values: 0x0 (DISABLE): Pass All Multicast is disabled 0x1 (ENABLE): Pass All Multicast is enabled

				Value After Reset: 0x0
DAIF	R/W	[3:3]	0x0	DA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast packets. When this bit is reset, normal filtering of packets is performed.Values: 0x0 (DISABLE): DA Inverse Filtering is disabled 0x1 (ENABLE): DA Inverse Filtering is enabled Value After Reset: 0x0
HMC	R/W	[2:2]	0x0	Hash Multicast When this bit is set, the MAC performs the destination address filtering of received multicast packets according to the hash table. When this bit is reset, the MAC performs the perfect destination address filtering for multicast packets, that is, it compares the DA field with the values programmed in DA registers.Values: 0x0 (DISABLE): Hash Multicast is disabled 0x1 (ENABLE): Hash Multicast is enabled Value After Reset: 0x0
HUC	R/W	[1:1]	0x0	Hash Unicast When this bit is set, the MAC performs the destination address filtering of unicast packets according to the hash table. When this bit is reset, the MAC performs a perfect destination address filtering for unicast packets, that is, it compares the DA field with the values programmed in DA registers.Values: 0x0 (DISABLE): Hash Unicast is disabled

				0x1 (ENABLE): Hash Unicast is enabled Value After Reset: 0x0
PR	R/W	[0:0]	0x0	Promiscuous Mode When this bit is set, the Address Filtering module passes all incoming packets irrespective of the destination or source address. The SA or DA Filter Fails status bits of the Rx Status Word are always cleared when PR is set.Values: 0x0 (DISABLE): Promiscuous Mode is disabled 0x1 (ENABLE): Promiscuous Mode is enabled Value After Reset: 0x0

2.3.4 EQOS_MAC_R_MAC_WATCHDOG_TIMEOUT

Access Type: RW

Address Offset: 0xc

Name	Access	Bit Range	Reset value	Description
RESERVED_31_9	R	[31:9]	0x0	Reserved. Value After Reset: 0x0
PWE	R/W	[8:8]	0x0	Programmable Watchdog Enable When this bit is set and the WD bit of the MAC_Configuration register is reset, the WTO field is used as watchdog timeout for a received packet. When this bit is cleared, the watchdog timeout for a received packet is controlled by setting of WD and JE bits in MAC_Configuration register.Values: 0x0 (DISABLE): Programmable Watchdog is disabled 0x1 (ENABLE): Programmable Watchdog is enabled

				Value After Reset: 0x0
RESERVED_7_4	R	[7:4]	0x0	Reserved. Value After Reset: 0x0
WTO	R/W	[3:0]	0x0	Watchdog Timeout When the PWE bit is set and the WD bit of the MAC_Configuration register is reset, this field is used as watchdog timeout for a received packet. If the length of a received packet exceeds the value of this field, such packet is terminated and declared as an error packet. Note: When the PWE bit is set, the value in this field should be more than 1,522 (0x05F2). Otherwise, the IEEE 802.3-specified valid tagged packets are declared as error packets and then dropped.Values: 0x0 (M_2KBYTES): 2 KB 0x1 (M_3KBYTES): 3 KB 0x2 (M_4KBYTES): 4 KB 0x3 (M_5KBYTES): 5 KB 0x4 (M_6KBYTES): 6 KB 0x5 (M_7KBYTES): 7 KB 0x6 (M_8KBYTES): 8 KB 0x7 (M_9KBYTES): 9 KB 0x8 (M_10KBYTES): 10 KB 0x9 (M_11KBYTES): 11 KB 0xa (M_12KBYTES): 12 KB 0xb (M_13KBYTES): 13 KB 0xc (M_14KBYTES): 14 KB

				0xd (M_15KBYTES): 15 KB 0xe (M_16383BYTES): 16383 Bytes 0xf (RESERVED): Reserved Value After Reset: 0x0

2.3.5 EQOS_MAC_R_MAC_HASH_TABLE_REG0

Access Type: RW

Address Offset: 0x10

Name	Access	Bit Range	Reset value	Description
HT31T0	R/W	[31:0]	0x0	MAC Hash Table First 32 Bits This field contains the first 32 Bits [31:0] of the Hash table. Value After Reset: 0x0

2.3.6 EQOS_MAC_R_MAC_HASH_TABLE_REG1

Access Type: RW

Address Offset: 0x14

Name	Access	Bit Range	Reset value	Description
HT63T32	R/W	[31:0]	0x0	MAC Hash Table Second 32 Bits This field contains the second 32 Bits [63:32] of the Hash table. Value After Reset: 0x0

2.3.7 EQOS_MAC_R_MAC_VLAN_TAG_CTRL

Access Type: RW

Address Offset: 0x50

Name	Access	Bit Range	Reset value	Description
RESERVED	R	[31:31]	0x0	Reserved Field: Yes
RESERVED_30	R	[30:30]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[29:26]	0x0	Reserved Field: Yes
VTHM	R/W	[25:25]	0x0	VLAN Tag Hash Table Match Enable

				When this bit is set, the most significant four bits of CRC of VLAN Tag are used to index the content of the MAC_VLAN_Hash_Table register. A value of 1 in the VLAN Hash Table register, corresponding to the index, indicates that the packet matched the VLAN hash table. When the ETV bit is set, the CRC of the 12-bit VLAN Identifier (VID) is used for comparison. When the ETV bit is reset, the CRC of the 16-bit VLAN tag is used for comparison. When this bit is reset, the VLAN Hash Match operation is not performed.Values: 0x0 (DISABLE): VLAN Tag Hash Table Match is disabled 0x1 (ENABLE): VLAN Tag Hash Table Match is enabled Value After Reset: 0x0
EVLRXS	R/W	[24:24]	0x0	Enable VLAN Tag in Rx status When this bit is set, MAC provides the outer VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the outer VLAN Tag in Rx status.Values: 0x0 (DISABLE): VLAN Tag in Rx status is disabled 0x1 (ENABLE): VLAN Tag in Rx status is enabled Value After Reset: 0x0
RESERVED_23	R	[23:23]	0x0	Reserved. Value After Reset: 0x0
EVLS	R/W	[22:21]	0x0	Enable VLAN Tag Stripping on Receive This field indicates the stripping operation on the outer VLAN Tag in received packet.Values:

				0x0 (DONOT): Do not strip 0x1 (IFPASS): Strip if VLAN filter passes 0x2 (IFFAIL): Strip if VLAN filter fails 0x3 (ALWAYS): Always strip Value After Reset: 0x0
DOVLTC	R/W	[20:20]	0x0	Disable VLAN Type Check for VLAN Hash Filtering When this bit is set, the MAC VLAN Hash Filter does not check whether the VLAN Tag specified by the ERIVLT bit is of type S-VLAN or C-VLAN. When this bit is reset, the MAC VLAN Hash Filter filters or matches the VLAN Tag specified by the ERIVLT bit only when VLAN Tag type is similar to the one specified by the ERSVLM bit.Values: 0x0 (ENABLE): VLAN Type Check is enabled 0x1 (DISABLE): VLAN Type Check is disabled Value After Reset: 0x0
ERSVLM	R/W	[19:19]	0x0	Enable Receive S-VLAN Match for VLAN Hash Filtering When this bit is set, the MAC receiver enables VLAN Hash filtering or matching for S-VLAN (Type = 0x88A8) packets. When this bit is reset, the MAC receiver enables VLAN Hash filtering or matching for C-VLAN (Type = 0x8100) packets. The ERIVLT bit determines the VLAN tag position considered for VLAN Hash filtering or matching.Values: 0x0 (DISABLE): Receive S-VLAN Match is disabled 0x1 (ENABLE): Receive S-VLAN Match is

				enabled Value After Reset: 0x0
ESVL	R/W	[18:18]	0x0	Enable S-VLAN When this bit is set, the MAC transmitter and receiver consider the S-VLAN packets (Type = 0x88A8) as valid VLAN tagged packets.Values: 0x0 (DISABLE): S-VLAN is disabled 0x1 (ENABLE): S-VLAN is enabled Value After Reset: 0x0
VTIM	R/W	[17:17]	0x0	VLAN Tag Inverse Match Enable When this bit is set, this bit enables the VLAN Tag inverse matching. The packets without matching VLAN Tag are marked as matched. When reset, this bit enables the VLAN Tag perfect matching. The packets with matched VLAN Tag are marked as matched.Values: 0x0 (DISABLE): VLAN Tag Inverse Match is disabled 0x1 (ENABLE): VLAN Tag Inverse Match is enabled Value After Reset: 0x0
ETV	R/W	[16:16]	0x0	Enable 12-Bit VLAN Tag Comparison for VLAN Hash Filtering When this bit is set, a 12-bit VLAN identifier is used for VLAN Hash filtering instead of the complete 16-bit VLAN tag. Bits[11:0] of VLAN tag in the received VLAN-tagged packet are used for hash-based VLAN filtering. When this bit is reset, all 16 bits of the 15th and 16th bytes of the received VLAN packet are used

				for VLAN hash filtering.Values: 0x0 (DISABLE): 12-Bit VLAN Tag Comparison is disabled 0x1 (ENABLE): 12-Bit VLAN Tag Comparison is enabled Value After Reset: 0x0
RESERVED_15_Y	R	[15:5]	0x0	Reserved. Value After Reset: 0x0
OFS	R/W	[4:2]	0x0	Offset This field holds the address offset of the MAC VLAN Tag Filter Register which the application is trying to access. The width of the field depends on the number of MAC VLAN Tag Registers enabled. Value After Reset: 0x0
CT	R/W	[1:1]	0x0	Command Type This bit indicates if the current register access is a read or a write. When set, it indicate a read operation. When reset, it indicates a write operation.Values: 0x0 (WRITE): Write operation 0x1 (READ): Read operation Value After Reset: 0x0
OB	R/W	[0:0]	0x0	Operation Busy This bit is set along with a read or write command for initiating the indirect access to per VLAN Tag Filter register. This bit is reset when the read or write command to per VLAN Tag Filter indirect access register is complete. The next indirect register access can be initiated only after this bit is

				reset. During a write operation, the bit is reset only after the data has been written into the Per VLAN Tag register. During a read operation, the data should be read from the MAC_VLAN_Tag_Data register only after this bit is reset.Values: 0x0 (DISABLE): Operation Busy is disabled 0x1 (ENABLE): Operation Busy is enabled Value After Reset: 0x0 Testable: untestable

2.3.8 EQOS_MAC_R_MAC_VLAN_TAG_FILTER(#I)(FORI=0;I<=7)

Access Type: RW

Address Offset: 0x54

Name	Access	Bit Range	Reset value	Description
RESERVED_31_Y	R	[31:27]	0x0	Reserved. Value After Reset: 0x0
DMACHN	R/W	[26:25]	0x0	DMA Channel Number The DMA Channel number to which the VLAN Tagged Frame is to be routed if it passes this VLAN Tag Filter is programmed in this field. If the Routing based on VLAN Tag Filter is not necessary, this field need not be programmed. Value After Reset: 0x0
DMACHEN	R/W	[24:24]	0x0	DMA Channel Number Enable This bit is the Enable for the DMA Channel Number value programmed in the field DMACH. When this bit is reset, the Routing does not occur based on VLAN Filter result. The frame is routed based on DA Based DMA Channel Routing.Values: 0x0 (DISABLE): DMA Channel Number is disabled

				0x1 (ENABLE): DMA Channel Number is enabled Value After Reset: 0x0
RESERVED_23_21	R	[23:21]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[20:20]	0x0	Reserved Field: Yes
ERSVLM	R/W	[19:19]	0x0	Enable S-VLAN Match for received Frames This bit is valid only when VLAN Tag Enable of the Filter is set. When this bit is set, the MAC receiver enables filtering or matching for S-VLAN (Type = 0x88A8) packets. When this bit is reset, the MAC receiver enables filtering or matching for C-VLAN (Type = 0x8100) packets.Values: 0x0 (DISABLE): Receive S-VLAN Match is disabled 0x1 (ENABLE): Receive S-VLAN Match is enabled Value After Reset: 0x0
DOVLTC	R/W	[18:18]	0x0	Disable VLAN Type Comparison This bit is valid only when VLAN Tag Enable of the Filter is set. When this bit is set, the MAC does not check whether the VLAN Tag specified by the Enable Inner VLAN Tag Comparison bit is of type S-VLAN or C-VLAN. When this bit is reset, the MAC filters or matches the VLAN Tag specified by the Enable Inner VLAN Tag Comparison bit only when VLAN Tag type is similar to the one specified by the Enable S-VLAN Match for received Frames bit.Values:

				0x0 (ENABLE): VLAN type comparison is enabled 0x1 (DISABLE): VLAN type comparison is disabled Value After Reset: 0x0
ETV	R/W	[17:17]	0x0	12bits or 16bits VLAN comparison This bit is valid only when VEN of the Filter is set. When this bit is set, a 12-bit VLAN identifier is used for comparing and filtering instead of the complete 16-bit VLAN tag. Bits [11:0] of VLAN tag are compared with the corresponding field in the received VLAN-tagged packet.Values: 0x0 (M_16BIT): 16 bit VLAN comparison 0x1 (M_12BIT): 12 bit VLAN comparison Value After Reset: 0x0
VEN	R/W	[16:16]	0x0	VLAN Tag Enable This bit is used to enable or disable the VLAN Tag. When this bit is set, the MAC compares the VLAN Tag of received packet with the VLAN Tag ID. When this bit is reset, no comparison is performed irrespective of the programming of the other fields.Values: 0x0 (DISABLE): VLAN Tag is disabled 0x1 (ENABLE): VLAN Tag is enabled Value After Reset: 0x0
VID	R/W	[15:0]	0x0	

				VLAN Tag ID This field holds the VLAN Tag value which is used by the MAC for perfect comparison. It is valid when VLAN Tag Enable is set. Value After Reset: 0x0

2.3.9 EQOS_MAC_R_MAC_VLAN_TAG_DATA

Access Type: RW

Address Offset: 0x54

Name	Access	Bit Range	Reset value	Description
RESERVED_31_Y	R	[31:27]	0x0	Reserved. Value After Reset: 0x0
DMACHN	R/W	[26:25]	0x0	DMA Channel Number The DMA Channel number to which the VLAN Tagged Frame is to be routed if it passes this VLAN Tag Filter is programmed in this field. If the Routing based on VLAN Tag Filter is not necessary, this field need not be programmed. Value After Reset: 0x0
DMACHEN	R/W	[24:24]	0x0	DMA Channel Number Enable This bit is the Enable for the DMA Channel Number value programmed in the field DMACH. When this bit is reset, the Routing does not occur based on VLAN Filter result. The frame is routed based on DA Based DMA Channel Routing.Values: 0x0 (DISABLE): DMA Channel Number is disabled 0x1 (ENABLE): DMA Channel Number is enabled Value After Reset: 0x0
RESERVED_23_21	R	[23:21]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[20:20]	0x0	Reserved Field: Yes

ERSVLM	R/W	[19:19]	0x0	Enable S-VLAN Match for received Frames This bit is valid only when VLAN Tag Enable of the Filter is set. When this bit is set, the MAC receiver enables filtering or matching for S-VLAN (Type = 0x88A8) packets. When this bit is reset, the MAC receiver enables filtering or matching for C-VLAN (Type = 0x8100) packets.Values: 0x0 (DISABLE): Receive S-VLAN Match is disabled 0x1 (ENABLE): Receive S-VLAN Match is enabled Value After Reset: 0x0
DOVLTC	R/W	[18:18]	0x0	Disable VLAN Type Comparison This bit is valid only when VLAN Tag Enable of the Filter is set. When this bit is set, the MAC does not check whether the VLAN Tag specified by the Enable Inner VLAN Tag Comparison bit is of type S-VLAN or C-VLAN. When this bit is reset, the MAC filters or matches the VLAN Tag specified by the Enable Inner VLAN Tag Comparison bit only when VLAN Tag type is similar to the one specified by the Enable S-VLAN Match for received Frames bit.Values: 0x0 (ENABLE): VLAN type comparison is enabled 0x1 (DISABLE): VLAN type comparison is disabled Value After Reset: 0x0
ETV	R/W	[17:17]	0x0	12bits or 16bits VLAN comparison

				This bit is valid only when VEN of the Filter is set. When this bit is set, a 12-bit VLAN identifier is used for comparing and filtering instead of the complete 16-bit VLAN tag. Bits [11:0] of VLAN tag are compared with the corresponding field in the received VLAN-tagged packet.Values: 0x0 (M_16BIT): 16 bit VLAN comparison 0x1 (M_12BIT): 12 bit VLAN comparison Value After Reset: 0x0
VEN	R/W	[16:16]	0x0	VLAN Tag Enable This bit is used to enable or disable the VLAN Tag. When this bit is set, the MAC compares the VLAN Tag of received packet with the VLAN Tag ID. When this bit is reset, no comparison is performed irrespective of the programming of the other fields.Values: 0x0 (DISABLE): VLAN Tag is disabled 0x1 (ENABLE): VLAN Tag is enabled Value After Reset: 0x0
VID	R/W	[15:0]	0x0	VLAN Tag ID This field holds the VLAN Tag value which is used by the MAC for perfect comparison. It is valid when VLAN Tag Enable is set. Value After Reset: 0x0

2.3.10 EQOS_MAC_R_MAC_VLAN_HASH_TABLE

Access Type: RW

Address Offset: 0x58

Name	Access	Bit Range	Reset value	Description

RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
VLHT	R/W	[15:0]	0x0	VLAN Hash Table This field contains the 16-bit VLAN Hash Table. Value After Reset: 0x0

2.3.11 EQOS_MAC_R_MAC_VLAN_INCL(#I)(FORI=0;I<=3)

Access Type: RW

Address Offset: 0x60

Name	Access	Bit Range	Reset value	Description
RESERVED_31_20	R	[31:20]	0x0	Reserved. Value After Reset: 0x0
CSVL	R/W	[19:19]	0x0	C-VLAN or S-VLAN When this bit is set, S-VLAN type (0x88A8) is inserted in the 13th and 14th bytes of transmitted packets. When this bit is reset, C-VLAN type (0x8100) is inserted in the 13th and 14th bytes of transmitted packets.Values: 0x0 (C-VLAN): C-VLAN type (0x8100) is inserted 0x1 (S-VLAN): S-VLAN type (0x88A8) is inserted Value After Reset: 0x0
RESERVED_18_16	R	[18:16]	0x0	Reserved. Value After Reset: 0x0
VLT	R/W	[15:0]	0x0	VLAN Tag for Transmit Packets This field contains the value of the VLAN tag to be inserted. The value must only be changed when the transmit lines are inactive or during the initialization phase. Bits[15:13] are the User Priority field, Bit 12 is the CFI/DEI field, and Bits[11:0] are the VID field

				in the VLAN tag. The following list describes the bits of this field: Bits[15:13]: User Priority Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) Bits[11:0]: VLAN Identifier (VID) field of VLAN tag Value After Reset: 0x0

2.3.12 EQOS_MAC_R_MAC_VLAN_INCL

Access Type: RW

Address Offset: 0x60

Name	Access	Bit Range	Reset value	Description
BUSY	R	[31:31]	0x0	Busy This bit indicates the status of the read/write operation of indirect access to the queue/channel specific VLAN inclusion register. For write operation write to a register is complete when this bit is reset. For read operation the read data is valid when the bit is reset. The application must make sure that this bit is reset before attempting subsequent access to this register.Values: 0x0 (INACTIVE): Busy status not detected 0x1 (ACTIVE): Busy status detected Value After Reset: 0x0 Testable: untestable
RDWR	R/W	[30:30]	0x0	Read write control This bit controls the read or write operation for indirectly accessing the queue/channel specific VLAN Inclusion register. When set indicates write operation and when reset indicates read operation.

				This does not have any effect when CBTI is reset.Values: 0x0 (READ): Read operation of indirect access 0x1 (WRITE): Write operation of indirect access Value After Reset: 0x0
RESERVED_29_Y	R	[29:26]	0x0	Reserved. Value After Reset: 0x0
ADDR	R/W	[25:24]	0x0	Address This field selects one of the queue/channel specific VLAN Inclusion register for read/write access. This does not have any effect when CBTI is reset. Value After Reset: 0x0
RESERVED_23_22	R	[23:22]	0x0	Reserved. Value After Reset: 0x0
CBTI	R/W	[21:21]	0x0	Channel based tag insertion When this bit is set, outer VLAN tag is inserted for every packets transmitted by the MAC. The tag value is taken from the queue/channel specific VLAN tag register. The VLTI, VLP, VLC, and VLT fields of this register are ignored when this bit is set. When this bit is set, a write operation to byte 3 of this register initiates the read/write access to the indirect register. When reset, outer VLAN operation is based on the setting of VLTI, VLP, VLC and VLT fields of this register.Values: 0x0 (DISABLE): Channel based tag insertion is disabled 0x1 (ENABLE): Channel based tag insertion is enabled

				Value After Reset: 0x0
VLTI	R/W	[20:20]	0x0	VLAN Tag Input When this bit is set, it indicates that the VLAN tag to be inserted or replaced in Tx packet should be taken from: The Tx descriptor Values: 0x0 (DISABLE): VLAN Tag Input is disabled 0x1 (ENABLE): VLAN Tag Input is enabled Value After Reset: 0x0
CSVL	R/W	[19:19]	0x0	C-VLAN or S-VLAN When this bit is set, S-VLAN type (0x88A8) is inserted or replaced in the 13th and 14th bytes of transmitted packets. When this bit is reset, C-VLAN type (0x8100) is inserted or replaced in the 13th and 14th bytes of transmitted packets.Values: 0x0 (C-VLAN): C-VLAN type (0x8100) is inserted or replaced 0x1 (S-VLAN): S-VLAN type (0x88A8) is inserted or replaced Value After Reset: 0x0
VLP	R/W	[18:18]	0x0	VLAN Priority Control When this bit is set, the control bits[17:16] are used for VLAN deletion, insertion, or replacement. When this bit is reset, the mti_vlan_ctrl_i control input is used and bits[17:16] are ignored.Values:

				0x0 (DISABLE): VLAN Priority Control is disabled 0x1 (ENABLE): VLAN Priority Control is enabled Value After Reset: 0x0
VLC	R/W	[17:16]	0x0	VLAN Tag Control in Transmit Packets 2'b00: No VLAN tag deletion, insertion, or replacement 2'b01: VLAN tag deletion The MAC removes the VLAN type (bytes 13 and 14) and VLAN tag (bytes 15 and 16) of all transmitted packets with VLAN tags. 2'b10: VLAN tag insertion The MAC inserts VLT in bytes 15 and 16 of the packet after inserting the Type value (0x8100 or 0x88a8) in bytes 13 and 14. This operation is performed on all transmitted packets, irrespective of whether they already have a VLAN tag. 2'b11: VLAN tag replacement The MAC replaces VLT in bytes 15 and 16 of all VLAN-type transmitted packets (Bytes 13 and 14 are 0x8100 or 0x88a8). Note: Changes to this field take effect only on the start of a packet. If you write this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated value.Values: 0x0 (NONE): No VLAN tag deletion, insertion, or replacement

				0x1 (DELETE): VLAN tag deletion 0x2 (INSERT): VLAN tag insertion 0x3 (REPLACE): VLAN tag replacement Value After Reset: 0x0
VLT	R/W	[15:0]	0x0	VLAN Tag for Transmit Packets This field contains the value of the VLAN tag to be inserted or replaced. The value must only be changed when the transmit lines are inactive or during the initialization phase. Bits[15:13] are the User Priority field, Bit 12 is the CFI/DEI field, and Bits[11:0] are the VID field in the VLAN tag. The following list describes the bits of this field: Bits[15:13]: User Priority Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) Bits[11:0]: VLAN Identifier (VID) field of VLAN tag Value After Reset: 0x0

2.3.13 EQOS_MAC_R_MAC_Q0_TX_FLOW_CTRL

Access Type: RW

Address Offset: 0x70

Name	Access	Bit Range	Reset value	Description
PT	R/W	[31:16]	0x0	Pause Time This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain. Value After Reset: 0x0

RESERVED_15_8	R	[15:8]	0x0	Reserved. Value After Reset: 0x0
DZPQ	R/W	[7:7]	0x0	Disable Zero-Quanta Pause When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled.Values: 0x0 (ENABLE): Zero-Quanta Pause packet generation is enabled 0x1 (DISABLE): Zero-Quanta Pause packet generation is disabled Value After Reset: 0x0
PLT	R/W	[6:4]	0x0	Pause Low Threshold This field configures the threshold of the Pause timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of the Pause packet. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot times), and PLT = 001, a second Pause packet is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot times after the first Pause packet is transmitted. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII or MII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times.Values: 0x0 (PT4): Pause Time minus 4 Slot Times (PT -4

				slot times) 0x1 (PT28): Pause Time minus 28 Slot Times (PT -28 slot times) 0x2 (PT36): Pause Time minus 36 Slot Times (PT -36 slot times) 0x3 (PT144): Pause Time minus 144 Slot Times (PT -144 slot times) 0x4 (PT256): Pause Time minus 256 Slot Times (PT -256 slot times) 0x5 (PT512): Pause Time minus 512 Slot Times (PT -512 slot times) 0x6 (RSVD): Reserved Value After Reset: 0x0
RESERVED_3_2	R	[3:2]	0x0	Reserved. Value After Reset: 0x0
TFE	R/W	[1:1]	0x0	Transmit Flow Control Enable In the full-duplex mode, when this bit is set, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets.Values: 0x0 (DISABLE): Transmit Flow Control is disabled 0x1 (ENABLE): Transmit Flow Control is enabled Value After Reset: 0x0
FCB_BPA	R/W	[0:0]	0x0	Flow Control Busy This bit initiates a Pause packet in the full-duplex mode if the TFE bit is set. In the full-duplex mode, this bit should be read as

				1'b0 before writing to this register. To initiate a Pause packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When Pause packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.Values: 0x0 (DISABLE): Flow Control Busy or Backpressure Activate is disabled 0x1 (ENABLE): Flow Control Busy or Backpressure Activate is enabled Value After Reset: 0x0 Testable: untestable

2.3.14 EQOS_MAC_R_MAC_RX_FLOW_CTRL

Access Type: RW

Address Offset: 0x90

Name	Access	Bit Range	Reset value	Description
RESERVED_31_9	R	[31:9]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[8:8]	0x0	Reserved Field: Yes
RESERVED_7_2	R	[7:2]	0x0	Reserved. Value After Reset: 0x0
UP	R/W	[1:1]	0x0	Unicast Pause Packet Detect A pause packet is processed when it has the unique multicast address specified in the IEEE 802.3. When this bit is set, the MAC can also detect Pause packets with unicast address of the station. This unicast address should be as specified in MAC_Address0_High and MAC_Address0_Low. When this bit is reset, the MAC only detects Pause

				packets with unique multicast address. Note: The MAC does not process a Pause packet if the multicast address is different from the unique multicast address. This is also applicable to the received PFC packet when the Priority Flow Control (PFC) is enabled. The unique multicast address (0x01_80_C2_00_00_01) is as specified in IEEE 802.1 Qbb-2011.Values: 0x0 (DISABLE): Unicast Pause Packet Detect disabled 0x1 (ENABLE): Unicast Pause Packet Detect enabled Value After Reset: 0x0
RFE	R/W	[0:0]	0x0	Receive Flow Control Enable When this bit is set and the MAC is operating in full-duplex mode, the MAC decodes the received Pause packet and disables its transmitter for a specified (Pause) time. When this bit is reset or the MAC is operating in half-duplex mode, the decode function of the Pause packet is disabled. When PFC is enabled, flow control is enabled for PFC packets. The MAC decodes the received PFC packet and disables the Transmit queue, with matching priorities, for a duration of received Pause time.Values: 0x0 (DISABLE): Receive Flow Control is disabled 0x1 (ENABLE): Receive Flow Control is enabled Value After Reset: 0x0

2.3.15 EQOS_MAC_R_MAC_RXQ_CTRL4

Access Type: RW

Address Offset: 0x94

Name	Access	Bit Range	Reset value	Description
RESERVED_31_Y	R	[31:19]	0x0	

				Reserved. Value After Reset: 0x0
VFFQ	R/W	[18:17]	0x0	VLAN Tag Filter Fail Packets Queue This field holds the Rx queue number to which the tagged packets failing the Destination or Source Address filter (and UFFQE/MFFQE not enabled) or failing the VLAN tag filter must be routed to. This field is valid only when the VFFQE bit is set. Value After Reset: 0x0
VFFQE	R/W	[16:16]	0x0	VLAN Tag Filter Fail Packets Queuing Enable When this bit is set, the tagged packets which fail the Destination or Source address filter or fail the VLAN tag filter, are routed to the Rx Queue Number programmed in the VFFQ. When this bit is reset, the tagged packets which fail the Destination or Source address filter or fail the VLAN tag filter are routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set.Values: 0x0 (DISABLE): VLAN tag Filter Fail Packets Queuing is disabled 0x1 (ENABLE): VLAN tag Filter Fail Packets Queuing is enabled Value After Reset: 0x0
RESERVED_15_Y	R	[15:11]	0x0	Reserved. Value After Reset: 0x0
MFFQ	R/W	[10:9]	0x0	Multicast Address Filter Fail Packets Queue. This field holds the Rx queue number to which the Multicast packets failing the Destination or Source Address filter are routed to. This field is valid only when the MFFQE bit is set. Value After Reset: 0x0
MFFQE	R/W	[8:8]	0x0	Multicast Address Filter Fail Packets Queuing

				Enable. When this bit is set, the Multicast packets which fail the Destination or Source address filter is routed to the Rx Queue Number programmed in the MFFQ. When this bit is reset, the Multicast packets which fail the Destination or Source address filter is routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set.Values: 0x0 (DISABLE): Multicast Address Filter Fail Packets Queuing is disabled 0x1 (ENABLE): Multicast Address Filter Fail Packets Queuing is enabled Value After Reset: 0x0
RESERVED_7_Y	R	[7:3]	0x0	Reserved. Value After Reset: 0x0
UFFQ	R/W	[2:1]	0x0	Unicast Address Filter Fail Packets Queue. This field holds the Rx queue number to which the Unicast packets failing the Destination or Source Address filter are routed to. This field is valid only when the UFFQE bit is set. Value After Reset: 0x0
UFFQE	R/W	[0:0]	0x0	Unicast Address Filter Fail Packets Queuing Enable. When this bit is set, the Unicast packets which fail the Destination or Source address filter is routed to the Rx Queue Number programmed in the UFFQ. When this bit is reset, the Unicast packets which fail the Destination or Source address filter is routed based on other routing options. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set.Values: 0x0 (DISABLE): Unicast Address Filter Fail Packets Queuing is disabled

				0x1 (ENABLE): Unicast Address Filter Fail Packets Queuing is enabled Value After Reset: 0x0

2.3.16 EQOS_MAC_R_MAC_RXQ_CTRL0

Access Type: RW

Address Offset: 0xa0

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[15:8]	0x0	Reserved Field: Yes
RXQ3EN	R/W	[7:6]	0x0	Receive Queue 3 Enable This field is similar to the RXQ0EN field.Values: 0x0 (DISABLE): Queue not enabled 0x1 (EN_AV): Queue enabled for AV 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic 0x3 (RSVD): Reserved Value After Reset: 0x0
RXQ2EN	R/W	[5:4]	0x0	Receive Queue 2 Enable This field is similar to the RXQ0EN field.Values: 0x0 (DISABLE): Queue not enabled 0x1 (EN_AV): Queue enabled for AV 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic 0x3 (RSVD): Reserved

				Value After Reset: 0x0
RXQ1EN	R/W	[3:2]	0x0	Receive Queue 1 Enable This field is similar to the RXQ0EN field.Values: 0x0 (DISABLE): Queue not enabled 0x1 (EN_AV): Queue enabled for AV 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic 0x3 (RSVD): Reserved Value After Reset: 0x0
RXQ0EN	R/W	[1:0]	0x0	Receive Queue 0 Enable This field indicates whether Rx Queue 0 is enabled for AV or DCB.Values: 0x0 (DISABLE): Queue not enabled 0x1 (EN_AV): Queue enabled for AV 0x2 (EN_DCB_GEN): Queue enabled for DCB/Generic 0x3 (RSVD): Reserved Value After Reset: 0x0

2.3.17 EQOS_MAC_R_MAC_RXQ_CTRL1

Access Type: RW

Address Offset: 0xa4

Name	Access	Bit Range	Reset value	Description
RESERVED_31_Y	R	[31:27]	0x0	Reserved. Value After Reset: 0x0

FPRQ	R/W	[26:24]	0x0	Frame Preemption Residue Queue This field holds the Rx queue number to which the residual preemption frames must be forwarded. Preemption frames that are tagged and pass the SA/DA/VLAN filtering are routed based on PSRQ and all other frames are treated as residual frames and is routed to the queue number mentioned in this field. The Queue-0 is used as a default queue for express frames, so this field cannot be programmed to a value 0. Value After Reset: 0x0
TPQC	R/W	[23:22]	0x0	Tagged PTP over Ethernet Packets Queuing Control. This field controls the routing of the VLAN Tagged PTPoE packets. If DWC_EQOS_AV_ENABLE is selected in the configuration, the following programmable options are allowed. 2'b00: VLAN Tagged PTPoE packets are routed as generic VLAN Tagged packet (based on PSRQ for only non-AV enabled Rx Queues). 2'b01: VLAN Tagged PTPoE packets are routed to Rx Queue specified by PTPQ field (That Rx Queue can be enabled for AV or non-AV traffic). 2'b10: VLAN Tagged PTPoE packets are routed to only AV enabled Rx Queues based on PSRQ. 2'b11: Reserved If DWC_EQOS_AV_ENABLE is not selected in the configuration, the following programmable options are allowed. 1'b0: VLAN Tagged PTPoE packets are routed as generic VLAN Tagged packet (based on PSRQ for DCB/Generic enabled Rx Queues). 1'b1: VLAN Tagged PTPoE packets are routed to

				Rx Queues specified by PTPQ field. Value After Reset: 0x0
TACPQE	R/W	[21:21]	0x0	Tagged AV Control Packets Queuing Enable. When set, the MAC routes the received Tagged AV Control packets to the Rx queue specified by AVCPQ field. When reset, the MAC routes the received Tagged AV Control packets based on the tag priority matching the PSRQ fields in MAC_RxQ_Ctrl2 and MAC_RxQ_Ctrl3 registers.Values: 0x0 (DISABLE): Tagged AV Control Packets Queuing is disabled 0x1 (ENABLE): Tagged AV Control Packets Queuing is enabled Value After Reset: 0x0
MCBCQEN	R/W	[20:20]	0x0	Multicast and Broadcast Queue Enable This bit specifies that Multicast or Broadcast packets routing to the Rx Queue is enabled and the Multicast or Broadcast packets must be routed to Rx Queue specified in MCBCQ field.Values: 0x0 (DISABLE): Multicast and Broadcast Queue is disabled 0x1 (ENABLE): Multicast and Broadcast Queue is enabled Value After Reset: 0x0
RESERVED_19	R	[19:19]	0x0	Reserved. Value After Reset: 0x0
MCBCQ	R/W	[18:16]	0x0	Multicast and Broadcast Queue This field specifies the Rx Queue onto which

				Multicast or Broadcast Packets are routed. Any Rx Queue enabled for Generic/DCB/AV traffic can be used to route the Multicast or Broadcast Packets.Values: 0x0 (QUEUE0): Receive Queue 0 0x1 (QUEUE1): Receive Queue 1 0x2 (QUEUE2): Receive Queue 2 0x3 (QUEUE3): Receive Queue 3 0x4 (QUEUE4): Receive Queue 4 0x5 (QUEUE5): Receive Queue 5 0x6 (QUEUE6): Receive Queue 6 0x7 (QUEUE7): Receive Queue 7 Value After Reset: 0x0
RESERVED_15	R	[15:15]	0x0	Reserved. Value After Reset: 0x0
UPQ	R/W	[14:12]	0x0	Untagged Packet Queue This field indicates the Rx Queue to which Untagged Packets are to be routed. Any Rx Queue enabled for Generic/DCB/AV traffic can be used to route the Untagged Packets.Values: 0x0 (QUEUE0): Receive Queue 0 0x1 (QUEUE1): Receive Queue 1 0x2 (QUEUE2): Receive Queue 2 0x3 (QUEUE3): Receive Queue 3 0x4 (QUEUE4): Receive Queue 4

				0x5 (QUEUE5): Receive Queue 5 0x6 (QUEUE6): Receive Queue 6 0x7 (QUEUE7): Receive Queue 7 Value After Reset: 0x0
RESERVED_11	R	[11:11]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[10:8]	0x0	Reserved Field: Yes
RESERVED_7	R	[7:7]	0x0	Reserved. Value After Reset: 0x0
PTPQ	R/W	[6:4]	0x0	PTP Packets Queue This field specifies the Rx queue on which the PTP packets sent over the Ethernet payload (not over IPv4 or IPv6) are routed. When the AV8021ASMEN bit of MAC_Timestamp_Control register is set, only untagged PTP over Ethernet packets are routed on an Rx Queue. If the bit is not set, then based on programming of TPQC field, both tagged and untagged PTPoE packets can be routed to this Rx Queue.Values: 0x0 (QUEUE0): Receive Queue 0 0x1 (QUEUE1): Receive Queue 1 0x2 (QUEUE2): Receive Queue 2 0x3 (QUEUE3): Receive Queue 3 0x4 (QUEUE4): Receive Queue 4 0x5 (QUEUE5): Receive Queue 5 0x6 (QUEUE6): Receive Queue 6

				0x7 (QUEUE7): Receive Queue 7 Value After Reset: 0x0
RESERVED_3	R	[3:3]	0x0	Reserved. Value After Reset: 0x0
AVCPQ	R/W	[2:0]	0x0	AV Untagged Control Packets Queue This field specifies the Receive queue on which the received AV tagged and untagged control packets are routed. The AV tagged (when TACPQE bit is set) and untagged control packets are routed to Receive queue specified by this field.Values: 0x0 (QUEUE0): Receive Queue 0 0x1 (QUEUE1): Receive Queue 1 0x2 (QUEUE2): Receive Queue 2 0x3 (QUEUE3): Receive Queue 3 0x4 (QUEUE4): Receive Queue 4 0x5 (QUEUE5): Receive Queue 5 0x6 (QUEUE6): Receive Queue 6 0x7 (QUEUE7): Receive Queue 7 Value After Reset: 0x0

2.3.18 EQOS_MAC_R_MAC_RXQ_CTRL2

Access Type: RW

Address Offset: 0xa8

Name	Access	Bit Range	Reset value	Description
PSRQ3	R/W	[31:24]	0x0	Priorities Selected in the Receive Queue 3 This field decides the priorities assigned to Rx Queue 3. All

				packets with priorities that match the values set in this field are routed to Rx Queue 3. For example, if PSRQ3[6, 3] are set, packets with USP field equal to 3 or 6 are routed to Rx Queue 3. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. Value After Reset: 0x0
PSRQ2	R/W	[23:16]	0x0	Priorities Selected in the Receive Queue 2 This field decides the priorities assigned to Rx Queue 2. All packets with priorities that match the values set in this field are routed to Rx Queue 2. For example, if PSRQ2[1, 0] are set, packets with USP field equal to 1 or 0 are routed to Rx Queue 2. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. Value After Reset: 0x0
PSRQ1	R/W	[15:8]	0x0	Priorities Selected in the Receive Queue 1 This field decides the priorities assigned to Rx Queue 1. All packets with priorities that match the values set in this field are routed to Rx Queue 1. For example, if PSRQ1[4] is set, packets with USP field equal to 4 are routed to Rx Queue 1. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues. Value After Reset: 0x0
PSRQ0	R/W	[7:0]	0x0	Priorities Selected in the Receive Queue 0 This field decides the priorities assigned to Rx Queue 0. All packets with priorities that match the values set in this field are routed to Rx Queue 0. For example, if PSRQ0[5] is set, packets with USP field equal to 5 are routed to Rx Queue 0. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues.

				Value After Reset: 0x0

2.3.19 EQOS_MAC_R_MAC_INTERRUPT_STATUS

Access Type: RW

Address Offset: 0xb0

Name	Access	Bit Range	Reset value	Description
RESERVED_31_21	R	[31:21]	0x0	Reserved. Value After Reset: 0x0
MFRIS	R	[20:20]	0x0	MMC FPE Receive Interrupt Status This bit is set high when an interrupt is generated in the MMC FPE Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option along with FPE support.Values: 0x0 (INACTIVE): MMC FPE Receive Interrupt status not active 0x1 (ACTIVE): MMC FPE Receive Interrupt status active Value After Reset: 0x0
MFTIS	R	[19:19]	0x0	MMC FPE Transmit Interrupt Status This bit is set high when an interrupt is generated in the MMC FPE Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option along with FPE support.Values: 0x0 (INACTIVE): MMC FPE Transmit Interrupt status not active 0x1 (ACTIVE): MMC FPE Transmit Interrupt status active

				Value After Reset: 0x0
MDIOIS	R	[18:18]	0x0	MDIO Interrupt Status This bit indicates an interrupt event after the completion of MDIO operation. To reset this bit, the application has to read this bit/Write 1 to this bit when RCWE bit of MAC_CSR_SW_Ctrl register is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MDIO Interrupt status not active 0x1 (ACTIVE): MDIO Interrupt status active Value After Reset: 0x0
FPEIS	R	[17:17]	0x0	Frame Preemption Interrupt Status This bit indicates an interrupt event during the operation of Frame Preemption (Bits[19:16] of MAC_FPE_CTRL_STS register is set). To reset this bit, the application must clear the event in MAC_FPE_CTRL_STS that has caused the Interrupt.Values: 0x0 (INACTIVE): Frame Preemption Interrupt status not active 0x1 (ACTIVE): Frame Preemption Interrupt status active Value After Reset: 0x0
RESERVED_16	R	[16:16]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[15:15]	0x0	Reserved Field: Yes
RXSTSIS	R	[14:14]	0x0	Receive Status Interrupt

				This bit indicates the status of received packets. This bit is set when the RWT bit is set in the MAC_Rx_Tx_Status register. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register.Values: 0x0 (INACTIVE): Receive Interrupt status not active 0x1 (ACTIVE): Receive Interrupt status active Value After Reset: 0x0
TXSTSIS	R	[13:13]	0x0	Transmit Status Interrupt This bit indicates the status of transmitted packets. This bit is set when any of the following bits is set in the MAC_Rx_Tx_Status register: Excessive Collision (EXCOL) Late Collision (LCOL) Excessive Deferral (EXDEF) Loss of Carrier (LCARR) No Carrier (NCARR) Jabber Timeout (TJT) This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register.Values: 0x0 (INACTIVE): Transmit Interrupt status not active 0x1 (ACTIVE): Transmit Interrupt status active

				Value After Reset: 0x0
TSIS	R	[12:12]	0x0	Timestamp Interrupt Status If the Timestamp feature is enabled, this bit is set when any of the following conditions is true: The system time value is equal to or exceeds the value specified in the Target Time High and Low registers. There is an overflow in the Seconds register. The Target Time Error occurred, that is, programmed target time already elapsed. If the Auxiliary Snapshot feature is enabled, this bit is set when the auxiliary snapshot trigger is asserted.In configurations other than EQOS_CORE, when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and Mac_TxTimestamp_Status_Seconds registers. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Timestamp_Status register.Values: 0x0 (INACTIVE): Timestamp Interrupt status not active 0x1 (ACTIVE): Timestamp Interrupt status active Value After Reset: 0x0
RESERVED	R	[11:11]	0x0	Reserved Field: Yes
MMCTXIS	R	[10:10]	0x0	MMC Transmit Interrupt Status This bit is set high when an interrupt is generated in the MMC Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are

				cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option.Values: 0x0 (INACTIVE): MMC Transmit Interrupt status not active 0x1 (ACTIVE): MMC Transmit Interrupt status active Value After Reset: 0x0
MMCRXIS	R	[9:9]	0x0	MMC Receive Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option.Values: 0x0 (INACTIVE): MMC Receive Interrupt status not active 0x1 (ACTIVE): MMC Receive Interrupt status active Value After Reset: 0x0
MMCIS	R	[8:8]	0x0	MMC Interrupt Status This bit is set high when Bit 11, Bit 10, or Bit 9 is set high. This bit is cleared only when all these bits are low. This bit is valid only when you select the Enable MAC Management Counters (MMC) option.Values: 0x0 (INACTIVE): MMC Interrupt status not active 0x1 (ACTIVE): MMC Interrupt status active

				Value After Reset: 0x0
RESERVED_7_6	R	[7:6]	0x0	Reserved. Value After Reset: 0x0
LPIIS	R	[5:5]	0x0	LPI Interrupt Status When the Energy Efficient Ethernet feature is enabled, this bit is set for any LPI state entry or exit in the MAC Transmitter or Receiver. This bit is cleared when the corresponding interrupt source bit of MAC_LPI_Control_Status register is read (or corresponding interrupt source bit of MAC_LPI_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set).Values: 0x0 (INACTIVE): LPI Interrupt status not active 0x1 (ACTIVE): LPI Interrupt status active Value After Reset: 0x0
RESERVED	R	[4:4]	0x0	Reserved Field: Yes
PHYIS	R	[3:3]	0x0	PHY Interrupt This bit is set when rising edge is detected on the phy_intr_i input. This bit is cleared when this register is read (or this bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set).Values: 0x0 (INACTIVE): PHY Interrupt not detected 0x1 (ACTIVE): PHY Interrupt detected Value After Reset: 0x0
RESERVED	R	[2:1]	0x0	Reserved Field: Yes
RGSMIIIS	R	[0:0]	0x0	RGMII or SMII Interrupt Status This bit is set because of any change in value of the

				Link Status of RGMII or SMII interface (LNKSTS bit in MAC_PHYIF_Control_Status register). This bit is cleared when the MAC_PHYIF_Control_Status register is read (or LNKSTS bit of MAC_PHYIF_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the optional RGMII or SMII PHY interface.Values: 0x0 (INACTIVE): RGMII or SMII Interrupt Status is not active 0x1 (ACTIVE): RGMII or SMII Interrupt Status is active Value After Reset: 0x0 Testable: untestable

2.3.20 EQOS_MAC_R_MAC_INTERRUPT_ENABLE

Access Type: RW

Address Offset: 0xb4

Name	Access	Bit Range	Reset value	Description
RESERVED_31_19	R	[31:19]	0x0	Reserved. Value After Reset: 0x0
MDIOIE	R/W	[18:18]	0x0	MDIO Interrupt Enable When this bit is set, it enables the assertion of the interrupt when MDIOIS field is set in the MAC_Interrupt_Status register.Values: 0x0 (DISABLE): MDIO Interrupt is disabled 0x1 (ENABLE): MDIO Interrupt is enabled Value After Reset: 0x0
FPEIE	R/W	[17:17]	0x0	Frame Preemption Interrupt Enable When this bit is set, it enables the assertion of the

				interrupt when FPEIS field is set in the MAC_Interrupt_Status register.Values: 0x0 (DISABLE): Frame Preemption Interrupt is disabled 0x1 (ENABLE): Frame Preemption Interrupt is enabled Value After Reset: 0x0
RESERVED_16	R	[16:16]	0x0	Reserved. Value After Reset: 0x0
RESERVED_15	R	[15:15]	0x0	Reserved. Value After Reset: 0x0
RXSTSIE	R/W	[14:14]	0x0	Receive Status Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of RXSTSIS bit in the MAC_Interrupt_Status register.Values: 0x0 (DISABLE): Receive Status Interrupt is disabled 0x1 (ENABLE): Receive Status Interrupt is enabled Value After Reset: 0x0
TXSTSIE	R/W	[13:13]	0x0	Transmit Status Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of TXSTSIS bit in the MAC_Interrupt_Status register.Values: 0x0 (DISABLE): Timestamp Status Interrupt is disabled 0x1 (ENABLE): Timestamp Status Interrupt is

				enabled Value After Reset: 0x0
TSIE	R/W	[12:12]	0x0	Timestamp Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of TSIS bit in MAC_Interrupt_Status register.Values: 0x0 (DISABLE): Timestamp Interrupt is disabled 0x1 (ENABLE): Timestamp Interrupt is enabled Value After Reset: 0x0
RESERVED_11_6	R	[11:6]	0x0	Reserved. Value After Reset: 0x0
LPIIE	R/W	[5:5]	0x0	LPI Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of LPIIS bit in MAC_Interrupt_Status register.Values: 0x0 (DISABLE): LPI Interrupt is disabled 0x1 (ENABLE): LPI Interrupt is enabled Value After Reset: 0x0
RESERVED	R	[4:4]	0x0	Reserved Field: Yes
PHYIE	R/W	[3:3]	0x0	PHY Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of PHYIS bit in MAC_Interrupt_Status register.Values: 0x0 (DISABLE): PHY Interrupt is disabled 0x1 (ENABLE): PHY Interrupt is enabled

				Value After Reset: 0x0
RESERVED	R	[2:1]	0x0	Reserved Field: Yes
RGSMIIIE	R/W	[0:0]	0x0	RGMII or SMII Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of RGSMIIIS bit in MAC_Interrupt_Status register.Values: 0x0 (DISABLE): RGMII or SMII Interrupt is disabled 0x1 (ENABLE): RGMII or SMII Interrupt is enabled Value After Reset: 0x0

2.3.21 EQOS_MAC_R_MAC_RX_TX_STATUS

Access Type: RW

Address Offset: 0xb8

Name	Access	Bit Range	Reset value	Description
RESERVED_31_9	R	[31:9]	0x0	Reserved. Value After Reset: 0x0
RWT	R	[8:8]	0x0	Receive Watchdog Timeout This bit is set when a packet with length greater than 2,048 bytes is received (10, 240 bytes when Jumbo Packet mode is enabled) and the WD bit is reset in the MAC_Configuration register. This bit is set when a packet with length greater than 16,383 bytes is received and the WD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.Values: 0x0 (INACTIVE): No receive watchdog timeout 0x1 (ACTIVE): Receive watchdog timed out

				Value After Reset: 0x0
RESERVED_7_6	R	[7:6]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[5:1]	0x0	Reserved Field: Yes
TJT	R	[0:0]	0x0	Transmit Jabber Timeout This bit indicates that the Transmit Jabber Timer expired which happens when the packet size exceeds 2,048 bytes (10,240 bytes when the Jumbo packet is enabled) and JD bit is reset in the MAC_Configuration register. This bit is set when the packet size exceeds 16,383 bytes and the JD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.Values: 0x0 (INACTIVE): No Transmit Jabber Timeout 0x1 (ACTIVE): Transmit Jabber Timeout occurred Value After Reset: 0x0

2.3.22 EQOS_MAC_R_MAC_LPI_CONTROL_STATUS

Access Type: RW

Address Offset: 0xd0

Name	Access	Bit Range	Reset value	Description
RESERVED_31_22	R	[31:22]	0x0	Reserved. Value After Reset: 0x0
LPITCSE	R/W	[21:21]	0x0	LPI Tx Clock Stop Enable When this bit is set, the MAC asserts sbd_tx_clk_gating_ctrl_o signal high after it enters Tx LPI mode to indicate that the Tx clock to MAC can be stopped. When this bit is reset, the MAC does not assert sbd_tx_clk_gating_ctrl_o signal high after it enters

				Tx LPI mode. If RGMII Interface is selected, the Tx clock is required for transmitting the LPI pattern. The Tx Clock cannot be gated and so the LPITCSE bit cannot be programmed.Values: 0x0 (DISABLE): LPI Tx Clock Stop is disabled 0x1 (ENABLE): LPI Tx Clock Stop is enabled Value After Reset: 0x0
LPIATE	R/W	[20:20]	0x0	LPI Timer Enable This bit controls the automatic entry of the MAC Transmitter into and exit out of the LPI state. When LPIATE, LPITXA and LPIEN bits are set, the MAC Transmitter enters LPI state only when the complete MAC TX data path is IDLE for a period indicated by the MAC_LPI_Entry_Timer register. After entering LPI state, if the data path becomes non-IDLE (due to a new packet being accepted for transmission), the Transmitter exits LPI state but does not clear LPIEN bit. This enables the re-entry into LPI state when it is IDLE again. When LPIATE is 0, the LPI Auto timer is disabled and MAC Transmitter enters LPI state based on the settings of LPITXA and LPIEN bit descriptions.Values: 0x0 (DISABLE): LPI Timer is disabled 0x1 (ENABLE): LPI Timer is enabled Value After Reset: 0x0
LPITXA	R/W	[19:19]	0x0	LPI Tx Automate This bit controls the behavior of the MAC when it is entering or coming out of the LPI mode on the Transmit side. This bit is not functional in the EQOS-CORE configurations in which the Tx clock

				gating is done during the LPI mode. If the LPITXA and LPIEN bits are set to 1, the MAC enters the LPI mode only after all outstanding packets (in the core) and pending packets (in the application interface) have been transmitted. The MAC comes out of the LPI mode when the application sends any packet for transmission or the application issues a Tx FIFO Flush command. In addition, the MAC automatically clears the LPIEN bit when it exits the LPI state. If Tx FIFO Flush is set in the FTQ bit of MTL_TxQ0_Operation_Mode register, when the MAC is in the LPI mode, it exits the LPI mode. When this bit is 0, the LPIEN bit directly controls behavior of the MAC when it is entering or coming out of the LPI mode.Values: 0x0 (DISABLE): LPI Tx Automate is disabled 0x1 (ENABLE): LPI Tx Automate is enabled Value After Reset: 0x0
PLSEN	R/W	[18:18]	0x0	PHY Link Status Enable This bit enables the link status received on the RGMII, SGMII, or SMII Receive paths to be used for activating the LPI LS TIMER. When this bit is set, the MAC uses the link-status bits of the MAC_PHYIF_Control_Status register and the PLS bit for the LPI LS Timer trigger. When this bit is reset, the MAC ignores the link-status bits of the MAC_PHYIF_Control_Status register and takes only the PLS bit.Values: 0x0 (DISABLE): PHY Link Status is disabled 0x1 (ENABLE): PHY Link Status is enabled Value After Reset: 0x0
PLS	R/W	[17:17]	0x0	PHY Link Status

				This bit indicates the link status of the PHY. The MAC Transmitter asserts the LPI pattern only when the link status is up (OKAY) at least for the time indicated by the LPI LS TIMER. When this bit is set, the link is considered to be okay (UP) and when this bit is reset, the link is considered to be down.Values: 0x0 (DISABLE): link is down 0x1 (ENABLE): link is okay (UP) Value After Reset: 0x0
LPIEN	R/W	[16:16]	0x0	LPI Enable When this bit is set, it instructs the MAC Transmitter to enter the LPI state. When this bit is reset, it instructs the MAC to exit the LPI state and resume normal transmission. This bit is cleared when the LPITXA bit is set and the MAC exits the LPI state because of the arrival of a new packet for transmission.Values: 0x0 (DISABLE): LPI state is disabled 0x1 (ENABLE): LPI state is enabled Value After Reset: 0x0
RESERVED_15_10	R	[15:10]	0x0	Reserved. Value After Reset: 0x0
RLPIST	R	[9:9]	0x0	Receive LPI State When this bit is set, it indicates that the MAC is receiving the LPI pattern on the GMII or MII interface.Values: 0x0 (INACTIVE): Receive LPI state not detected 0x1 (ACTIVE): Receive LPI state detected

				Value After Reset: 0x0
TLPIST	R	[8:8]	0x0	Transmit LPI State When this bit is set, it indicates that the MAC is transmitting the LPI pattern on the GMII or MII interface.Values: 0x0 (INACTIVE): Transmit LPI state not detected 0x1 (ACTIVE): Transmit LPI state detected Value After Reset: 0x0
RESERVED_7_4	R	[7:4]	0x0	Reserved. Value After Reset: 0x0
RLPIEX	R	[3:3]	0x0	Receive LPI Exit When this bit is set, it indicates that the MAC Receiver has stopped receiving the LPI pattern on the GMII or MII interface, exited the LPI state, and resumed the normal reception. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Note: This bit might not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock.Values: 0x0 (INACTIVE): Receive LPI exit not detected 0x1 (ACTIVE): Receive LPI exit detected Value After Reset: 0x0
RLPIEN	R	[2:2]	0x0	Receive LPI Entry When this bit is set, it indicates that the MAC Receiver has received an LPI pattern and entered the LPI state. This bit is cleared by a read into this

				register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Note: This bit might not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock.Values: 0x0 (INACTIVE): Receive LPI entry not detected 0x1 (ACTIVE): Receive LPI entry detected Value After Reset: 0x0
TLPIEX	R	[1:1]	0x0	Transmit LPI Exit When this bit is set, it indicates that the MAC transmitter exited the LPI state after the application cleared the LPIEN bit and the LPI TW Timer has expired. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set).Values: 0x0 (INACTIVE): Transmit LPI exit not detected 0x1 (ACTIVE): Transmit LPI exit detected Value After Reset: 0x0
TLPIEN	R	[0:0]	0x0	Transmit LPI Entry When this bit is set, it indicates that the MAC Transmitter has entered the LPI state because of the setting of the LPIEN bit. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set).Values: 0x0 (INACTIVE): Transmit LPI entry not detected 0x1 (ACTIVE): Transmit LPI entry detected Value After Reset: 0x0

2.3.23 EQOS_MAC_R_MAC_LPI_TIMERS_CONTROL

Access Type: RW

Address Offset: 0xd4

Name	Access	Bit Range	Reset value	Description
RESERVED_31_26	R	[31:26]	0x0	Reserved. Value After Reset: 0x0
LST	R/W	[25:16]	0x3e8	LPI LS Timer This field specifies the minimum time (in milliseconds) for which the link status from the PHY should be up (OKAY) before the LPI pattern can be transmitted to the PHY. The MAC does not transmit the LPI pattern even when the LPIEN bit is set unless the LPI LS Timer reaches the programmed terminal count. The default value of the LPI LS Timer is 1000 (1 sec) as defined in the IEEE standard. Value After Reset: 0x3e8
TWT	R/W	[15:0]	0x0	LPI TW Timer This field specifies the minimum time (in microseconds) for which the MAC waits after it stops transmitting the LPI pattern to the PHY and before it resumes the normal transmission. The TLPIEX status bit is set after the expiry of this timer. Value After Reset: 0x0

2.3.24 EQOS_MAC_R_MAC_LPI_ENTRY_TIMER

Access Type: RW

Address Offset: 0xd8

Name	Access	Bit Range	Reset value	Description
RESERVED_31_20	R	[31:20]	0x0	Reserved. Value After Reset: 0x0
LPIET	R/W	[19:3]	0x0	LPI Entry Timer This field specifies the time in microseconds the MAC waits to enter LPI mode, after it has transmitted all the frames. This field is valid and

				used only when LPITE and LPITXA are set to 1. Bits [2:0] are read-only so that the granularity of this timer is in steps of 8 micro-seconds. Value After Reset: 0x0
RESERVED_2_0	R	[2:0]	0x0	Reserved. Value After Reset: 0x0

2.3.25 EQOS_MAC_R_MAC_1US_TIC_COUNTER

Access Type: RW

Address Offset: 0xdc

Name	Access	Bit Range	Reset value	Description
RESERVED_31_12	R	[31:12]	0x0	Reserved. Value After Reset: 0x0
TIC_1US_CNTR	R/W	[11:0]	0x63	1US TIC Counter The application must program this counter so that the number of clock cycles of CSR clock is 1us. (Subtract 1 from the value before programming). For example if the CSR clock is 100MHz then this field needs to be programmed to value 100 - 1 = 99 (which is 0x63). This is required to generate the 1US events that are used to update some of the EEE related counters. Value After Reset: 0x63

2.3.26 EQOS_MAC_R_MAC_PHYIF_CONTROL_STATUS

Access Type: RW

Address Offset: 0xf8

Name	Access	Bit Range	Reset value	Description
RESERVED_31_22	R	[31:22]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[21:20]	0x0	Reserved Field: Yes
LNKSTS	R	[19:19]	0x0	Link Status This bit indicates whether the link is up (1'b1) or down (1'b0).Values:

				0x0 (INACTIVE): Link down 0x1 (ACTIVE): Link up Value After Reset: 0x0 Testable: untestable
LNKSPEED	R	[18:17]	0x0	Link Speed This bit indicates the current speed of the link.Values: 0x0 (M_2500K): 2.5 MHz 0x1 (M_25M): 25 MHz 0x2 (M_125M): 125 MHz 0x3 (RSVD): Reserved Value After Reset: 0x0 Testable: untestable
LNKMOD	R	[16:16]	0x0	Link Mode This bit indicates the current mode of operation of the link.Values: 0x0 (HDUPLX): Half-duplex mode 0x1 (FDUPLX): Full-duplex mode Value After Reset: 0x0 Testable: untestable
RESERVED_15_5	R	[15:5]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[4:4]	0x0	Reserved Field: Yes
RESERVED_3	R	[3:3]	0x0	Reserved. Value After Reset: 0x0

RESERVED	R	[2:2]	0x0	Reserved Field: Yes
LUD	R/W	[1:1]	0x0	Link Up or Down This bit indicates whether the link is up or down during transmission of configuration in the RGMII, SGMII, or SMII interface.Values: 0x0 (LINKDOWN): Link down 0x1 (LINKUP): Link up Value After Reset: 0x0
TC	R/W	[0:0]	0x0	Transmit Configuration in RGMII, SGMII, or SMII When set, this bit enables the transmission of duplex mode, link speed, and link up or down information to the PHY in the RGMII, SMII, or SGMII port. When this bit is reset, no such information is driven to the PHY. The details of this feature are provided in the following sections: "Reduced Gigabit Media Independent Interface" "Serial Media Independent Interface" "Serial Gigabit Media Independent Interface" Values: 0x0 (DISABLE): Disable Transmit Configuration in RGMII, SGMII, or SMII 0x1 (ENABLE): Enable Transmit Configuration in RGMII, SGMII, or SMII Value After Reset: 0x0

2.3.27 EQOS_MAC_R_MAC_VERSION

Access Type: RW

Address Offset: 0x110

Name	Access	Bit	Reset	Description

		Range	value	
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
USERVER	R	[15:8]	0x10	User-defined Version (configured with coreConsultant) Value After Reset: 0x10
SNPSVER	R	[7:0]	0x51	Synopsys-defined Version Value After Reset: 0x51

2.3.28 EQOS_MAC_R_MAC_DEBUG

Access Type: RW

Address Offset: 0x114

Name	Access	Bit Range	Reset value	Description
RESERVED_31_19	R	[31:19]	0x0	Reserved. Value After Reset: 0x0
TFCSTS	R	[18:17]	0x0	MAC Transmit Packet Controller Status This field indicates the state of the MAC Transmit Packet Controller module.Values: 0x0 (IDLE): Idle state 0x1 (WAITING): Waiting for one of the following: Status of the previous packet OR IPG or back off period to be over 0x2 (GEN_TX_PAU): Generating and transmitting a Pause control packet (in full-duplex mode) 0x3 (TRNSFR): Transferring input packet for transmission Value After Reset: 0x0
TPESTS	R	[16:16]	0x0	MAC GMII or MII Transmit Protocol Engine

				Status When this bit is set, it indicates that the MAC GMII or MII transmit protocol engine is actively transmitting data, and it is not in the Idle state.Values: 0x0 (INACTIVE): MAC GMII or MII Transmit Protocol Engine Status not detected 0x1 (ACTIVE): MAC GMII or MII Transmit Protocol Engine Status detected Value After Reset: 0x0
RESERVED_15_3	R	[15:3]	0x0	Reserved. Value After Reset: 0x0
RFCFCSTS	R	[2:1]	0x0	MAC Receive Packet Controller FIFO Status When this bit is set, this field indicates the active state of the small FIFO Read and Write controllers of the MAC Receive Packet Controller module. Value After Reset: 0x0
RPESTS	R	[0:0]	0x0	MAC GMII or MII Receive Protocol Engine Status When this bit is set, it indicates that the MAC GMII or MII receive protocol engine is actively receiving data, and it is not in the Idle state.Values: 0x0 (INACTIVE): MAC GMII or MII Receive Protocol Engine Status not detected 0x1 (ACTIVE): MAC GMII or MII Receive Protocol Engine Status detected Value After Reset: 0x0

2.3.29 EQOS_MAC_R_MAC_HW_FEATURE0

Access Type: RW

Address Offset: 0x11c

Name	Access	Bit Range	Reset value	Description
RESERVED_31	R	[31:31]	0x0	Reserved. Value After Reset: 0x0
ACTPHYSEL	R	[30:28]	0x0	Active PHY Selected When you have multiple PHY interfaces in your configuration, this field indicates the sampled value of phy_intf_sel_i during reset de-assertion.Values: 0x0 (GMII_MII): GMII or MII 0x1 (RGMII): RGMII 0x2 (SGMII): SGMII 0x3 (TBI): TBI 0x4 (RMII): RMII 0x5 (RTBI): RTBI 0x6 (SMII): SMII 0x7 (REVMIII): RevMII Value After Reset: 0x0
SAVLANINS	R	[27:27]	0x1	Source Address or VLAN Insertion Enable This bit is set to 1 when the Enable SA and VLAN Insertion on Tx option is selectedValues: 0x0 (INACTIVE): Source Address or VLAN Insertion Enable option is not selected 0x1 (ACTIVE): Source Address or VLAN Insertion Enable option is selected Value After Reset: 0x1

TSSTSSEL	R	[26:25]	0x3	Timestamp System Time Source This bit indicates the source of the Timestamp system time: This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selectedValues: 0x0 (INTRNL): Internal 0x1 (EXTRNL): External 0x2 (BOTH): Both 0x3 (RSVD): Reserved Value After Reset: 0x3
MACADR64SEL	R	[24:24]	0x0	MAC Addresses 64-127 Selected This bit is set to 1 when the Enable Additional 64 MAC Address Registers (64-127) option is selectedValues: 0x0 (INACTIVE): MAC Addresses 64-127 Select option is not selected 0x1 (ACTIVE): MAC Addresses 64-127 Select option is selected Value After Reset: 0x0
MACADR32SEL	R	[23:23]	0x0	MAC Addresses 32-63 Selected This bit is set to 1 when the Enable Additional 32 MAC Address Registers (32-63) option is selectedValues: 0x0 (INACTIVE): MAC Addresses 32-63 Select option is not selected 0x1 (ACTIVE): MAC Addresses 32-63 Select option is selected

				Value After Reset: 0x0
ADDMACADRSEL	R	[22:18]	0x7	MAC Addresses 1-31 Selected This bit is set to 1 when the non-zero value is selected for Enable Additional 1-31 MAC Address Registers option Value After Reset: 0x7
RESERVED_17	R	[17:17]	0x0	Reserved. Value After Reset: 0x0
RXCOESEL	R	[16:16]	0x1	Receive Checksum Offload Enabled This bit is set to 1 when the Enable Receive TCP/IP Checksum Check option is selectedValues: 0x0 (INACTIVE): Receive Checksum Offload Enable option is not selected 0x1 (ACTIVE): Receive Checksum Offload Enable option is selected Value After Reset: 0x1
RESERVED_15	R	[15:15]	0x0	Reserved. Value After Reset: 0x0
TXCOESEL	R	[14:14]	0x1	Transmit Checksum Offload Enabled This bit is set to 1 when the Enable Transmit TCP/IP Checksum Insertion option is selectedValues: 0x0 (INACTIVE): Transmit Checksum Offload Enable option is not selected 0x1 (ACTIVE): Transmit Checksum Offload Enable option is selected Value After Reset: 0x1

EEESEL	R	[13:13]	0x1	Energy Efficient Ethernet Enabled This bit is set to 1 when the Enable Energy Efficient Ethernet (EEE) option is selectedValues: 0x0 (INACTIVE): Energy Efficient Ethernet Enable option is not selected 0x1 (ACTIVE): Energy Efficient Ethernet Enable option is selected Value After Reset: 0x1
TSSEL	R	[12:12]	0x1	IEEE 1588-2008 Timestamp Enabled This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selectedValues: 0x0 (INACTIVE): IEEE 1588-2008 Timestamp Enable option is not selected 0x1 (ACTIVE): IEEE 1588-2008 Timestamp Enable option is selected Value After Reset: 0x1
RESERVED_11_10	R	[11:10]	0x0	Reserved. Value After Reset: 0x0
ARPOFFSEL	R	[9:9]	0x0	ARP Offload Enabled This bit is set to 1 when the Enable IPv4 ARP Offload option is selectedValues: 0x0 (INACTIVE): ARP Offload Enable option is not selected 0x1 (ACTIVE): ARP Offload Enable option is selected Value After Reset: 0x0

MMCSEL	R	[8:8]	0x1	RMON Module Enable This bit is set to 1 when the Enable MAC Management Counters (MMC) option is selectedValues: 0x0 (INACTIVE): RMON Module Enable option is not selected 0x1 (ACTIVE): RMON Module Enable option is selected Value After Reset: 0x1
MGKSEL	R	[7:7]	0x0	PMT Magic Packet Enable This bit is set to 1 when the Enable Magic Packet Detection option is selectedValues: 0x0 (INACTIVE): PMT Magic Packet Enable option is not selected 0x1 (ACTIVE): PMT Magic Packet Enable option is selected Value After Reset: 0x0
RWKSEL	R	[6:6]	0x0	PMT Remote Wake-up Packet Enable This bit is set to 1 when the Enable Remote Wake-Up Packet Detection option is selectedValues: 0x0 (INACTIVE): PMT Remote Wake-up Packet Enable option is not selected 0x1 (ACTIVE): PMT Remote Wake-up Packet Enable option is selected Value After Reset: 0x0
SMASEL	R	[5:5]	0x1	SMA (MDIO) Interface

				This bit is set to 1 when the Enable Station Management (MDIO Interface) option is selectedValues: 0x0 (INACTIVE): SMA (MDIO) Interface not selected 0x1 (ACTIVE): SMA (MDIO) Interface selected Value After Reset: 0x1
VLHASH	R	[4:4]	0x1	VLAN Hash Filter Selected This bit is set to 1 when the Enable VLAN Hash Table Based Filtering option is selectedValues: 0x0 (INACTIVE): VLAN Hash Filter not selected 0x1 (ACTIVE): VLAN Hash Filter selected Value After Reset: 0x1
PCSSEL	R	[3:3]	0x0	PCS Registers (TBI, SGMII, or RTBI PHY interface) This bit is set to 1 when the TBI, SGMII, or RTBI PHY interface option is selectedValues: 0x0 (INACTIVE): No PCS Registers (TBI, SGMII, or RTBI PHY interface) 0x1 (ACTIVE): PCS Registers (TBI, SGMII, or RTBI PHY interface) Value After Reset: 0x0
HDSEL	R	[2:2]	0x0	Half-duplex Support This bit is set to 1 when the half-duplex mode is selectedValues: 0x0 (INACTIVE): No Half-duplex support

				0x1 (ACTIVE): Half-duplex support Value After Reset: 0x0
GMIISEL	R	[1:1]	0x1	1000 Mbps Support This bit is set to 1 when 1000 Mbps is selected as the Mode of OperationValues: 0x0 (INACTIVE): No 1000 Mbps support 0x1 (ACTIVE): 1000 Mbps support Value After Reset: 0x1
MIISEL	R	[0:0]	0x1	10 or 100 Mbps Support This bit is set to 1 when 10/100 Mbps is selected as the Mode of OperationValues: 0x0 (INACTIVE): No 10 or 100 Mbps support 0x1 (ACTIVE): 10 or 100 Mbps support Value After Reset: 0x1

2.3.30 EQOS_MAC_R_MAC_HW_FEATURE1

Access Type: RW

Address Offset: 0x120

Name	Access	Bit Range	Reset value	Description
RESERVED_31	R	[31:31]	0x0	Reserved. Value After Reset: 0x0
L3L4FNUM	R	[30:27]	0x2	Total number of L3 or L4 Filters This field indicates the total number of L3 or L4 filters:Values: 0x0 (NOFILT): No L3 or L4 Filter

				0x1 (M_1FILT): 1 L3 or L4 Filter 0x2 (M_2FILT): 2 L3 or L4 Filters 0x3 (M_3FILT): 3 L3 or L4 Filters 0x4 (M_4FILT): 4 L3 or L4 Filters 0x5 (M_5FILT): 5 L3 or L4 Filters 0x6 (M_6FILT): 6 L3 or L4 Filters 0x7 (M_7FILT): 7 L3 or L4 Filters 0x8 (M_8FILT): 8 L3 or L4 Filters Value After Reset: 0x2
RESERVED_26	R	[26:26]	0x0	Reserved. Value After Reset: 0x0
HASHTBLSZ	R	[25:24]	0x1	Hash Table Size This field indicates the size of the hash table:Values: 0x0 (NO_HT): No hash table 0x1 (M_64): 64 0x2 (M_128): 128 0x3 (M_256): 256 Value After Reset: 0x1
POUOST	R	[23:23]	0x0	One Step for PTP over UDP/IP Feature Enable This bit is set to 1 when the Enable One step timestamp for PTP over UDP/IP feature is selected.Values: 0x0 (INACTIVE): One Step for PTP over UDP/IP Feature is not selected

				0x1 (ACTIVE): One Step for PTP over UDP/IP Feature is selected Value After Reset: 0x0
RESERVED_22	R	[22:22]	0x0	Reserved. Value After Reset: 0x0
RAVSEL	R	[21:21]	0x0	Rx Side Only AV Feature Enable This bit is set to 1 when the Enable Audio Video Bridging option on Rx Side Only is selected.Values: 0x0 (INACTIVE): Rx Side Only AV Feature is not selected 0x1 (ACTIVE): Rx Side Only AV Feature is selected Value After Reset: 0x0
AVSEL	R	[20:20]	0x1	AV Feature Enable This bit is set to 1 when the Enable Audio Video Bridging option is selected.Values: 0x0 (INACTIVE): AV Feature is not selected 0x1 (ACTIVE): AV Feature is selected Value After Reset: 0x1
DBGMEMA	R	[19:19]	0x1	DMA Debug Registers Enable This bit is set to 1 when the Debug Mode Enable option is selectedValues: 0x0 (INACTIVE): DMA Debug Registers option is not selected 0x1 (ACTIVE): DMA Debug Registers option is selected

				Value After Reset: 0x1
TSOEN	R	[18:18]	0x0	TCP Segmentation Offload Enable This bit is set to 1 when the Enable TCP Segmentation Offloading for TCP/IP Packets option is selectedValues: 0x0 (INACTIVE): TCP Segmentation Offload Feature is not selected 0x1 (ACTIVE): TCP Segmentation Offload Feature is selected Value After Reset: 0x0
SPHEN	R	[17:17]	0x1	Split Header Feature Enable This bit is set to 1 when the Enable Split Header Structure option is selectedValues: 0x0 (INACTIVE): Split Header Feature is not selected 0x1 (ACTIVE): Split Header Feature is selected Value After Reset: 0x1
DCBEN	R	[16:16]	0x0	DCB Feature Enable This bit is set to 1 when the Enable Data Center Bridging option is selectedValues: 0x0 (INACTIVE): DCB Feature is not selected 0x1 (ACTIVE): DCB Feature is selected Value After Reset: 0x0
ADDR64	R	[15:14]	0x1	Address Width.

				This field indicates the configured address width:Values: 0x0 (M_32): 32 0x1 (M_40): 40 0x2 (M_48): 48 0x3 (RSVD): Reserved Value After Reset: 0x1
ADVTHWORD	R	[13:13]	0x1	IEEE 1588 High Word Register Enable This bit is set to 1 when the Add IEEE 1588 Higher Word Register option is selectedValues: 0x0 (INACTIVE): IEEE 1588 High Word Register option is not selected 0x1 (ACTIVE): IEEE 1588 High Word Register option is selected Value After Reset: 0x1
PTOEN	R	[12:12]	0x0	PTP Offload Enable This bit is set to 1 when the Enable PTP Timestamp Offload Feature is selected.Values: 0x0 (INACTIVE): PTP Offload feature is not selected 0x1 (ACTIVE): PTP Offload feature is selected Value After Reset: 0x0
OSTEN	R	[11:11]	0x1	One-Step Timestamping Enable This bit is set to 1 when the Enable One-Step Timestamp Feature is selected.Values:

				0x0 (INACTIVE): One-Step Timestamping feature is not selected 0x1 (ACTIVE): One-Step Timestamping feature is selected Value After Reset: 0x1
TXFIFOSIZE	R	[10:6]	0x7	MTL Transmit FIFO Size This field contains the configured value of MTL Tx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(TXFIFO_SIZE) -7:Values: 0x0 (M_128B): 128 bytes 0x1 (M_256B): 256 bytes 0x2 (M_512B): 512 bytes 0x3 (M_1024B): 1024 bytes 0x4 (M_2048B): 2048 bytes 0x5 (M_4096B): 4096 bytes 0x6 (M_8192B): 8192 bytes 0x7 (M_16384B): 16384 bytes 0x8 (M_32KB): 32 KB 0x9 (M_64KB): 64 KB 0xa (M_128KB): 128 KB 0xb (RSVD): Reserved Value After Reset: 0x7
SPRAM	R	[5:5]	0x0	Single Port RAM Enable This bit is set to 1 when the Use single port RAM

				Feature is selected.Values: 0x0 (INACTIVE): Single Port RAM feature is not selected 0x1 (ACTIVE): Single Port RAM feature is selected Value After Reset: 0x0
RXFIFOSIZE	R	[4:0]	0x7	MTL Receive FIFO Size This field contains the configured value of MTL Rx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(RXFIFO_SIZE) -7:Values: 0x0 (M_128B): 128 bytes 0x1 (M_256B): 256 bytes 0x2 (M_512B): 512 bytes 0x3 (M_1024B): 1024 bytes 0x4 (M_2048B): 2048 bytes 0x5 (M_4096B): 4096 bytes 0x6 (M_8192B): 8192 bytes 0x7 (M_16384B): 16384 bytes 0x8 (M_32KB): 32 KB 0x9 (M_64KB): 64 KB 0xa (M_128KB): 128 KB 0xb (M_256KB): 256 KB 0xc (RSVD): Reserved Value After Reset: 0x7

2.3.31 EQOS_MAC_R_MAC_HW_FEATURE2

Access Type: RW

Address Offset: 0x124

Name	Access	Bit Range	Reset value	Description
RESERVED_31	R	[31:31]	0x0	Reserved. Value After Reset: 0x0
AUXSNAPNUM	R	[30:28]	0x2	Number of Auxiliary Snapshot Inputs This field indicates the number of auxiliary snapshot inputs:Values: 0x0 (NO_AUXI): No auxiliary input 0x1 (M_1_AUXI): 1 auxiliary input 0x2 (M_2_AUXI): 2 auxiliary input 0x3 (M_3_AUXI): 3 auxiliary input 0x4 (M_4_AUXI): 4 auxiliary input 0x5 (RSVD): Reserved Value After Reset: 0x2
RESERVED_27	R	[27:27]	0x0	Reserved. Value After Reset: 0x0
PPSOUTNUM	R	[26:24]	0x0	Number of PPS Outputs This field indicates the number of PPS outputs:Values: 0x0 (NO_PPSO): No PPS output 0x1 (M_1_PPSO): 1 PPS output 0x2 (M_2_PPSO): 2 PPS output 0x3 (M_3_PPSO): 3 PPS output

				0x4 (M_4_PPSO): 4 PPS output 0x5 (RSVD): Reserved Value After Reset: 0x0
RESERVED_23_22	R	[23:22]	0x0	Reserved. Value After Reset: 0x0
TXCHCNT	R	[21:18]	0x3	Number of DMA Transmit Channels This field indicates the number of DMA Transmit channels:Values: 0x0 (M_1TXCH): 1 MTL Tx Channel 0x1 (M_2TXCH): 2 MTL Tx Channels 0x2 (M_3TXCH): 3 MTL Tx Channels 0x3 (M_4TXCH): 4 MTL Tx Channels 0x4 (M_5TXCH): 5 MTL Tx Channels 0x5 (M_6TXCH): 6 MTL Tx Channels 0x6 (M_7TXCH): 7 MTL Tx Channels 0x7 (M_8TXCH): 8 MTL Tx Channels Value After Reset: 0x3
RESERVED_17_16	R	[17:16]	0x0	Reserved. Value After Reset: 0x0
RXCHCNT	R	[15:12]	0x3	Number of DMA Receive Channels This field indicates the number of DMA Receive channels:Values: 0x0 (M_1RXCH): 1 MTL Rx Channel

				0x1 (M_2RXCH): 2 MTL Rx Channels 0x2 (M_3RXCH): 3 MTL Rx Channels 0x3 (M_4RXCH): 4 MTL Rx Channels 0x4 (M_5RXCH): 5 MTL Rx Channels 0x5 (M_6RXCH): 6 MTL Rx Channels 0x6 (M_7RXCH): 7 MTL Rx Channels 0x7 (M_8RXCH): 8 MTL Rx Channels Value After Reset: 0x3
RESERVED_11_10	R	[11:10]	0x0	Reserved. Value After Reset: 0x0
TXQCNT	R	[9:6]	0x3	Number of MTL Transmit Queues This field indicates the number of MTL Transmit queues:Values: 0x0 (M_1TXQ): 1 MTL Tx Queue 0x1 (M_2TXQ): 2 MTL Tx Queues 0x2 (M_3TXQ): 3 MTL Tx Queues 0x3 (M_4TXQ): 4 MTL Tx Queues 0x4 (M_5TXQ): 5 MTL Tx Queues 0x5 (M_6TXQ): 6 MTL Tx Queues 0x6 (M_7TXQ): 7 MTL Tx Queues 0x7 (M_8TXQ): 8 MTL Tx Queues Value After Reset: 0x3

RESERVED_5_4	R	[5:4]	0x0	Reserved. Value After Reset: 0x0
RXQCNT	R	[3:0]	0x3	Number of MTL Receive Queues This field indicates the number of MTL Receive queues:Values: 0x0 (M_1RXQ): 1 MTL Rx Queue 0x1 (M_2RXQ): 2 MTL Rx Queues 0x2 (M_3RXQ): 3 MTL Rx Queues 0x3 (M_4RXQ): 4 MTL Rx Queues 0x4 (M_5RXQ): 5 MTL Rx Queues 0x5 (M_6RXQ): 6 MTL Rx Queues 0x6 (M_7RXQ): 7 MTL Rx Queues 0x7 (M_8RXQ): 8 MTL Rx Queues Value After Reset: 0x3

2.3.32 EQOS_MAC_R_MAC_HW_FEATURE3

Access Type: RW

Address Offset: 0x128

Name	Access	Bit Range	Reset value	Description
RESERVED_31_30	R	[31:30]	0x0	Reserved. Value After Reset: 0x0
ASP	R	[29:28]	0x3	Automotive Safety Package Following are the encoding for the different Safety featuresValues: 0x0 (NONE): No Safety features selected 0x1 (ECC_ONLY): Only "ECC protection for

				external memory" feature is selected 0x2 (AS_NPPE): All the Automotive Safety features are selected without the "Parity Port Enable for external interface" feature 0x3 (AS_PPE): All the Automotive Safety features are selected with the "Parity Port Enable for external interface" feature Value After Reset: 0x3
TBSSEL	R	[27:27]	0x1	Time Based Scheduling Enable This bit is set to 1 when the Time Based Scheduling feature is selected.Values: 0x0 (INACTIVE): Time Based Scheduling Enable feature is not selected 0x1 (ACTIVE): Time Based Scheduling Enable feature is selected Value After Reset: 0x1
FPESEL	R	[26:26]	0x1	Frame Preemption Enable This bit is set to 1 when the Enable Frame preemption feature is selected.Values: 0x0 (INACTIVE): Frame Preemption Enable feature is not selected 0x1 (ACTIVE): Frame Preemption Enable feature is selected Value After Reset: 0x1
RESERVED_25_22	R	[25:22]	0x0	Reserved. Value After Reset: 0x0
ESTWID	R	[21:20]	0x3	

				Width of the Time Interval field in the Gate Control List This field indicates the width of the Configured Time Interval FieldValues: 0x0 (NOWIDTH): Width not configured 0x1 (WIDTH16): 16 0x2 (WIDTH20): 20 0x3 (WIDTH24): 24 Value After Reset: 0x3
ESTDEP	R	[19:17]	0x3	Depth of the Gate Control List This field indicates the depth of Gate Control list expressed as Log2(DWC_EQOS_EST_DEP)-5Values: 0x0 (NODEPTH): No Depth configured 0x1 (DEPTH64): 64 0x2 (DEPTH128): 128 0x3 (DEPTH256): 256 0x4 (DEPTH512): 512 0x5 (DEPTH1024): 1024 0x6 (RSVD): Reserved Value After Reset: 0x3
ESTSEL	R	[16:16]	0x1	Enhancements to Scheduling Traffic Enable This bit is set to 1 when the Enable Enhancements to Scheduling Traffic feature is selected.Values: 0x0 (INACTIVE): Enable Enhancements to

				Scheduling Traffic feature is not selected 0x1 (ACTIVE): Enable Enhancements to Scheduling Traffic feature is selected Value After Reset: 0x1
RESERVED_15	R	[15:15]	0x0	Reserved. Value After Reset: 0x0
FRPES	R	[14:13]	0x0	Flexible Receive Parser Table Entries size This field indicates the Max Number of Parser Entries supported by Flexible Receive Parser.Values: 0x0 (M_64ENTR): 64 Entries 0x1 (M_128ENTR): 128 Entries 0x2 (M_256ENTR): 256 Entries 0x3 (RSVD): Reserved Value After Reset: 0x0
FRPBS	R	[12:11]	0x0	Flexible Receive Parser Buffer size This field indicates the supported Max Number of bytes of the packet data to be Parsed by Flexible Receive Parser.Values: 0x0 (M_64BYTES): 64 Bytes 0x1 (M_128BYTES): 128 Bytes 0x2 (M_256BYTES): 256 Bytes 0x3 (RSVD): Reserved Value After Reset: 0x0

FRPSEL	R	[10:10]	0x0	Flexible Receive Parser Selected This bit is set to 1 when the Enable Flexible Programmable Receive Parser option is selected.Values: 0x0 (INACTIVE): Flexible Receive Parser feature is not selected 0x1 (ACTIVE): Flexible Receive Parser feature is selected Value After Reset: 0x0
PDUPSEL	R	[9:9]	0x0	Broadcast/Multicast Packet Duplication This bit is set to 1 when the Broadcast/Multicast Packet Duplication feature is selected.Values: 0x0 (INACTIVE): Broadcast/Multicast Packet Duplication feature is not selected 0x1 (ACTIVE): Broadcast/Multicast Packet Duplication feature is selected Value After Reset: 0x0
RESERVED_7_6	R	[8:6]	0x0	Reserved. Value After Reset: 0x0
DVLAN	R	[5:5]	0x0	Double VLAN Tag Processing Selected This bit is set to 1 when the Enable Double VLAN Processing Feature is selected.Values: 0x0 (INACTIVE): Double VLAN option is not selected 0x1 (ACTIVE): Double VLAN option is selected Value After Reset: 0x0

CBTISEL	R	[4:4]	0x1	Queue/Channel based VLAN tag insertion on Tx Enable This bit is set to 1 when the Enable Queue/Channel based VLAN tag insertion on Tx Feature is selected.Values: 0x0 (INACTIVE): Enable Queue/Channel based VLAN tag insertion on Tx feature is not selected 0x1 (ACTIVE): Enable Queue/Channel based VLAN tag insertion on Tx feature is selected Value After Reset: 0x1
RESERVED_3	R	[3:3]	0x0	Reserved. Value After Reset: 0x0
NRVF	R	[2:0]	0x2	Number of Extended VLAN Tag Filters Enabled This field indicates the Number of Extended VLAN Tag Filters selected:Values: 0x0 (NO_ERVLAN): No Extended Rx VLAN Filters 0x1 (M_4_ERVLAN): 4 Extended Rx VLAN Filters 0x2 (M_8_ERVLAN): 8 Extended Rx VLAN Filters 0x3 (M_16_ERVLAN): 16 Extended Rx VLAN Filters 0x4 (M_24_ERVLAN): 24 Extended Rx VLAN Filters 0x5 (M_32_ERVLAN): 32 Extended Rx VLAN Filters 0x6 (RSVD): Reserved

				Value After Reset: 0x2

2.3.33 EQOS_MAC_R_MAC_DPP_FSM_INTERRUPT_STATUS

Access Type: RW

Address Offset: 0x140

Name	Access	Bit Range	Reset value	Description
RESERVED_31_25	R	[31:25]	0x0	Reserved. Value After Reset: 0x0
FSMPES	R/W	[24:24]	0x0	FSM State Parity Error Status This field when set indicates one of the FSMs State registers has a parity error detected.Values: 0x0 (INACTIVE): FSM State Parity Error Status not detected 0x1 (ACTIVE): FSM State Parity Error Status detected Value After Reset: 0x0 Testable: untestable
RESERVED_23_18	R	[23:18]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[17:17]	0x0	Reserved Field: Yes
MSTTES	R/W	[16:16]	0x0	Master Read/Write Timeout Error Status This field when set indicates that an Application/CSR Timeout has occurred on the master (AXI/AHB/ARI/ATI) interface.Values: 0x0 (INACTIVE): Master Read/Write Timeout Error Status not detected 0x1 (ACTIVE): Master Read/Write Timeout Error Status detected Value After Reset: 0x0

				Testable: untestable
RESERVED	R	[15:13]	0x0	Reserved Field: Yes
PTES	R/W	[12:12]	0x0	PTP FSM Timeout Error Status This field when set indicates that one of the PTP FSM Timeout has occurred.Values: 0x0 (INACTIVE): PTP FSM Timeout Error Status not detected 0x1 (ACTIVE): PTP FSM Timeout Error Status detected Value After Reset: 0x0 Testable: untestable
ATES	R/W	[11:11]	0x0	APP FSM Timeout Error Status This field when set indicates that one of the APP FSM Timeout has occurred.Values: 0x0 (INACTIVE): APP FSM Timeout Error Status not detected 0x1 (ACTIVE): APP FSM Timeout Error Status detected Value After Reset: 0x0 Testable: untestable
CTES	R/W	[10:10]	0x0	CSR FSM Timeout Error Status This field when set indicates that one of the CSR FSM Timeout has occurred.Values: 0x0 (INACTIVE): CSR FSM Timeout Error Status not detected 0x1 (ACTIVE): CSR FSM Timeout Error Status detected

				Value After Reset: 0x0 Testable: untestable
RTES	R/W	[9:9]	0x0	Rx FSM Timeout Error Status This field when set indicates that one of the Rx FSM Timeout has occurred.Values: 0x0 (INACTIVE): Rx FSM Timeout Error Status not detected 0x1 (ACTIVE): Rx FSM Timeout Error Status detected Value After Reset: 0x0 Testable: untestable
TTES	R/W	[8:8]	0x0	Tx FSM Timeout Error Status This field when set indicates that one of the Tx FSM Timeout has occurred.Values: 0x0 (INACTIVE): Tx FSM Timeout Error Status not detected 0x1 (ACTIVE): Tx FSM Timeout Error Status detected Value After Reset: 0x0 Testable: untestable
RESERVED	R	[7:6]	0x0	Reserved Field: Yes
ARPES	R/W	[5:5]	0x0	Application Receive interface data path Parity Error Status This bit when set indicates that a parity error is detected at following checkers based on the system configuration as described below In MTL configuration (DWC_EQOS_SYS=1), parity checker (PC6 as shown in Receive Data path Parity protection diagram) at ARI interface.

				In DMA configuration (DWC_EQOS_SYS=2), parity checker (PC6 as shown in Receive Data path Parity protection diagram) at DMA application interface. In AHB configuration (DWC_EQOS_SYS=3), parity checker (PC6 as shown in Receive Data path Parity protection diagram) at AHB master interface. In AXI configuration (DWC_EQOS_SYS=4), parity checker (PC6 as shown in Receive Data path Parity protection diagram) at AXI master interface. Values: 0x0 (INACTIVE): Application Receive interface data path Parity Error Status not detected 0x1 (ACTIVE): Application Receive interface data path Parity Error Status detected Value After Reset: 0x0 Testable: untestable
MTSPES	R/W	[4:4]	0x0	MTL TX Status data path Parity checker Error Status This filed when set indicates that, parity error is detected on the MTL TX Status data on ati interface (or at PC5 as shown in Transmit data path parity protection diagram).Values: 0x0 (INACTIVE): MTL TX Status data path Parity checker Error Status not detected 0x1 (ACTIVE): MTL TX Status data path Parity checker Error Status detected Value After Reset: 0x0 Testable: untestable
MPES	R/W	[3:3]	0x0	

				MTL data path Parity checker Error Status This bit when set indicates that a parity error is detected at the MTL transmit write controller parity checker (or at PC4 as shown in Transmit data path parity protection diagram).Values: 0x0 (INACTIVE): MTL data path Parity checker Error Status not detected 0x1 (ACTIVE): MTL data path Parity checker Error Status detected Value After Reset: 0x0 Testable: untestable
RDPES	R/W	[2:2]	0x0	Read Descriptor Parity checker Error Status This bit when set indicates that a parity error is detected at the DMA Read descriptor parity checker (or at PC3 as shown in Transmit data path parity protection diagram).Values: 0x0 (INACTIVE): Read Descriptor Parity checker Error Status not detected 0x1 (ACTIVE): Read Descriptor Parity checker Error Status detected Value After Reset: 0x0 Testable: untestable
RESERVED	R	[1:1]	0x0	Reserved Field: Yes
ATPES	R/W	[0:0]	0x0	Application Transmit Interface Parity checker Error Status This bit when set indicates that a parity error is detected on the AXI/AHB Master read data parity checker. This bit when set indicates that a parity error is detected on the interface port parity checker. Following are the checkers located based on the system configuration,

				In MTL configuration (DWC_EQOS_SYS=1), parity checker (PC1 as shown in Transmit data path parity protection diagram) at ATI interface. In DMA configuration (DWC_EQOS_SYS=2), parity checker (PC1 as shown in Transmit data path parity protection diagram) at DMA application interface. In AHB configuration (DWC_EQOS_SYS=3), parity checker (PC1 as shown in Transmit data path parity protection diagram) at AHB master interface. In AXI configuration (DWC_EQOS_SYS=4), parity checker (PC1 as shown in Transmit data path parity protection diagram) at AXI master interface. Values: 0x0 (INACTIVE): Application Transmit Interface Parity checker Error Status not detected 0x1 (ACTIVE): Application Transmit Interface Parity checker Error Status detected Value After Reset: 0x0 Testable: untestable

2.3.34 EQOS_MAC_R_MAC_FSM_CONTROL

Access Type: RW

Address Offset: 0x148

Name	Access	Bit Range	Reset value	Description
RESERVED	R	[31:29]	0x0	Reserved Field: Yes
PLGRNML	R/W	[28:28]	0x0	PTP Large/Normal Mode Select This field when set indicates that large mode tic generation is used for PTP domain, else normal mode tic generation is used.Values: 0x0 (DISABLE): normal mode tic generation is used for PTP domain

				0x1 (ENABLE): large mode tic generation is used for PTP domain Value After Reset: 0x0
ALGRNML	R/W	[27:27]	0x0	APP Large/Normal Mode Select This field when set indicates that large mode tic generation is used for APP domain, else normal mode tic generation is used.Values: 0x0 (DISABLE): normal mode tic generation is used for APP domain 0x1 (ENABLE): large mode tic generation is used for APP domain Value After Reset: 0x0
CLGRNML	R/W	[26:26]	0x0	CSR Large/Normal Mode Select This field when set indicates that large mode tic generation is used for CSR domain, else normal mode tic generation is used.Values: 0x0 (DISABLE): normal mode tic generation is used for CSR domain 0x1 (ENABLE): large mode tic generation is used for CSR domain Value After Reset: 0x0
RLGRNML	R/W	[25:25]	0x0	Rx Large/Normal Mode Select This field when set indicates that large mode tic generation is used for Rx domain, else normal mode tic generation is used.Values: 0x0 (DISABLE): normal mode tic generation is used for Rx domain

				0x1 (ENABLE): large mode tic generation is used for Rx domain Value After Reset: 0x0
TLGRNML	R/W	[24:24]	0x0	Tx Large/Normal Mode Select This field when set indicates that large mode tic generation is used for Tx domain, else normal mode tic generation is used.Values: 0x0 (DISABLE): normal mode tic generation is used for Tx domain 0x1 (ENABLE): large mode tic generation is used for Tx domain Value After Reset: 0x0
RESERVED	R	[23:21]	0x0	Reserved Field: Yes
PPEIN	R/W	[20:20]	0x0	PTP FSM Parity Error Injection This field when set indicates that Error Injection for PTP FSM Parity is enabled.Values: 0x0 (DISABLE): PTP FSM Parity Error Injection is disabled 0x1 (ENABLE): PTP FSM Parity Error Injection is enabled Value After Reset: 0x0
APEIN	R/W	[19:19]	0x0	APP FSM Parity Error Injection This field when set indicates that Error Injection for APP FSM Parity is enabled.Values: 0x0 (DISABLE): APP FSM Parity Error Injection is disabled 0x1 (ENABLE): APP FSM Parity Error Injection is

				enabled Value After Reset: 0x0
CPEIN	R/W	[18:18]	0x0	CSR FSM Parity Error Injection This field when set indicates that Error Injection for CSR Parity is enabled.Values: 0x0 (DISABLE): CSR FSM Parity Error Injection is disabled 0x1 (ENABLE): CSR FSM Parity Error Injection is enabled Value After Reset: 0x0
RPEIN	R/W	[17:17]	0x0	Rx FSM Parity Error Injection This field when set indicates that Error Injection for RX FSM Parity is enabled.Values: 0x0 (DISABLE): Rx FSM Parity Error Injection is disabled 0x1 (ENABLE): Rx FSM Parity Error Injection is enabled Value After Reset: 0x0
TPEIN	R/W	[16:16]	0x0	Tx FSM Parity Error Injection This field when set indicates that Error Injection for TX FSM Parity is enabled.Values: 0x0 (DISABLE): Tx FSM Parity Error Injection is disabled 0x1 (ENABLE): Tx FSM Parity Error Injection is enabled Value After Reset: 0x0

RESERVED	R	[15:13]	0x0	Reserved Field: Yes
PTEIN	R/W	[12:12]	0x0	PTP FSM Timeout Error Injection This field when set indicates that Error Injection for PTP FSM timeout is enabled.Values: 0x0 (DISABLE): PTP FSM Timeout Error Injection is disabled 0x1 (ENABLE): PTP FSM Timeout Error Injection is enabled Value After Reset: 0x0
ATEIN	R/W	[11:11]	0x0	APP FSM Timeout Error Injection This field when set indicates that Error Injection for APP FSM timeout is enabled.Values: 0x0 (DISABLE): APP FSM Timeout Error Injection is disabled 0x1 (ENABLE): APP FSM Timeout Error Injection is enabled Value After Reset: 0x0
CTEIN	R/W	[10:10]	0x0	CSR FSM Timeout Error Injection This field when set indicates that Error Injection for CSR timeout is enabled.Values: 0x0 (DISABLE): CSR FSM Timeout Error Injection is disabled 0x1 (ENABLE): CSR FSM Timeout Error Injection is enabled Value After Reset: 0x0
RTEIN	R/W	[9:9]	0x0	Rx FSM Timeout Error Injection

				This field when set indicates that Error Injection for RX FSM timeout is enabled.Values: 0x0 (DISABLE): Rx FSM Timeout Error Injection is disabled 0x1 (ENABLE): Rx FSM Timeout Error Injection is enabled Value After Reset: 0x0
TTEIN	R/W	[8:8]	0x0	Tx FSM Timeout Error Injection This field when set indicates that Error Injection for TX FSM timeout is enabled.Values: 0x0 (DISABLE): Tx FSM Timeout Error Injection is disabled 0x1 (ENABLE): Tx FSM Timeout Error Injection is enabled Value After Reset: 0x0
RESERVED_7_2	R	[7:2]	0x0	Reserved. Value After Reset: 0x0
PRTYEN	R/W	[1:1]	0x0	This bit when set indicates that the FSM parity feature is enabled.Values: 0x0 (DISABLE): FSM Parity feature is disabled 0x1 (ENABLE): FSM Parity feature is enabled Value After Reset: 0x0
TMOUTEN	R/W	[0:0]	0x0	This bit when set indicates that the FSM timeout feature is enabled.Values:

				0x0 (DISABLE): FSM timeout feature is disabled 0x1 (ENABLE): FSM timeout feature is enabled Value After Reset: 0x0

2.3.35 EQOS_MAC_R_MAC_FSM_ACT_TIMER

Access Type: RW

Address Offset: 0x14c

Name	Access	Bit Range	Reset value	Description
RESERVED_31_24	R	[31:24]	0x0	Reserved. Value After Reset: 0x0
LTMRMD	R/W	[23:20]	0x0	This field provides the mode value to be used for large mode FSM and other interface time outs. The timeout duration based on the mode value is given belowValues: 0x0 (DISABLE): Timer disabled 0x1 (M_1MICRO_SEC): 1us 0x2 (M_4MILLI_SEC): 1.024ms (~4ms) 0x3 (M_16MILLI_SEC): 16.384ms (~16ms) 0x4 (M_64MILLI_SEC): 65.536ms (~64ms) 0x5 (M_256MILLI_SEC): 262.144ms (~256ms) 0x6 (M_1SEC): 1.048sec (~1sec) 0x7 (M_4SEC): 4.194sec (~4sec) 0x8 (M_16SEC): 16.777sec (~16sec) 0x9 (M_32SEC): 33.554sec (~32sec) 0xa (M_64SEC): 67.108sec (~64sec)

				0xb (RSVD): Reserved Value After Reset: 0x0
NTMRMD	R/W	[19:16]	0x0	This field provides the value to be used for normal mode FSM and other interface time outs. The timeout duration based on the mode value is given belowValues: 0x0 (DISABLE): Timer disabled 0x1 (M_1MICRO_SEC): 1us 0x2 (M_4MILLI_SEC): 1.024ms (~4ms) 0x3 (M_16MILLI_SEC): 16.384ms (~16ms) 0x4 (M_64MILLI_SEC): 65.536ms (~64ms) 0x5 (M_256MILLI_SEC): 262.144ms (~256ms) 0x6 (M_1SEC): 1.048sec (~1sec) 0x7 (M_4SEC): 4.194sec (~4sec) 0x8 (M_16SEC): 16.777sec (~16sec) 0x9 (M_32SEC): 33.554sec (~32sec) 0xa (M_64SEC): 67.108sec (~64sec) 0xb (RSVD): Reserved Value After Reset: 0x0
RESERVED_15_10	R	[15:10]	0x0	Reserved. Value After Reset: 0x0
TMR	R/W	[9:0]	0x0	

				This field indicates the number of CSR clocks required to generate 1us tic. Value After Reset: 0x0

2.3.36 EQOS_MAC_R_SNPS_SCS_REG1

Access Type: RW

Address Offset: 0x150

Name	Access	Bit Range	Reset value	Description
MAC_SCS1	R/W	[31:0]	0x0	Synopsys Reserved, All the bits must be set to "0". This field is reserved for Synopsys Internal use, and must always be set to "0" unless instructed by Synopsys. Setting any bit to "1" might cause unexpected behavior in the IP. Value After Reset: 0x0

2.3.37 EQOS_MAC_R_MAC_MDIO_ADDRESS

Access Type: RW

Address Offset: 0x200

Name	Access	Bit Range	Reset value	Description
RESERVED_31_28	R	[31:28]	0x0	Reserved. Value After Reset: 0x0
PSE	R/W	[27:27]	0x0	Preamble Suppression Enable When this bit is set, the SMA suppresses the 32-bit preamble and transmits MDIO frames with only 1 preamble bit. When this bit is 0, the MDIO frame always has 32 bits of preamble as defined in the IEEE specifications.Values: 0x0 (DISABLE): Preamble Suppression disabled 0x1 (ENABLE): Preamble Suppression enabled Value After Reset: 0x0
BTB	R/W	[26:26]	0x0	Back to Back transactions

				When this bit is set and the NTC has value greater than 0, then the MAC informs the completion of a read or write command at the end of frame transfer (before the trailing clocks are transmitted). The software can thus initiate the next command which is executed immediately irrespective of the number trailing clocks generated for the previous frame. When this bit is reset, then the read/write command completion (GB is cleared) only after the trailing clocks are generated. In this mode, it is ensured that the NTC is always generated after each frame. This bit must not be set when NTC=0.Values: 0x0 (DISABLE): Back to Back transactions disabled 0x1 (ENABLE): Back to Back transactions enabled Value After Reset: 0x0
PA	R/W	[25:21]	0x0	Physical Layer Address This field indicates which Clause 22 PHY devices (out of 32 devices) the MAC is accessing. This field indicates which Clause 45 capable PHYs (out of 32 PHYs) the MAC is accessing. Value After Reset: 0x0 Testable: untestable
RDA	R/W	[20:16]	0x0	Register/Device Address These bits select the PHY register in selected Clause 22 PHY device. These bits select the Device (MMD) in selected Clause 45 capable PHY. Value After Reset: 0x0
RESERVED_15	R	[15:15]	0x0	Reserved. Value After Reset: 0x0
NTC	R/W	[14:12]	0x0	

				Number of Trailing Clocks This field controls the number of trailing clock cycles generated on gmii_mdc_o (MDC) after the end of transmission of MDIO frame. The valid values can be from 0 to 7. Programming the value to 3'h3 indicates that there are additional three clock cycles on the MDC line after the end of MDIO frame transfer. Value After Reset: 0x0
CR	R/W	[11:8]	0x0	CSR Clock Range The CSR Clock Range selection determines the frequency of the MDC clock according to the CSR clock frequency used in your design: 0000: CSR clock = 60-100 MHz; MDC clock = CSR clock/42 0001: CSR clock = 100-150 MHz; MDC clock = CSR clock/62 0010: CSR clock = 20-35 MHz; MDC clock = CSR clock/16 0011: CSR clock = 35-60 MHz; MDC clock = CSR clock/26 0100: CSR clock = 150-250 MHz; MDC clock = CSR clock/102 0101: CSR clock = 250-300 MHz; MDC clock = CSR clock/124 0110: CSR clock = 300-500 MHz; MDC clock = CSR clock/204 0111: CSR clock = 500-800 MHz; MDC clock = CSR clock/324 The suggested range of CSR clock frequency applicable for each value (when Bit 11 = 0) ensures that the MDC clock is approximately between 1.0 MHz to 2.5 MHz freqency range.

				When Bit 11 is set, you can achieve a higher frequency of the MDC clock than the frequency limit of 2.5 MHz (specified in the IEEE 802.3) and program a clock divider of lower value. For example, when CSR clock is of 100 MHz frequency and you program these bits as 1010, the resultant MDC clock is of 12.5 MHz which is above the range specified in IEEE 802.3. Program the following values only if the interfacing chips support faster MDC clocks: 1000: CSR clock/4 1001: CSR clock/6 1010: CSR clock/8 1011: CSR clock/10 1100: CSR clock/12 1101: CSR clock/14 1110: CSR clock/16 1111: CSR clock/18 These bits are not used for accessing RevMII. These bits are read-only if the RevMII interface is selected as single PHY interface. Value After Reset: 0x0
RESERVED_7_5	R	[7:5]	0x0	Reserved. Value After Reset: 0x0
SKAP	R/W	[4:4]	0x0	Skip Address Packet When this bit is set, the SMA does not send the address packets before read, write, or post-read increment address packets. This bit is valid only when C45E is set.Values: 0x0 (DISABLE): Skip Address Packet is disabled

				0x1 (ENABLE): Skip Address Packet is enabled Value After Reset: 0x0
GOC_1	R/W	[3:3]	0x0	GMII Operation Command 1 This bit is higher bit of the operation command to the PHY or RevMII, GOC_1 and GOC_O is encoded as follows: 00: Reserved 01: Write 10: Post Read Increment Address for Clause 45 PHY 11: Read When Clause 22 PHY or RevMII is enabled, only Write and Read commands are valid.Values: 0x0 (DISABLE): GMII Operation Command 1 is disabled 0x1 (ENABLE): GMII Operation Command 1 is enabled Value After Reset: 0x0 Testable: untestable
GOC_0	R/W	[2:2]	0x0	GMII Operation Command 0 This is the lower bit of the operation command to the PHY or RevMII. When in SMA mode (MDIO master) this bit along with GOC_1 determines the operation to be performed to the PHY. When only RevMII is selected in configuration this bit is read-only and tied to 1.Values: 0x0 (DISABLE): GMII Operation Command 0 is disabled

				0x1 (ENABLE): GMII Operation Command 0 is enabled Value After Reset: 0x0
C45E	R/W	[1:1]	0x0	Clause 45 PHY Enable When this bit is set, Clause 45 capable PHY is connected to MDIO. When this bit is reset, Clause 22 capable PHY is connected to MDIO.Values: 0x0 (DISABLE): Clause 45 PHY is disabled 0x1 (ENABLE): Clause 45 PHY is enabled Value After Reset: 0x0
GB	R/W	[0:0]	0x0	GMII Busy The application sets this bit to instruct the SMA to initiate a Read or Write access to the MDIO slave. The MAC clears this bit after the MDIO frame transfer is completed. Hence the software must not write or change any of the fields in MAC_MDIO_Address and MAC_MDIO_Data registers as long as this bit is set. For write transfers, the application must first write 16-bit data in the GDl field (and also RA field when C45E is set) in MAC_MDIO_Data register before setting this bit. When C45E is set, it should also write into the RA field of MAC_MDIO_Data register before initiating a read transfer. When a read transfer is completed (GB=0), the data read from the PHY register is valid in the GD field of the MAC_MDIO_Data register. Note: Even if the addressed PHY is not present, there is no change in the functionality of this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.Values:

				0x0 (DISABLE): GMII Busy is disabled 0x1 (ENABLE): GMII Busy is enabled Value After Reset: 0x0 Testable: untestable

2.3.38 EQOS_MAC_R_MAC_MDIO_DATA

Access Type: RW

Address Offset: 0x204

Name	Access	Bit Range	Reset value	Description
RA	R/W	[31:16]	0x0	Register Address This field is valid only when C45E is set. It contains the Register Address in the PHY to which the MDIO frame is intended for. Value After Reset: 0x0 Testable: untestable
GD	R/W	[15:0]	0x0	GMII Data This field contains the 16-bit data value read from the PHY or RevMII after a Management Read operation or the 16-bit data value to be written to the PHY or RevMII before a Management Write operation. Value After Reset: 0x0 Testable: untestable

2.3.39 EQOS_MAC_R_MAC_CSR_SW_CTRL

Access Type: RW

Address Offset: 0x230

Name	Access	Bit Range	Reset value	Description
RESERVED_31_9	R	[31:9]	0x0	Reserved. Value After Reset: 0x0
SEEN	R/W	[8:8]	0x0	Slave Error Response Enable When this bit is set, the MAC responds with Slave Error for accesses to reserved registers in CSR space.

				When this bit is reset, the MAC responds with Okay response to any register accessed from CSR space.Values: 0x0 (DISABLE): Slave Error Response is disabled 0x1 (ENABLE): Slave Error Response is enabled Value After Reset: 0x0
RESERVED_7_1	R	[7:1]	0x0	Reserved. Value After Reset: 0x0
RCWE	R/W	[0:0]	0x0	Register Clear on Write 1 Enable When this bit is set, the access mode of some register fields changes to Clear on Write 1, the application needs to set that respective bit to 1 to clear it. When this bit is reset, the access mode of these register fields remain as Clear on Read.Values: 0x0 (DISABLE): Register Clear on Write 1 is disabled 0x1 (ENABLE): Register Clear on Write 1 is enabled Value After Reset: 0x0

2.3.40 EQOS_MAC_R_MAC_FPE_CTRL_STS

Access Type: RW

Address Offset: 0x234

Name	Access	Bit Range	Reset value	Description
RESERVED_31_20	R	[31:20]	0x0	Reserved. Value After Reset: 0x0
TRSP	R/W	[19:19]	0x0	Transmitted Respond Frame Set when a Respond mPacket is transmitted (triggered by setting SRSP field). An interrupt can

				be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.Values: 0x0 (INACTIVE): Not transmitted Respond Frame 0x1 (ACTIVE): transmitted Respond Frame Value After Reset: 0x0
TVER	R/W	[18:18]	0x0	Transmitted Verify Frame Set when a Verify mPacket is transmitted (triggered by setting SVER field). An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.Values: 0x0 (INACTIVE): Not transmitted Verify Frame 0x1 (ACTIVE): transmitted Verify Frame Value After Reset: 0x0
RRSP	R/W	[17:17]	0x0	Received Respond Frame Set when a Respond mPacket is received. An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.Values: 0x0 (INACTIVE): Not received Respond Frame

				0x1 (ACTIVE): Received Respond Frame Value After Reset: 0x0
RVER	R/W	[16:16]	0x0	Received Verify Frame Set when a Verify mPacket is received. An interrupt can be generated for this event if FPEIE bit of MAC_Interrupt_Enable is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.Values: 0x0 (INACTIVE): Not received Verify Frame 0x1 (ACTIVE): Received Verify Frame Value After Reset: 0x0
RESERVED_15_4	R	[15:4]	0x0	Reserved. Value After Reset: 0x0
S1_SET_0	R/W	[3:3]	0x0	Synopsys Reserved, Must be set to "0". This field is reserved for Synopsys Internal use, and must always be set to "0" unless instructed by Synopsys. Setting to "1" might cause unexpected behavior in the IP. Value After Reset: 0x0
SRSP	R/W	[2:2]	0x0	Send Respond mPacket When set indicates hardware to send a Respond mPacket. Reset by hardware after sending the Respond mPacket. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.Values: 0x0 (DISABLE): Send Respond mPacket is disabled

				0x1 (ENABLE): Send Respond mPacket is enabled Value After Reset: 0x0
SVER	R/W	[1:1]	0x0	Send Verify mPacket When set indicates hardware to send a verify mPacket. Reset by hardware after sending the Verify mPacket. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.Values: 0x0 (DISABLE): Send Verify mPacket is disabled 0x1 (ENABLE): Send Verify mPacket is enabled Value After Reset: 0x0
EFPE	R/W	[0:0]	0x0	Enable Tx Frame Preemption When set Frame Preemption Tx functionality is enabled.Values: 0x0 (DISABLE): Tx Frame Preemption is disabled 0x1 (ENABLE): Tx Frame Preemption is enabled Value After Reset: 0x0

2.3.41 EQOS_MAC_R_MAC_EXT_CFG1

Access Type: RW

Address Offset: 0x238

Name	Access	Bit Range	Reset value	Description
RESERVED_31_10	R	[31:10]	0x0	Reserved. Value After Reset: 0x0
SPLM	R/W	[9:8]	0x0	Split Mode These bits indicate the mode of splitting the

				incoming Rx packets. They areValues: 0x0 (L3L4): Split at L3/L4 header 0x1 (L2OFST): Split at L2 header with an offset. Always Split at SPLOFST bytes from the beginning of Length/Type field of the Frame 0x2 (COMBN): Combination mode: Split similar to SPLM=00 for IP packets that are untagged or tagged and VLAN stripped 0x3 (RSVD): Reserved Value After Reset: 0x0
RESERVED_7	R	[7:7]	0x0	Reserved. Value After Reset: 0x0
SPLOFST	R/W	[6:0]	0x2	Split Offset These bits indicate the value of offset from the beginning of Length/Type field at which header split should take place when the appropriate SPLM is selected. The reset value of this field is 2 bytes indicating a split at L2 header. Value is in terms of bytes. Value After Reset: 0x2

2.3.42 EQOS_MAC_R_MAC_ADDRESS0_HIGH

Access Type: RW

Address Offset: 0x300

Name	Access	Bit Range	Reset value	Description
AE	R	[31:31]	0x1	Address Enable This bit is always set to 1.Values: 0x0 (DISABLE): INVALID : This bit must be always set to 1 0x1 (ENABLE): This bit is always set to 1

				Value After Reset: 0x1
RESERVED_30_Y	R	[30:18]	0x0	Reserved. Value After Reset: 0x0
DCS	R/W	[17:16]	0x0	DMA Channel Select If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address0 content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address0 content is routed. Value After Reset: 0x0
ADDRHI	R/W	[15:0]	0xffff	MAC Address0[47:32] This field contains the upper 16 bits [47:32] of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets. Value After Reset: 0xffff

2.3.43 EQOS_MAC_R_MAC_ADDRESS0_LOW

Access Type: RW

Address Offset: 0x304

Name	Access	Bit Range	Reset value	Description
ADDRLO	R/W	[31:0]	0xffffffff	MAC Address0[31:0] This field contains the lower 32 bits of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets. Value After Reset: 0xffffffff

2.3.44 EQOS_MAC_R_MAC_ADDRESS(#I)_HIGH(FORI=1;I<=7)

Access Type: RW

Address Offset: (0x0008*i)+0x0300

Name	Access	Bit Range	Reset value	Description
AE	R/W	[31:31]	0x0	Address Enable When this bit is set, the address filter module uses the second MAC address for perfect filtering. When this bit is reset, the address filter module ignores the address for filtering.Values: 0x0 (DISABLE): Address is ignored 0x1 (ENABLE): Address is enabled Value After Reset: 0x0
SA	R/W	[30:30]	0x0	Source Address When this bit is set, the MAC Address1[47:0] is used to compare with the SA fields of the received packet. When this bit is reset, the MAC Address1[47:0] is used to compare with the DA fields of the received packet.Values: 0x0 (DA): Compare with Destination Address 0x1 (SA): Compare with Source Address Value After Reset: 0x0
MBC	R/W	[29:24]	0x0	Mask Byte Control These bits are mask control bits for comparing each of the MAC Address bytes. When set high, the MAC does not compare the corresponding byte of received DA or SA with the contents of MAC Address1 registers. Each bit controls the masking of the bytes as follows: Bit 29: MAC_Address${i}_High[15:8] Bit 28: MAC_Address${i}_High[7:0]

				Bit 27: MAC_Address${i}_Low[31:24] .. Bit 24: MAC_Address${i}_Low[7:0] You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address. Value After Reset: 0x0
RESERVED_23_Y	R	[23:18]	0x0	Reserved. Value After Reset: 0x0
DCS	R/W	[17:16]	0x0	DMA Channel Select If the PDC bit of MAC_Ext_Configuration register is not set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address(#i) content is routed. If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address(#i) content is routed. Value After Reset: 0x0
ADDRHI	R/W	[15:0]	0xffff	MAC Address1 [47:32] This field contains the upper 16 bits[47:32] of the second 6-byte MAC address. Value After Reset: 0xffff

2.3.45 EQOS_MAC_R_MAC_ADDRESS(#I)_LOW(FORI=1;I<=7)

Access Type: RW

Address Offset: (0x0008*i)+0x0304

Name	Access	Bit Range	Reset value	Description
ADDRLO	R/W	[31:0]	0xffffffff	MAC Address1 [31:0] This field contains the lower 32 bits of second 6-byte MAC address. The content of this field is undefined

				until loaded by the application after the initialization process. Value After Reset: 0xffffffff

2.3.46 EQOS_MAC_R_MMC_CONTROL

Access Type: RW

Address Offset: 0x700

Name	Access	Bit Range	Reset value	Description
RESERVED_31_9	R	[31:9]	0x0	Reserved. Value After Reset: 0x0
UCDBC	R/W	[8:8]	0x0	Update MMC Counters for Dropped Broadcast Packets Note: The CNTRST bit has a higher priority than the CNTPRST bit. Therefore, when the software tries to set both bits in the same write cycle, all counters are cleared and the CNTPRST bit is not set. When set, the MAC updates all related MMC Counters for Broadcast packets that are dropped because of the setting of the DBF bit of MAC_Packet_Filter register. When reset, the MMC Counters are not updated for dropped Broadcast packets.Values: 0x0 (DISABLE): Update MMC Counters for Dropped Broadcast Packets is disabled 0x1 (ENABLE): Update MMC Counters for Dropped Broadcast Packets is enabled Value After Reset: 0x0
RESERVED_7_6	R	[7:6]	0x0	Reserved. Value After Reset: 0x0
CNTPRSTLVL	R/W	[5:5]	0x0	Full-Half Preset When this bit is low and the CNTPRST bit is set, all MMC counters get preset to almost-half value. All octet counters get preset to 0x7FFF_F800 (Half

				2KBytes) and all packet-counters gets preset to 0x7FFF_FFF0 (Half 16). When this bit is high and the CNTPRST bit is set, all MMC counters get preset to almost-full value. All octet counters get preset to 0xFFFF_F800 (Full 2KBytes) and all packet-counters gets preset to 0xFFFF_FFF0 (Full 16). For 16-bit counters, the almost-half preset values are 0x7800 and 0x7FF0 for the respective octet and packet counters. Similarly, the almost-full preset values for the 16-bit counters are 0xF800 and 0xFFF0.Values: 0x0 (DISABLE): Full-Half Preset is disabled 0x1 (ENABLE): Full-Half Preset is enabled Value After Reset: 0x0
CNTPRST	R/W	[4:4]	0x0	Counters Preset When this bit is set, all counters are initialized or preset to almost full or almost half according to the CNTPRSTLVL bit. This bit is cleared automatically after 1 clock cycle. This bit, along with the CNTPRSTLVL bit, is useful for debugging and testing the assertion of interrupts because of MMC counter becoming half-full or full. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets.Values: 0x0 (DISABLE): Counters Preset is disabled 0x1 (ENABLE): Counters Preset is enabled Value After Reset: 0x0 Testable: untestable
CNTFREEZ	R/W	[3:3]	0x0	MMC Counter Freeze When this bit is set, it freezes all MMC counters to their current value. Until this bit is reset to 0, no MMC counter is

				updated because of any transmitted or received packet. If any MMC counter is read with the Reset on Read bit set, then that counter is also cleared in this mode.Values: 0x0 (DISABLE): MMC Counter Freeze is disabled 0x1 (ENABLE): MMC Counter Freeze is enabled Value After Reset: 0x0
RSTONRD	R/W	[2:2]	0x0	Reset on Read When this bit is set, the MMC counters are reset to zero after Read (self-clearing after reset). The counters are cleared when the least significant byte lane (Bits[7:0]) is read.Values: 0x0 (DISABLE): Reset on Read is disabled 0x1 (ENABLE): Reset on Read is enabled Value After Reset: 0x0
CNTSTOPRO	R/W	[1:1]	0x0	Counter Stop Rollover When this bit is set, the counter does not roll over to zero after reaching the maximum value.Values: 0x0 (DISABLE): Counter Stop Rollover is disabled 0x1 (ENABLE): Counter Stop Rollover is enabled Value After Reset: 0x0
CNTRST	R/W	[0:0]	0x0	Counters Reset When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets.Values: 0x0 (DISABLE): Counters are not reset

				0x1 (ENABLE): All counters are reset Value After Reset: 0x0 Testable: untestable

2.3.47 EQOS_MAC_R_MMC_RX_INTERRUPT

Access Type: RW

Address Offset: 0x704

Name	Access	Bit Range	Reset value	Description
RESERVED_31_28	R	[31:28]	0x0	Reserved. Value After Reset: 0x0
RXLPITRCIS	R	[27:27]	0x0	MMC Receive LPI transition counter interrupt status This bit is set when the Rx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Receive LPI transition Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive LPI transition Counter Interrupt Status detected Value After Reset: 0x0
RESERVED	R	[26:26]	0x0	Reserved Field: Yes
RXCTRLPIS	R	[25:25]	0x0	MMC Receive Control Packet Counter Interrupt Status This bit is set when the rxctrlpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values:

				0x0 (INACTIVE): MMC Receive Control Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive Control Packet Counter Interrupt Status detected Value After Reset: 0x0
RXRCVERRPIS	R	[24:24]	0x0	MMC Receive Error Packet Counter Interrupt Status This bit is set when the rxrcverror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Receive Error Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive Error Packet Counter Interrupt Status detected Value After Reset: 0x0
RESERVED	R	[23:23]	0x0	Reserved Field: Yes
RXVLANGBPIS	R	[22:22]	0x0	MMC Receive VLAN Good Bad Packet Counter Interrupt Status This bit is set when the rxvlanpackets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Receive VLAN Good Bad Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive VLAN Good Bad Packet Counter Interrupt Status

				detected Value After Reset: 0x0
RXFOVPIS	R	[21:21]	0x0	MMC Receive FIFO Overflow Packet Counter Interrupt Status This bit is set when the rxfifooverflow counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Receive FIFO Overflow Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive FIFO Overflow Packet Counter Interrupt Status detected Value After Reset: 0x0
RXPAUSPIS	R	[20:20]	0x0	MMC Receive Pause Packet Counter Interrupt Status This bit is set when the rxpausepackets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Receive Pause Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive Pause Packet Counter Interrupt Status detected Value After Reset: 0x0
RESERVED	R	[19:18]	0x0	Reserved Field: Yes

RXUCGPIS	R	[17:17]	0x0	MMC Receive Unicast Good Packet Counter Interrupt Status This bit is set when the rxunicastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Receive Unicast Good Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive Unicast Good Packet Counter Interrupt Status detected Value After Reset: 0x0
RX1024TMAXOCTGBPIS	R	[16:16]	0x0	MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status This bit is set when the rx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Status detected Value After Reset: 0x0
RX512T1023OCTGBPIS	R	[15:15]	0x0	MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Status This bit is set when the

				rx512to1023octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Status detected Value After Reset: 0x0
RX256T511OCTGBPIS	R	[14:14]	0x0	MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Status This bit is set when the rx256to511octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Status detected Value After Reset: 0x0
RX128T255OCTGBPIS	R	[13:13]	0x0	MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Status This bit is set when the rx128to255octets_gb counter reaches half of the maximum value or the maximum value.

				Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Status detected Value After Reset: 0x0
RX65T127OCTGBPIS	R	[12:12]	0x0	MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Status This bit is set when the rx65to127octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Status detected Value After Reset: 0x0
RX64OCTGBPIS	R	[11:11]	0x0	MMC Receive 64 Octet Good Bad Packet Counter Interrupt Status This bit is set when the rx64octets_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Status

				not detected 0x1 (ACTIVE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Status detected Value After Reset: 0x0
RXOSIZEGPIS	R	[10:10]	0x0	MMC Receive Oversize Good Packet Counter Interrupt Status This bit is set when the rxoversize_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Receive Oversize Good Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive Oversize Good Packet Counter Interrupt Status detected Value After Reset: 0x0
RXUSIZEGPIS	R	[9:9]	0x0	MMC Receive Undersize Good Packet Counter Interrupt Status This bit is set when the rxundersize_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Receive Undersize Good Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive Undersize Good Packet Counter Interrupt Status detected

				Value After Reset: 0x0
RXJABERPIS	R	[8:8]	0x0	MMC Receive Jabber Error Packet Counter Interrupt Status This bit is set when the rxjabbererror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Receive Jabber Error Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive Jabber Error Packet Counter Interrupt Status detected Value After Reset: 0x0
RXRUNTPIS	R	[7:7]	0x0	MMC Receive Runt Packet Counter Interrupt Status This bit is set when the rxrunterror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Receive Runt Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive Runt Packet Counter Interrupt Status detected Value After Reset: 0x0
RXALGNERPIS	R	[6:6]	0x0	MMC Receive Alignment Error Packet Counter Interrupt Status

				This bit is set when the rxalignmenterror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Receive Alignment Error Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive Alignment Error Packet Counter Interrupt Status detected Value After Reset: 0x0
RXCRCERPIS	R	[5:5]	0x0	MMC Receive CRC Error Packet Counter Interrupt Status This bit is set when the rxcrcerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Receive CRC Error Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive CRC Error Packet Counter Interrupt Status detected Value After Reset: 0x0
RXMCGPIS	R	[4:4]	0x0	MMC Receive Multicast Good Packet Counter Interrupt Status This bit is set when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values:

				0x0 (INACTIVE): MMC Receive Multicast Good Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive Multicast Good Packet Counter Interrupt Status detected Value After Reset: 0x0
RXBCGPIS	R	[3:3]	0x0	MMC Receive Broadcast Good Packet Counter Interrupt Status This bit is set when the rxbroadcastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Receive Broadcast Good Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive Broadcast Good Packet Counter Interrupt Status detected Value After Reset: 0x0
RXGOCTIS	R	[2:2]	0x0	MMC Receive Good Octet Counter Interrupt Status This bit is set when the rxoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Receive Good Octet Counter Interrupt Status not detected

				0x1 (ACTIVE): MMC Receive Good Octet Counter Interrupt Status detected Value After Reset: 0x0
RXGBOCTIS	R	[1:1]	0x0	MMC Receive Good Bad Octet Counter Interrupt Status This bit is set when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Receive Good Bad Octet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive Good Bad Octet Counter Interrupt Status detected Value After Reset: 0x0
RXGBPKTIS	R	[0:0]	0x0	MMC Receive Good Bad Packet Counter Interrupt Status This bit is set when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Receive Good Bad Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive Good Bad Packet Counter Interrupt Status detected Value After Reset: 0x0

2.3.48 EQOS_MAC_R_MMC_TX_INTERRUPT

Access Type: RW

Address Offset: 0x708

Name	Access	Bit Range	Reset value	Description
RESERVED_31_28	R	[31:28]	0x0	Reserved. Value After Reset: 0x0
TXLPITRCIS	R	[27:27]	0x0	MMC Transmit LPI transition counter interrupt status This bit is set when the Tx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Transmit LPI transition Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Transmit LPI transition Counter Interrupt Status detected Value After Reset: 0x0
RESERVED	R	[26:26]	0x0	Reserved Field: Yes
TXOSIZEGPIS	R	[25:25]	0x0	MMC Transmit Oversize Good Packet Counter Interrupt Status This bit is set when the txoversize_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Transmit Oversize Good Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Transmit Oversize Good Packet Counter Interrupt Status detected Value After Reset: 0x0

TXVLANGPIS	R	[24:24]	0x0	MMC Transmit VLAN Good Packet Counter Interrupt Status This bit is set when the txvlanpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Transmit VLAN Good Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Transmit VLAN Good Packet Counter Interrupt Status detected Value After Reset: 0x0
TXPAUSPIS	R	[23:23]	0x0	MMC Transmit Pause Packet Counter Interrupt Status This bit is set when the txpausepacketserror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Transmit Pause Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Transmit Pause Packet Counter Interrupt Status detected Value After Reset: 0x0
RESERVED	R	[22:22]	0x0	Reserved Field: Yes
TXGPKTIS	R	[21:21]	0x0	MMC Transmit Good Packet Counter Interrupt Status This bit is set when the txpacketcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values:

				0x0 (INACTIVE): MMC Transmit Good Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Transmit Good Packet Counter Interrupt Status detected Value After Reset: 0x0
TXGOCTIS	R	[20:20]	0x0	MMC Transmit Good Octet Counter Interrupt Status This bit is set when the txoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Transmit Good Octet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Transmit Good Octet Counter Interrupt Status detected Value After Reset: 0x0
RESERVED	R	[19:14]	0x0	Reserved Field: Yes
TXUFLOWERPIS	R	[13:13]	0x0	MMC Transmit Underflow Error Packet Counter Interrupt Status This bit is set when the txunderflowerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Transmit Underflow Error Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Transmit Underflow Error Packet Counter Interrupt Status detected

				Value After Reset: 0x0
RESERVED	R	[12:4]	0x0	Reserved Field: Yes
TXMCGPIS	R	[3:3]	0x0	MMC Transmit Multicast Good Packet Counter Interrupt Status This bit is set when the txmulticastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Transmit Multicast Good Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Transmit Multicast Good Packet Counter Interrupt Status detected Value After Reset: 0x0
TXBCGPIS	R	[2:2]	0x0	MMC Transmit Broadcast Good Packet Counter Interrupt Status This bit is set when the txbroadcastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Transmit Broadcast Good Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Transmit Broadcast Good Packet Counter Interrupt Status detected Value After Reset: 0x0
TXGBPKTIS	R	[1:1]	0x0	MMC Transmit Good Bad Packet Counter Interrupt Status This bit is set when the txpacketcount_gb counter

				reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Transmit Good Bad Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Transmit Good Bad Packet Counter Interrupt Status detected Value After Reset: 0x0
TXGBOCTIS	R	[0:0]	0x0	MMC Transmit Good Bad Octet Counter Interrupt Status This bit is set when the txoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): MMC Transmit Good Bad Octet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Transmit Good Bad Octet Counter Interrupt Status detected Value After Reset: 0x0

2.3.49 EQOS_MAC_R_MMC_RX_INTERRUPT_MASK

Access Type: RW

Address Offset: 0x70c

Name	Access	Bit Range	Reset value	Description
RESERVED_31_28	R	[31:28]	0x0	Reserved. Value After Reset: 0x0
RXLPITRCIM	R/W	[27:27]	0x0	MMC Receive LPI transition counter interrupt Mask Setting this bit masks the interrupt when

				the Rx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive LPI transition counter interrupt Mask is disabled 0x1 (ENABLE): MMC Receive LPI transition counter interrupt Mask is enabled Value After Reset: 0x0
RESERVED	R	[26:26]	0x0	Reserved Field: Yes
RXCTRLPIM	R/W	[25:25]	0x0	MMC Receive Control Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxctrlpackets_g counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive Control Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive Control Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
RXRCVERRPIM	R/W	[24:24]	0x0	MMC Receive Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxrcverror counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive Error Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive Error

				Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
RESERVED	R	[23:23]	0x0	Reserved Field: Yes
RXVLANGBPIM	R/W	[22:22]	0x0	MMC Receive VLAN Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxvlanpackets_gb counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive VLAN Good Bad Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive VLAN Good Bad Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
RXFOVPIM	R/W	[21:21]	0x0	MMC Receive FIFO Overflow Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxfifooverflow counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive FIFO Overflow Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive FIFO Overflow Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
RXPAUSPIM	R/W	[20:20]	0x0	

				MMC Receive Pause Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxpausepackets counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive Pause Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive Pause Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
RESERVED	R	[19:18]	0x0	Reserved Field: Yes
RXUCGPIM	R/W	[17:17]	0x0	MMC Receive Unicast Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxunicastpackets_g counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive Unicast Good Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive Unicast Good Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
RX1024TMAXOCTGBPIM	R/W	[16:16]	0x0	MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask. Setting this bit masks the interrupt when the rx1024tomaxoctets_gb counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive 1024 to

				Maximum Octet Good Bad Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive 1024 to Maximum Octet Good Bad Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
RX512T1023OCTGBPIM	R/W	[15:15]	0x0	MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rx512to1023octets_gb counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive 512 to 1023 Octet Good Bad Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
RX256T511OCTGBPIM	R/W	[14:14]	0x0	MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rx256to511octets_gb counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive 256 to 511 Octet Good Bad Packet Counter Interrupt Mask is enabled

				Value After Reset: 0x0
RX128T255OCTGBPIM	R/W	[13:13]	0x0	MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rx128to255octets_gb counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive 128 to 255 Octet Good Bad Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
RX65T127OCTGBPIM	R/W	[12:12]	0x0	MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rx65to127octets_gb counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive 65 to 127 Octet Good Bad Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
RX64OCTGBPIM	R/W	[11:11]	0x0	MMC Receive 64 Octet Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rx64octets_gb counter reaches half of

				the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive 64 Octet Good Bad Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
RXOSIZEGPIM	R/W	[10:10]	0x0	MMC Receive Oversize Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxoversize_g counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive Oversize Good Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive Oversize Good Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
RXUSIZEGPIM	R/W	[9:9]	0x0	MMC Receive Undersize Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxundersize_g counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive Undersize Good Packet Counter Interrupt Mask is disabled

				0x1 (ENABLE): MMC Receive Undersize Good Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
RXJABERPIM	R/W	[8:8]	0x0	MMC Receive Jabber Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxjabbererror counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive Jabber Error Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive Jabber Error Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
RXRUNTPIM	R/W	[7:7]	0x0	MMC Receive Runt Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxrunterror counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive Runt Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive Runt Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
RXALGNERPIM	R/W	[6:6]	0x0	MMC Receive Alignment Error Packet Counter Interrupt Mask

				Setting this bit masks the interrupt when the rxalignmenterror counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive Alignment Error Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive Alignment Error Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
RXCRCERPIM	R/W	[5:5]	0x0	MMC Receive CRC Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxcrcerror counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive CRC Error Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive CRC Error Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
RXMCGPIM	R/W	[4:4]	0x0	MMC Receive Multicast Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive Multicast Good Packet Counter Interrupt Mask is

				disabled 0x1 (ENABLE): MMC Receive Multicast Good Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
RXBCGPIM	R/W	[3:3]	0x0	MMC Receive Broadcast Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxbroadcastpackets_g counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive Broadcast Good Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive Broadcast Good Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
RXGOCTIM	R/W	[2:2]	0x0	MMC Receive Good Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxoctetcount_g counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive Good Octet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive Good Octet Counter Interrupt Mask is enabled Value After Reset: 0x0
RXGBOCTIM	R/W	[1:1]	0x0	

				MMC Receive Good Bad Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive Good Bad Octet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive Good Bad Octet Counter Interrupt Mask is enabled Value After Reset: 0x0
RXGBPKTIM	R/W	[0:0]	0x0	MMC Receive Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Receive Good Bad Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive Good Bad Packet Counter Interrupt Mask is enabled Value After Reset: 0x0

2.3.50 EQOS_MAC_R_MMC_TX_INTERRUPT_MASK

Access Type: RW

Address Offset: 0x710

Name	Access	Bit Range	Reset value	Description
RESERVED_31_28	R	[31:28]	0x0	Reserved. Value After Reset: 0x0
TXLPITRCIM	R/W	[27:27]	0x0	

				MMC Transmit LPI transition counter interrupt Mask Setting this bit masks the interrupt when the Tx_LPI_Tran_Cntr counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Transmit LPI transition counter interrupt Mask is disabled 0x1 (ENABLE): MMC Transmit LPI transition counter interrupt Mask is enabled Value After Reset: 0x0
RESERVED	R	[26:26]	0x0	Reserved Field: Yes
TXOSIZEGPIM	R/W	[25:25]	0x0	MMC Transmit Oversize Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txoversize_g counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Transmit Oversize Good Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Transmit Oversize Good Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
TXVLANGPIM	R/W	[24:24]	0x0	MMC Transmit VLAN Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txvlanpackets_g counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Transmit VLAN Good Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Transmit VLAN Good Packet Counter Interrupt Mask is enabled

				Value After Reset: 0x0
TXPAUSPIM	R/W	[23:23]	0x0	MMC Transmit Pause Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txpausepackets counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Transmit Pause Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Transmit Pause Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
RESERVED	R	[22:22]	0x0	Reserved Field: Yes
TXGPKTIM	R/W	[21:21]	0x0	MMC Transmit Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txpacketcount_g counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Transmit Good Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Transmit Good Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
TXGOCTIM	R/W	[20:20]	0x0	MMC Transmit Good Octet Counter Interrupt Mask Setting this bit masks the interrupt when the txoctetcount_g counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Transmit Good Octet Counter Interrupt Mask is disabled

				0x1 (ENABLE): MMC Transmit Good Octet Counter Interrupt Mask is enabled Value After Reset: 0x0
RESERVED	R	[19:14]	0x0	Reserved Field: Yes
TXUFLOWERPIM	R/W	[13:13]	0x0	MMC Transmit Underflow Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txunderflowerror counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Transmit Underflow Error Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Transmit Underflow Error Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
RESERVED	R	[12:4]	0x0	Reserved Field: Yes
TXMCGPIM	R/W	[3:3]	0x0	MMC Transmit Multicast Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txmulticastpackets_g counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Transmit Multicast Good Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Transmit Multicast Good Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
TXBCGPIM	R/W	[2:2]	0x0	MMC Transmit Broadcast Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the

				txbroadcastpackets_g counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Transmit Broadcast Good Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Transmit Broadcast Good Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
TXGBPKTIM	R/W	[1:1]	0x0	MMC Transmit Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txpacketcount_gb counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Transmit Good Bad Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Transmit Good Bad Packet Counter Interrupt Mask is enabled Value After Reset: 0x0
TXGBOCTIM	R/W	[0:0]	0x0	MMC Transmit Good Bad Octet Counter Interrupt Mask Setting this bit masks the interrupt when the txoctetcount_gb counter reaches half of the maximum value or the maximum value.Values: 0x0 (DISABLE): MMC Transmit Good Bad Octet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Transmit Good Bad Octet Counter Interrupt Mask is enabled Value After Reset: 0x0

2.3.51 EQOS_MAC_R_TX_OCTET_COUNT_GOOD_BAD

Access Type: RW

Address Offset: 0x714

Name	Access	Bit Range	Reset value	Description
TXOCTGB	R	[31:0]	0x0	Tx Octet Count Good Bad This field indicates the number of bytes transmitted, exclusive of preamble and retried bytes, in good and bad packets. Value After Reset: 0x0

2.3.52 EQOS_MAC_R_TX_PACKET_COUNT_GOOD_BAD

Access Type: RW

Address Offset: 0x718

Name	Access	Bit Range	Reset value	Description
TXPKTGB	R	[31:0]	0x0	Tx Packet Count Good Bad This field indicates the number of good and bad packets transmitted, exclusive of retried packets. Value After Reset: 0x0

2.3.53 EQOS_MAC_R_TX_BROADCAST_PACKETS_GOOD

Access Type: RW

Address Offset: 0x71c

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
TXBCASTG	R	[15:0]	0x0	Tx Broadcast Packets Good This field indicates the number of good broadcast packets transmitted. Value After Reset: 0x0

2.3.54 EQOS_MAC_R_TX_MULTICAST_PACKETS_GOOD

Access Type: RW

Address Offset: 0x720

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0

TXMCASTG	R	[15:0]	0x0	Tx Multicast Packets Good This field indicates the number of good multicast packets transmitted. Value After Reset: 0x0

2.3.55 EQOS_MAC_R_TX_UNDERFLOW_ERROR_PACKETS

Access Type: RW

Address Offset: 0x748

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
TXUNDRFLW	R	[15:0]	0x0	Tx Underflow Error Packets This field indicates the number of packets aborted because of packets underflow error. Value After Reset: 0x0

2.3.56 EQOS_MAC_R_TX_OCTET_COUNT_GOOD

Access Type: RW

Address Offset: 0x764

Name	Access	Bit Range	Reset value	Description
TXOCTG	R	[31:0]	0x0	Tx Octet Count Good This field indicates the number of bytes transmitted, exclusive of preamble, only in good packets. Value After Reset: 0x0

2.3.57 EQOS_MAC_R_TX_PACKET_COUNT_GOOD

Access Type: RW

Address Offset: 0x768

Name	Access	Bit Range	Reset value	Description
TXPKTG	R	[31:0]	0x0	Tx Packet Count Good This field indicates the number of good packets transmitted. Value After Reset: 0x0

2.3.58 EQOS_MAC_R_TX_PAUSE_PACKETS

Access Type: RW

Address Offset: 0x770

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
TXPAUSE	R	[15:0]	0x0	Tx Pause Packets This field indicates the number of good Pause packets transmitted. Value After Reset: 0x0

2.3.59 EQOS_MAC_R_TX_VLAN_PACKETS_GOOD

Access Type: RW

Address Offset: 0x774

Name	Access	Bit Range	Reset value	Description
TXVLANG	R	[31:0]	0x0	Tx VLAN Packets Good This field provides the number of good VLAN packets transmitted. Value After Reset: 0x0

2.3.60 EQOS_MAC_R_TX_OSIZE_PACKETS_GOOD

Access Type: RW

Address Offset: 0x778

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
TXOSIZG	R	[15:0]	0x0	Tx OSize Packets Good This field indicates the number of packets transmitted without errors and with length greater than the maxsize (1,518 or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in S2KP bit of the MAC_Configuration register). Value After Reset: 0x0

2.3.61 EQOS_MAC_R_RX_PACKETS_COUNT_GOOD_BAD

Access Type: RW

Address Offset: 0x780

Name	Access	Bit Range	Reset value	Description

RXPKTGB	R	[31:0]	0x0	Rx Packets Count Good Bad This field indicates the number of good and bad packets received. Value After Reset: 0x0

2.3.62 EQOS_MAC_R_RX_OCTET_COUNT_GOOD_BAD

Access Type: RW

Address Offset: 0x784

Name	Access	Bit Range	Reset value	Description
RXOCTGB	R	[31:0]	0x0	Rx Octet Count Good Bad This field indicates the number of bytes received, exclusive of preamble, in good and bad packets. Value After Reset: 0x0

2.3.63 EQOS_MAC_R_RX_OCTET_COUNT_GOOD

Access Type: RW

Address Offset: 0x788

Name	Access	Bit Range	Reset value	Description
RXOCTG	R	[31:0]	0x0	Rx Octet Count Good This field indicates the number of bytes received, exclusive of preamble, only in good packets. Value After Reset: 0x0

2.3.64 EQOS_MAC_R_RX_BROADCAST_PACKETS_GOOD

Access Type: RW

Address Offset: 0x78c

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
RXBCASTG	R	[15:0]	0x0	Rx Broadcast Packets Good This field indicates the number of good broadcast packets received. Value After Reset: 0x0

2.3.65 EQOS_MAC_R_RX_MULTICAST_PACKETS_GOOD

Access Type: RW

Address Offset: 0x790

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
RXMCASTG	R	[15:0]	0x0	Rx Multicast Packets Good This field indicates the number of good multicast packets received. Value After Reset: 0x0

2.3.66 EQOS_MAC_R_RX_CRC_ERROR_PACKETS

Access Type: RW

Address Offset: 0x794

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
RXCRCERR	R	[15:0]	0x0	Rx CRC Error Packets This field indicates the number of packets received with CRC error. Value After Reset: 0x0

2.3.67 EQOS_MAC_R_RX_ALIGNMENT_ERROR_PACKETS

Access Type: RW

Address Offset: 0x798

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
RXALGNERR	R	[15:0]	0x0	Rx Alignment Error Packets This field indicates the number of packets received with alignment (dribble) error. It is valid only in 10/100 mode. Value After Reset: 0x0

2.3.68 EQOS_MAC_R_RX_RUNT_ERROR_PACKETS

Access Type: RW

Address Offset: 0x79c

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
RXRUNTERR	R	[15:0]	0x0	Rx Runt Error Packets This field indicates the number of packets received with runt (length less than 64 bytes and CRC error) error. Value After Reset: 0x0

2.3.69 EQOS_MAC_R_RX_JABBER_ERROR_PACKETS

Access Type: RW

Address Offset: 0x7a0

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
RXJABERR	R	[15:0]	0x0	Rx Jabber Error Packets This field indicates the number of giant packets received with length (including CRC) greater than 1,518 bytes (1,522 bytes for VLAN tagged) and with CRC error. If Jumbo Packet mode is enabled, packets of length greater than 9,018 bytes (9,022 bytes for VLAN tagged) are considered as giant packets. Value After Reset: 0x0

2.3.70 EQOS_MAC_R_RX_UNDERSIZE_PACKETS_GOOD

Access Type: RW

Address Offset: 0x7a4

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
RXUNDERSZG	R	[15:0]	0x0	Rx Undersize Packets Good This field indicates the number of packets received with length less than 64 bytes, without

				any errors. Value After Reset: 0x0

2.3.71 EQOS_MAC_R_RX_OVERSIZE_PACKETS_GOOD

Access Type: RW

Address Offset: 0x7a8

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
RXOVERSZG	R	[15:0]	0x0	Rx Oversize Packets Good This field indicates the number of packets received without errors, with length greater than the maxsize (1,518 bytes or 1,522 bytes for VLAN tagged packets; 2000 bytes if enabled in the S2KP bit of the MAC_Configuration register). Value After Reset: 0x0

2.3.72 EQOS_MAC_R_RX_64OCTETS_PACKETS_GOOD_BAD

Access Type: RW

Address Offset: 0x7ac

Name	Access	Bit Range	Reset value	Description
RX64OCTGB	R	[31:0]	0x0	Rx 64 Octets Packets Good Bad This field indicates the number of good and bad packets received with length 64 bytes, exclusive of the preamble. Value After Reset: 0x0

2.3.73 EQOS_MAC_R_RX_65TO127OCTETS_PACKETS_GOOD_BAD

Access Type: RW

Address Offset: 0x7b0

Name	Access	Bit Range	Reset value	Description
RX65_127OCTGB	R	[31:0]	0x0	Rx 65-127 Octets Packets Good BadThis field indicates the number of good and bad packets received with length between 65 and 127 (inclusive) bytes, exclusive of the preamble. Value After Reset: 0x0

2.3.74 EQOS_MAC_R_RX_128TO255OCTETS_PACKETS_GOOD_BAD

Access Type: RW

Address Offset: 0x7b4

Name	Access	Bit Range	Reset value	Description
RX128_255OCTGB	R	[31:0]	0x0	Rx 128-255 Octets Packets Good Bad This field indicates the number of good and bad packets received with length between 128 and 255 (inclusive) bytes, exclusive of the preamble. Value After Reset: 0x0

2.3.75 EQOS_MAC_R_RX_256TO511OCTETS_PACKETS_GOOD_BAD

Access Type: RW

Address Offset: 0x7b8

Name	Access	Bit Range	Reset value	Description
RX256_511OCTGB	R	[31:0]	0x0	Rx 256-511 Octets Packets Good Bad This field indicates the number of good and bad packets received with length between 256 and 511 (inclusive) bytes, exclusive of the preamble. Value After Reset: 0x0

2.3.76 EQOS_MAC_R_RX_512TO1023OCTETS_PACKETS_GOOD_BAD

Access Type: RW

Address Offset: 0x7bc

Name	Access	Bit Range	Reset value	Description
RX512_1023OCTGB	R	[31:0]	0x0	RX 512-1023 Octets Packets Good Bad This field indicates the number of good and bad packets received with length between 512 and 1023 (inclusive) bytes, exclusive of the preamble. Value After Reset: 0x0

2.3.77 EQOS_MAC_R_RX_1024TOMAXOCTETS_PACKETS_GOOD_BAD

Access Type: RW

Address Offset: 0x7c0

Name	Access	Bit Range	Reset value	Description
RX1024_MAXOCTGB	R	[31:0]	0x0	Rx 1024-Max Octets Good Bad

				This field indicates the number of good and bad packets received with length between 1024 and maxsize (inclusive) bytes, exclusive of the preamble. Value After Reset: 0x0

2.3.78 EQOS_MAC_R_RX_UNICAST_PACKETS_GOOD

Access Type: RW

Address Offset: 0x7c4

Name	Access	Bit Range	Reset value	Description
RXUCASTG	R	[31:0]	0x0	Rx Unicast Packets Good This field indicates the number of good unicast packets received. Value After Reset: 0x0

2.3.79 EQOS_MAC_R_RX_PAUSE_PACKETS

Access Type: RW

Address Offset: 0x7d0

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
RXPAUSEPKT	R	[15:0]	0x0	Rx Pause Packets This field indicates the number of good and valid Pause packets received. Value After Reset: 0x0

2.3.80 EQOS_MAC_R_RX_FIFO_OVERFLOW_PACKETS

Access Type: RW

Address Offset: 0x7d4

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
RXFIFOOVFL	R	[15:0]	0x0	Rx FIFO Overflow Packets This field indicates the number of missed received packets because of FIFO overflow. Value After Reset: 0x0

2.3.81 EQOS_MAC_R_RX_VLAN_PACKETS_GOOD_BAD

Access Type: RW

Address Offset: 0x7d8

Name	Access	Bit Range	Reset value	Description
RXVLANPKTGB	R	[31:0]	0x0	Rx VLAN Packets Good Bad This field indicates the number of good and bad VLAN packets received. Value After Reset: 0x0

2.3.82 EQOS_MAC_R_RX_RECEIVE_ERROR_PACKETS

Access Type: RW

Address Offset: 0x7e0

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
RXRCVERR	R	[15:0]	0x0	Rx Receive Error Packets This field indicates the number of packets received with Receive error or Packet Extension error on the GMII or MII interface. Value After Reset: 0x0

2.3.83 EQOS_MAC_R_RX_CONTROL_PACKETS_GOOD

Access Type: RW

Address Offset: 0x7e4

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
RXCTRLG	R	[15:0]	0x0	Rx Control Packets Good This field indicates the number of good control packets received. Value After Reset: 0x0

2.3.84 EQOS_MAC_R_TX_LPI_TRAN_CNTR

Access Type: RW

Address Offset: 0x7f0

Name	Access	Bit	Reset	Description

		Range	value	
RESERVED	R	[31:16]	0x0	Reserved Field: Yes
TXLPITRC	R	[15:0]	0x0	Tx LPI Transition counter This field indicates the number of times Tx LPI Entry has occurred. Even if Tx LPI Entry occurs in Automate Mode (because of LPITXA bit set in the LPI Control and Status register), the counter increments. Value After Reset: 0x0

2.3.85 EQOS_MAC_R_RX_LPI_TRAN_CNTR

Access Type: RW

Address Offset: 0x7f8

Name	Access	Bit Range	Reset value	Description
RESERVED	R	[31:16]	0x0	Reserved Field: Yes
RXLPITRC	R	[15:0]	0x0	Rx LPI Transition counter This field indicates the number of times Rx LPI Entry has occurred. Value After Reset: 0x0

2.3.86 EQOS_MAC_R_MMC_FPE_TX_INTERRUPT

Access Type: RW

Address Offset: 0x8a0

Name	Access	Bit Range	Reset value	Description
RESERVED_31_2	R	[31:2]	0x0	Reserved. Value After Reset: 0x0
HRCIS	R	[1:1]	0x0	MMC Tx Hold Request Counter Interrupt Status This bit is set when the Tx_Hold_Req_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration.Values: 0x0 (INACTIVE): MMC Tx Hold Request Counter Interrupt Status not detected

				0x1 (ACTIVE): MMC Tx Hold Request Counter Interrupt Status detected Value After Reset: 0x0
FCIS	R	[0:0]	0x0	MMC Tx FPE Fragment Counter Interrupt status This bit is set when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.Values: 0x0 (INACTIVE): MMC Tx FPE Fragment Counter Interrupt status not detected 0x1 (ACTIVE): MMC Tx FPE Fragment Counter Interrupt status detected Value After Reset: 0x0

2.3.87 EQOS_MAC_R_MMC_FPE_TX_INTERRUPT_MASK

Access Type: RW

Address Offset: 0x8a4

Name	Access	Bit Range	Reset value	Description
RESERVED_31_2	R	[31:2]	0x0	Reserved. Value After Reset: 0x0
HRCIM	R/W	[1:1]	0x0	MMC Transmit Hold Request Counter Interrupt Mask Setting this bit masks the interrupt when the Tx_Hold_Req_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration.Values:

				0x0 (DISABLE): MMC Transmit Hold Request Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Transmit Hold Request Counter Interrupt Mask is enabled Value After Reset: 0x0
FCIM	R/W	[0:0]	0x0	MMC Transmit Fragment Counter Interrupt Mask Setting this bit masks the interrupt when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.Values: 0x0 (DISABLE): MMC Transmit Fragment Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Transmit Fragment Counter Interrupt Mask is enabled Value After Reset: 0x0

2.3.88 EQOS_MAC_R_MMC_TX_FPE_FRAGMENT_CNTR

Access Type: RW

Address Offset: 0x8a8

Name	Access	Bit Range	Reset value	Description
TXFFC	R	[31:0]	0x0	Tx FPE Fragment counter This field indicates the number of additional mPackets that has been transmitted due to preemption Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. Value After Reset: 0x0

2.3.89 EQOS_MAC_R_MMC_TX_HOLD_REQ_CNTR

Access Type: RW

Address Offset: 0x8ac

Name	Access	Bit	Reset	Description

		Range	value	
TXHRC	R	[31:0]	0x0	Tx Hold Request Counter This field indicates count of number of a hold request is given to MAC. Exists when any one of the RX/TX MMC counters are enabled during FPE with AV_EST Enabled configuration. Value After Reset: 0x0

2.3.90 EQOS_MAC_R_MMC_FPE_RX_INTERRUPT

Access Type: RW

Address Offset: 0x8c0

Name	Access	Bit Range	Reset value	Description
RESERVED_31_4	R	[31:4]	0x0	Reserved. Value After Reset: 0x0
FCIS	R	[3:3]	0x0	MMC Rx FPE Fragment Counter Interrupt Status This bit is set when the Rx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.Values: 0x0 (INACTIVE): MMC Rx FPE Fragment Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Rx FPE Fragment Counter Interrupt Status detected Value After Reset: 0x0
PAOCIS	R	[2:2]	0x0	MMC Rx Packet Assembly OK Counter Interrupt Status This bit is set when the Rx_Packet_Assemble_Ok_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set

				to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.Values: 0x0 (INACTIVE): MMC Rx Packet Assembly OK Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Rx Packet Assembly OK Counter Interrupt Status detected Value After Reset: 0x0
PSECIS	R	[1:1]	0x0	MMC Rx Packet SMD Error Counter Interrupt Status This bit is set when the Rx_Packet_SMD_Err_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.Values: 0x0 (INACTIVE): MMC Rx Packet SMD Error Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Rx Packet SMD Error Counter Interrupt Status detected Value After Reset: 0x0
PAECIS	R	[0:0]	0x0	MMC Rx Packet Assembly Error Counter Interrupt Status This bit is set when the Rx_Packet_Assemble_Err_Cntr counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled

				configuration.Values: 0x0 (INACTIVE): MMC Rx Packet Assembly Error Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Rx Packet Assembly Error Counter Interrupt Status detected Value After Reset: 0x0

2.3.91 EQOS_MAC_R_MMC_FPE_RX_INTERRUPT_MASK

Access Type: RW

Address Offset: 0x8c4

Name	Access	Bit Range	Reset value	Description
RESERVED_31_4	R	[31:4]	0x0	Reserved. Value After Reset: 0x0
FCIM	R/W	[3:3]	0x0	MMC Rx FPE Fragment Counter Interrupt Mask Setting this bit masks the interrupt when the Tx_FPE_Fragment_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.Values: 0x0 (DISABLE): MMC Rx FPE Fragment Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Rx FPE Fragment Counter Interrupt Mask is enabled Value After Reset: 0x0
PAOCIM	R/W	[2:2]	0x0	MMC Rx Packet Assembly OK Counter Interrupt Mask Setting this bit masks the interrupt when the Rx_Packet_Assemble_Ok_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters

				are enabled during FPE Enabled configuration.Values: 0x0 (DISABLE): MMC Rx Packet Assembly OK Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Rx Packet Assembly OK Counter Interrupt Mask is enabled Value After Reset: 0x0
PSECIM	R/W	[1:1]	0x0	MMC Rx Packet SMD Error Counter Interrupt Mask Setting this bit masks the interrupt when the R Rx_Packet_SMD_Err_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.Values: 0x0 (DISABLE): MMC Rx Packet SMD Error Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Rx Packet SMD Error Counter Interrupt Mask is enabled Value After Reset: 0x0
PAECIM	R/W	[0:0]	0x0	MMC Rx Packet Assembly Error Counter Interrupt Mask Setting this bit masks the interrupt when the R Rx_Packet_Assemble_Err_Cntr counter reaches half of the maximum value or the maximum value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration.Values: 0x0 (DISABLE): MMC Rx Packet Assembly Error Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Rx Packet Assembly Error

				Counter Interrupt Mask is enabled Value After Reset: 0x0

2.3.92 EQOS_MAC_R_MMC_RX_PACKET_ASSEMBLY_ERR_CNTR

Access Type: RW

Address Offset: 0x8c8

Name	Access	Bit Range	Reset value	Description
PAEC	R	[31:0]	0x0	Rx Packet Assembly Error Counter This field indicates the number of MAC frames with reassembly errors on the Receiver, due to mismatch in the Fragment Count value. Exists when any one of the RX/TX MMC counters are enabled during FPE Enabled configuration. Value After Reset: 0x0

2.3.93 EQOS_MAC_R_MMC_RX_PACKET_SMD_ERR_CNTR

Access Type: RW

Address Offset: 0x8cc

Name	Access	Bit Range	Reset value	Description
PSEC	R	[31:0]	0x0	Rx Packet SMD Error Counter This field indicates the number of MAC frames rejected due to unknown SMD value and MAC frame fragments rejected due to arriving with an SMD-C when there was no preceding preempted frame. Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration. Value After Reset: 0x0

2.3.94 EQOS_MAC_R_MMC_RX_PACKET_ASSEMBLY_OK_CNTR

Access Type: RW

Address Offset: 0x8d0

Name	Access	Bit Range	Reset value	Description
PAOC	R	[31:0]	0x0	Rx Packet Assembly OK Counter This field indicates the number of MAC frames that were successfully reassembled and delivered to MAC. Exists when at least one of the RX/TX MMC counters are

				enabled during FPE Enabled configuration. Value After Reset: 0x0

2.3.95 EQOS_MAC_R_MMC_RX_FPE_FRAGMENT_CNTR

Access Type: RW

Address Offset: 0x8d4

Name	Access	Bit Range	Reset value	Description
FFC	R	[31:0]	0x0	Rx FPE Fragment Counter This field indicates the number of additional mPackets received due to preemption Exists when at least one of the RX/TX MMC counters are enabled during FPE Enabled configuration. Value After Reset: 0x0

2.3.96 EQOS_MAC_R_MAC_L3_L4_CONTROL(#I)(FORI=0;I<=1)

Access Type: RW

Address Offset: (0x0030*i)+0x0900

Name	Access	Bit Range	Reset value	Description
RESERVED_31_29	R	[31:29]	0x0	Reserved. Value After Reset: 0x0
DMCHEN0	R/W	[28:28]	0x0	DMA Channel Select Enable When set, this bit enables the selection of the DMA channel number for the packet that is passed by this L3_L4 filter. The DMA channel is indicated by the DMCHN bits. When this bit is reset, the DMA channel is not decided by this filter.Values: 0x0 (DISABLE): DMA Channel Select is disabled 0x1 (ENABLE): DMA Channel Select is enabled Value After Reset: 0x0
RESERVED_27_Y	R	[27:26]	0x0	Reserved. Value After Reset: 0x0
DMCHN0	R/W	[25:24]	0x0	

				DMA Channel Number When DMCHEN is set high, this field selects the DMA Channel number to which the packet passed by this filter is routed. The width of this field depends on the number of the DMA channels present in your configuration. Value After Reset: 0x0
RESERVED_23_22	R	[23:22]	0x0	Reserved. Value After Reset: 0x0
L4DPIM0	R/W	[21:21]	0x0	Layer 4 Destination Port Inverse Match Enable When this bit is set, the Layer 4 Destination Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Destination Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4DPM0 bit is set high.Values: 0x0 (DISABLE): Layer 4 Destination Port Inverse Match is disabled 0x1 (ENABLE): Layer 4 Destination Port Inverse Match is enabled Value After Reset: 0x0
L4DPM0	R/W	[20:20]	0x0	Layer 4 Destination Port Match Enable When this bit is set, the Layer 4 Destination Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Destination Port number field for matching.Values: 0x0 (DISABLE): Layer 4 Destination Port Match is disabled 0x1 (ENABLE): Layer 4 Destination Port Match is enabled Value After Reset: 0x0

L4SPIM0	R/W	[19:19]	0x0	Layer 4 Source Port Inverse Match Enable When this bit is set, the Layer 4 Source Port number field is enabled for inverse matching. When this bit is reset, the Layer 4 Source Port number field is enabled for perfect matching. This bit is valid and applicable only when the L4SPM0 bit is set high.Values: 0x0 (DISABLE): Layer 4 Source Port Inverse Match is disabled 0x1 (ENABLE): Layer 4 Source Port Inverse Match is enabled Value After Reset: 0x0
L4SPM0	R/W	[18:18]	0x0	Layer 4 Source Port Match Enable When this bit is set, the Layer 4 Source Port number field is enabled for matching. When this bit is reset, the MAC ignores the Layer 4 Source Port number field for matching.Values: 0x0 (DISABLE): Layer 4 Source Port Match is disabled 0x1 (ENABLE): Layer 4 Source Port Match is enabled Value After Reset: 0x0
RESERVED_17	R	[17:17]	0x0	Reserved. Value After Reset: 0x0
L4PEN0	R/W	[16:16]	0x0	Layer 4 Protocol Enable When this bit is set, the Source and Destination Port number fields of UDP packets are used for matching. When this bit is reset, the Source and Destination Port number fields of TCP packets are used for matching. The Layer 4 matching is done only when the

				L4SPM0 or L4DPM0 bit is set.Values: 0x0 (DISABLE): Layer 4 Protocol is disabled 0x1 (ENABLE): Layer 4 Protocol is enabled Value After Reset: 0x0
L3HDBM0	R/W	[15:11]	0x0	Layer 3 IP DA Higher Bits Match IPv4 Packets: This field contains the number of higher bits of IP Destination Address that are matched in the IPv4 packets. The following list describes the values of this field: 0: No bits are masked. 1: LSb[0] is masked 2: Two LSbs [1:0] are masked .. 31: All bits except MSb are masked. IPv6 Packets: Bits[12:11] of this field correspond to Bits[6:5] of L3HSBM0 which indicate the number of lower bits of IP Source or Destination Address that are masked in the IPv6 packets. The following list describes the concatenated values of the L3HDBM0[1:0] and L3HSBM0 bits: 0: No bits are masked. 1: LSb[0] is masked. 2: Two LSbs [1:0] are masked .. 127: All bits except MSb are masked.

				This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set. Value After Reset: 0x0
L3HSBM0	R/W	[10:6]	0x0	Layer 3 IP SA Higher Bits Match IPv4 Packets: This field contains the number of lower bits of IP Source Address that are masked for matching in the IPv4 packets. The following list describes the values of this field: 0: No bits are masked. 1: LSb[0] is masked 2: Two LSbs [1:0] are masked .. 31: All bits except MSb are masked. IPv6 Packets: This field contains Bits[4:0] of L3HSBM0. These bits indicate the number of higher bits of IP Source or Destination Address matched in the IPv6 packets. This field is valid and applicable only when the L3DAM0 or L3SAM0 bit is set high. Value After Reset: 0x0
L3DAIM0	R/W	[5:5]	0x0	Layer 3 IP DA Inverse Match Enable When this bit is set, the Layer 3 IP Destination Address field is enabled for inverse matching. When this bit is reset, the Layer 3 IP Destination Address field is enabled for perfect matching. This bit is valid and applicable only when the L3DAM0 bit is set high.Values: 0x0 (DISABLE): Layer 3 IP DA Inverse Match is disabled 0x1 (ENABLE): Layer 3 IP DA Inverse Match is enabled

				Value After Reset: 0x0
L3DAM0	R/W	[4:4]	0x0	Layer 3 IP DA Match Enable When this bit is set, the Layer 3 IP Destination Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Destination Address field for matching. Note: When the L3PEN0 bit is set, you should set either this bit or the L3SAM0 bit because either IPv6 DA or SA can be checked for filtering.Values: 0x0 (DISABLE): Layer 3 IP DA Match is disabled 0x1 (ENABLE): Layer 3 IP DA Match is enabled Value After Reset: 0x0
L3SAIM0	R/W	[3:3]	0x0	Layer 3 IP SA Inverse Match Enable When this bit is set, the Layer 3 IP Source Address field is enabled for inverse matching. When this bit reset, the Layer 3 IP Source Address field is enabled for perfect matching. This bit is valid and applicable only when the L3SAM0 bit is set.Values: 0x0 (DISABLE): Layer 3 IP SA Inverse Match is disabled 0x1 (ENABLE): Layer 3 IP SA Inverse Match is enabled Value After Reset: 0x0
L3SAM0	R/W	[2:2]	0x0	Layer 3 IP SA Match Enable When this bit is set, the Layer 3 IP Source Address field is enabled for matching. When this bit is reset, the MAC ignores the Layer 3 IP Source Address field for matching.

				Note: When the L3PEN0 bit is set, you should set either this bit or the L3DAM0 bit because either IPv6 SA or DA can be checked for filtering.Values: 0x0 (DISABLE): Layer 3 IP SA Match is disabled 0x1 (ENABLE): Layer 3 IP SA Match is enabled Value After Reset: 0x0
RESERVED_1	R	[1:1]	0x0	Reserved. Value After Reset: 0x0
L3PEN0	R/W	[0:0]	0x0	Layer 3 Protocol Enable When this bit is set, the Layer 3 IP Source or Destination Address matching is enabled for IPv6 packets. When this bit is reset, the Layer 3 IP Source or Destination Address matching is enabled for IPv4 packets. The Layer 3 matching is done only when the L3SAM0 or L3DAM0 bit is set.Values: 0x0 (DISABLE): Layer 3 Protocol is disabled 0x1 (ENABLE): Layer 3 Protocol is enabled Value After Reset: 0x0

2.3.97 EQOS_MAC_R_MAC_LAYER4_ADDRESS(#I)(FORI=0;I<=1)

Access Type: RW

Address Offset: (0x0030*i)+0x0904

Name	Access	Bit Range	Reset value	Description
L4DP0	R/W	[31:16]	0x0	Layer 4 Destination Port Number Field When the L4PEN0 bit is reset and the L4DPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Destination Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4DPM0 bits are set in

				MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Destination Port Number field in the IPv4 or IPv6 packets. Value After Reset: 0x0
L4SP0	R/W	[15:0]	0x0	Layer 4 Source Port Number Field When the L4PEN0 bit is reset and the L4SPM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the TCP Source Port Number field in the IPv4 or IPv6 packets. When the L4PEN0 and L4SPM0 bits are set in MAC_L3_L4_Control0 register, this field contains the value to be matched with the UDP Source Port Number field in the IPv4 or IPv6 packets. Value After Reset: 0x0

2.3.98 EQOS_MAC_R_MAC_LAYER3_ADDR0_REG(#I)(FORI=0;I<=1)

Access Type: RW

Address Offset: (0x0030*i)+0x0910

Name	Access	Bit Range	Reset value	Description
L3A00	R/W	[31:0]	0x0	Layer 3 Address 0 Field When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[31:0] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Source Address field in the IPv4 packets. Value After Reset: 0x0

2.3.99 EQOS_MAC_R_MAC_LAYER3_ADDR1_REG(#I)(FORI=0;I<=1)

Access Type: RW

Address Offset: (0x0030*i)+0x0914

Name	Access	Bit Range	Reset value	Description
L3A10	R/W	[31:0]	0x0	Layer 3 Address 1 Field

				When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[63:32] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset and the L3SAM0 bit is set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with the IP Destination Address field in the IPv4 packets. Value After Reset: 0x0

2.3.100 EQOS_MAC_R_MAC_LAYER3_ADDR2_REG(#I)(FORI=0;I<=1)

Access Type: RW

Address Offset: (0x0030*i)+0x0918

Name	Access	Bit Range	Reset value	Description
L3A20	R/W	[31:0]	0x0	Layer 3 Address 2 Field When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Source Address field in the IPv6 packets. When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[95:64] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used. Value After Reset: 0x0

2.3.101 EQOS_MAC_R_MAC_LAYER3_ADDR3_REG(#I)(FORI=0;I<=1)

Access Type: RW

Address Offset: (0x0030*i)+0x091C

Name	Access	Bit Range	Reset value	Description
L3A30	R/W	[31:0]	0x0	Layer 3 Address 3 Field When the L3PEN0 and L3SAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Source Address field in the IPv6 packets.

				When the L3PEN0 and L3DAM0 bits are set in the MAC_L3_L4_Control0 register, this field contains the value to be matched with Bits[127:96] of the IP Destination Address field in the IPv6 packets. When the L3PEN0 bit is reset in the MAC_L3_L4_Control0 register, this field is not used. Value After Reset: 0x0

2.3.102 EQOS_MAC_R_MAC_TIMESTAMP_CONTROL

Access Type: RW

Address Offset: 0xb00

Name	Access	Bit Range	Reset value	Description
RESERVED_31_29	R	[31:29]	0x0	Reserved. Value After Reset: 0x0
AV8021ASMEN	R/W	[28:28]	0x0	AV 802.1AS Mode Enable When this bit is set, the MAC processes only untagged PTP over Ethernet packets for providing PTP status and capturing timestamp snapshots, that is, IEEE 802.1AS mode of operation. When PTP offload feature is enabled, for the purpose of PTP offload, the transport specific field in the PTP header is generated and checked based on the value of this bit.Values: 0x0 (DISABLE): AV 802.1AS Mode is disabled 0x1 (ENABLE): AV 802.1AS Mode is enabled Value After Reset: 0x0
RESERVED_27_25	R	[27:25]	0x0	Reserved. Value After Reset: 0x0
TXTSSTSM	R/W	[24:24]	0x0	Transmit Timestamp Status Mode When this bit is set, the MAC overwrites the earlier transmit timestamp status even if it is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds

				register. When this bit is reset, the MAC ignores the timestamp status of current packet if the timestamp status of previous packet is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register.Values: 0x0 (DISABLE): Transmit Timestamp Status Mode is disabled 0x1 (ENABLE): Transmit Timestamp Status Mode is enabled Value After Reset: 0x0
RESERVED_23_21	R	[23:21]	0x0	Reserved. Value After Reset: 0x0
ESTI	R/W	[20:20]	0x0	External System Time Input When this bit is set, the MAC uses the external 64-bit reference System Time input for the following: To take the timestamp provided as status To insert the timestamp in transmit PTP packets when One-step Timestamp or Timestamp Offload feature is enabled. When this bit is reset, the MAC uses the internal reference System Time.Values: 0x0 (DISABLE): External System Time Input is disabled 0x1 (ENABLE): External System Time Input is enabled Value After Reset: 0x0

RESERVED	R	[19:19]	0x0	Reserved Field: Yes
TSENMACADDR	R/W	[18:18]	0x0	Enable MAC Address for PTP Packet Filtering When this bit is set, the DA MAC address (that matches any MAC Address register) is used to filter the PTP packets when PTP is directly sent over Ethernet. When this bit is set, received PTP packets with DA containing a special multicast or unicast address that matches the one programmed in MAC address registers are considered for processing as indicated below, when PTP is directly sent over Ethernet. For normal time stamping operation, MAC address registers 0 to 31 is considered for unicast destination address matching. For PTP offload, only MAC address register 0 is considered for unicast destination address matching.Values: 0x0 (DISABLE): MAC Address for PTP Packet Filtering is disabled 0x1 (ENABLE): MAC Address for PTP Packet Filtering is enabled Value After Reset: 0x0
SNAPTYPSEL	R/W	[17:16]	0x0	Select PTP packets for Taking Snapshots These bits, along with Bits 15 and 14, decide the set of PTP packet types for which snapshot needs to be taken. The encoding is given in Timestamp Snapshot Dependency on Register Bits Table. Value After Reset: 0x0
TSMSTRENA	R/W	[15:15]	0x0	Enable Snapshot for Messages Relevant to Master When this bit is set, the snapshot is taken only for the messages that are relevant to the master node. Otherwise, the snapshot is taken for the messages relevant to the slave node.Values: 0x0 (DISABLE): Snapshot for Messages Relevant to Master is disabled

				0x1 (ENABLE): Snapshot for Messages Relevant to Master is enabled Value After Reset: 0x0
TSEVNTENA	R/W	[14:14]	0x0	Enable Timestamp Snapshot for Event Messages When this bit is set, the timestamp snapshot is taken only for event messages (SYNC, Delay_Req, Pdelay_Req, or Pdelay_Resp). When this bit is reset, the snapshot is taken for all messages except Announce, Management, and Signaling. For more information about the timestamp snapshots, see Timestamp Snapshot Dependency on Register Bits Table.Values: 0x0 (DISABLE): Timestamp Snapshot for Event Messages is disabled 0x1 (ENABLE): Timestamp Snapshot for Event Messages is enabled Value After Reset: 0x0
TSIPV4ENA	R/W	[13:13]	0x1	Enable Processing of PTP Packets Sent over IPv4-UDP When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv4-UDP packets. When this bit is reset, the MAC ignores the PTP transported over IPv4-UDP packets. This bit is set by default.Values: 0x0 (DISABLE): Processing of PTP Packets Sent over IPv4-UDP is disabled 0x1 (ENABLE): Processing of PTP Packets Sent over IPv4-UDP is enabled Value After Reset: 0x1
TSIPV6ENA	R/W	[12:12]	0x0	

				Enable Processing of PTP Packets Sent over IPv6-UDP When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv6-UDP packets. When this bit is clear, the MAC ignores the PTP transported over IPv6-UDP packets.Values: 0x0 (DISABLE): Processing of PTP Packets Sent over IPv6-UDP is disabled 0x1 (ENABLE): Processing of PTP Packets Sent over IPv6-UDP is enabled Value After Reset: 0x0
TSIPENA	R/W	[11:11]	0x0	Enable Processing of PTP over Ethernet Packets When this bit is set, the MAC receiver processes the PTP packets encapsulated directly in the Ethernet packets. When this bit is reset, the MAC ignores the PTP over Ethernet packets.Values: 0x0 (DISABLE): Processing of PTP over Ethernet Packets is disabled 0x1 (ENABLE): Processing of PTP over Ethernet Packets is enabled Value After Reset: 0x0
TSVER2ENA	R/W	[10:10]	0x0	Enable PTP Packet Processing for Version 2 Format When this bit is set, the IEEE 1588 version 2 format is used to process the PTP packets. When this bit is reset, the IEEE 1588 version 1 format is used to process the PTP packets. The IEEE 1588 formats are described in 'PTP Processing and Control'.Values: 0x0 (DISABLE): PTP Packet Processing for Version 2 Format is disabled 0x1 (ENABLE): PTP Packet Processing for Version

				2 Format is enabled Value After Reset: 0x0
TSCTRLSSR	R/W	[9:9]	0x0	Timestamp Digital or Binary Rollover Control When this bit is set, the Timestamp Low register rolls over after 0x3B9A_C9FF value (that is, 1 nanosecond accuracy) and increments the timestamp (High) seconds. When this bit is reset, the rollover value of sub-second register is 0x7FFF_FFFF. The sub-second increment must be programmed correctly depending on the PTP reference clock frequency and the value of this bit.Values: 0x0 (DISABLE): Timestamp Digital or Binary Rollover Control is disabled 0x1 (ENABLE): Timestamp Digital or Binary Rollover Control is enabled Value After Reset: 0x0
TSENALL	R/W	[8:8]	0x0	Enable Timestamp for All Packets When this bit is set, the timestamp snapshot is enabled for all packets received by the MAC.Values: 0x0 (DISABLE): Timestamp for All Packets disabled 0x1 (ENABLE): Timestamp for All Packets enabled Value After Reset: 0x0
RESERVED_7	R	[7:7]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[6:6]	0x0	Reserved Field: Yes

TSADDREG	R/W	[5:5]	0x0	Update Addend Register When this bit is set, the content of the Timestamp Addend register is updated in the PTP block for fine correction. This bit is cleared when the update is complete. This bit should be zero before it is set. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.Values: 0x0 (DISABLE): Addend Register is not updated 0x1 (ENABLE): Addend Register is updated Value After Reset: 0x0 Testable: untestable
TSTRIG	R/W	[4:4]	0x0	Enable Timestamp Interrupt Trigger When this bit is set, the timestamp interrupt is generated when the System Time becomes greater than the value written in the Target Time register. This bit is reset after the Timestamp Trigger Interrupt is generated. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.Values: 0x0 (DISABLE): Timestamp Interrupt Trigger is not enabled 0x1 (ENABLE): Timestamp Interrupt Trigger is enabled Value After Reset: 0x0 Testable: untestable
TSUPDT	R/W	[3:3]	0x0	Update Timestamp When this bit is set, the system time is updated (added or subtracted) with the value specified in MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before updating it. This bit

				is reset when the update is complete in hardware. The Timestamp Higher Word register (if enabled during core configuration) is not updated. When Media Clock Generation and Recovery is configured (DWC_EQOS_FLEXI_PPS_OUT_EN) and enabled MAC_Presn_Time_Updt should also be updated before setting this field. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.Values: 0x0 (DISABLE): Timestamp is not updated 0x1 (ENABLE): Timestamp is updated Value After Reset: 0x0 Testable: untestable
TSINIT	R/W	[2:2]	0x0	Initialize Timestamp When this bit is set, the system time is initialized (overwritten) with the value specified in the MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before it is updated. This bit is reset when the initialization is complete. The Timestamp Higher Word register (if enabled during core configuration) can only be initialized. When Media Clock Generation and Recovery is configured (DWC_EQOS_FLEXI_PPS_OUT_EN) and enabled MAC_Presn_Time_Updt should also be updated before setting this field. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.Values: 0x0 (DISABLE): Timestamp is not initialized 0x1 (ENABLE): Timestamp is initialized Value After Reset: 0x0 Testable: untestable
TSCFUPDT	R/W	[1:1]	0x0	

				Fine or Coarse Timestamp Update When this bit is set, the Fine method is used to update system timestamp. When this bit is reset, Coarse method is used to update the system timestamp.Values: 0x0 (COARSE): Coarse method is used to update system timestamp 0x1 (FINE): Fine method is used to update system timestamp Value After Reset: 0x0
TSENA	R/W	[0:0]	0x0	Enable Timestamp When this bit is set, the timestamp is added for Transmit and Receive packets. When disabled, timestamp is not added for transmit and receive packets and the Timestamp Generator is also suspended. You need to initialize the Timestamp (system time) after enabling this mode. On the Receive side, the MAC processes the 1588 packets only if this bit is set.Values: 0x0 (DISABLE): Timestamp is disabled 0x1 (ENABLE): Timestamp is enabled Value After Reset: 0x0

2.3.103 EQOS_MAC_R_MAC_SUB_SECOND_INCREMENT

Access Type: RW

Address Offset: 0xb04

Name	Access	Bit Range	Reset value	Description
RESERVED_31_24	R	[31:24]	0x0	Reserved. Value After Reset: 0x0
SSINC	R/W	[23:16]	0x0	Sub-second Increment Value The value programmed in this field is accumulated

				every clock cycle (of clk_ptp_i) with the contents of the sub-second register. For example, when the PTP clock is 50 MHz (period is 20 ns), you should program 20 (0x14) when the System Time Nanoseconds register has an accuracy of 1 ns [Bit 9 (TSCTRLSSR) is set in MAC_Timestamp_Control]. When TSCTRLSSR is clear, the Nanoseconds register has a resolution of ~0.465 ns. In this case, you should program a value of 43 (0x2B) which is derived by 20 ns/0.465. Value After Reset: 0x0
SNSINC	R/W	[15:8]	0x0	Sub-nanosecond Increment Value This field contains the sub-nanosecond increment value, represented in nanoseconds multiplied by 2^8. This value is accumulated with the sub-nanoseconds field of the subsecond register. For example, when TSCTRLSSR field in the MAC_Timestamp_Control register is set. and if the required increment is 5.3ns, then SSINC should be 0x05 and SNSINC should be 0x4C. Value After Reset: 0x0
RESERVED_7_0	R	[7:0]	0x0	Reserved. Value After Reset: 0x0

2.3.104 EQOS_MAC_R_MAC_SYSTEM_TIME_SECONDS

Access Type: RW

Address Offset: 0xb08

Name	Access	Bit Range	Reset value	Description
TSS	R	[31:0]	0x0	Timestamp Second The value in this field indicates the current value in seconds of the System Time maintained by the MAC. Value After Reset: 0x0

2.3.105 EQOS_MAC_R_MAC_SYSTEM_TIME_NANOSECONDS

Access Type: RW

Address Offset: 0xb0c

Name	Access	Bit	Reset	Description

		Range	value	
RESERVED_31	R	[31:31]	0x0	Reserved. Value After Reset: 0x0
TSSS	R	[30:0]	0x0	Timestamp Sub Seconds The value in this field has the sub-second representation of time, with an accuracy of 0.46 ns. When Bit 9 is set in MAC_Timestamp_Control, each bit represents 1 ns. The maximum value is 0x3B9A_C9FF after which it rolls-over to zero. Value After Reset: 0x0

2.3.106 EQOS_MAC_R_MAC_SYSTEM_TIME_SECONDS_UPDATE

Access Type: RW

Address Offset: 0xb10

Name	Access	Bit Range	Reset value	Description
TSS	R/W	[31:0]	0x0	Timestamp Seconds The value in this field is the seconds part of the update. When ADDSUB is reset, this field must be programmed with the seconds part of the update value. When ADDSUB is set, this field must be programmed with the complement of the seconds part of the update value. For example, if 2.000000001 seconds need to be subtracted from the system time, the TSS field in the MAC_Timestamp_Seconds_Update register must be 0xFFFF_FFFE (that is, 2^32 - 2). Value After Reset: 0x0

2.3.107 EQOS_MAC_R_MAC_SYSTEM_TIME_NANOSECONDS_UPDATE

Access Type: RW

Address Offset: 0xb14

Name	Access	Bit Range	Reset value	Description
ADDSUB	R/W	[31:31]	0x0	Add or Subtract Time When this bit is set, the time value is subtracted with the contents of the update register. When this bit is reset, the time value is added with the contents of the update register.Values: 0x0 (ADD): Add time

				0x1 (SUB): Subtract time Value After Reset: 0x0
TSSS	R/W	[30:0]	0x0	Timestamp Sub Seconds The value in this field is the sub-seconds part of the update. When ADDSUB is reset, this field must be programmed with the sub-seconds part of the update value, with an accuracy based on the TSCTRLSSR bit of the MAC_Timestamp_Control register. When ADDSUB is set, this field must be programmed with the complement of the sub-seconds part of the update value as described below. When TSCTRLSSR bit in MAC_Timestamp_Control is set, the programmed value must be 10^9 - . When TSCTRLSSR bit in MAC_Timestamp_Control is reset, the programmed value must be 2^31 - . When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, each bit represents an accuracy of 0.46 ns. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, each bit represents 1 ns and the programmed value should not exceed 0x3B9A_C9FF. For example, if 2.000000001 seconds need to be subtracted from the system time, then the TSSS field in the MAC_Timestamp_Nanoseconds_Update register must be 0x7FFF_FFFF (that is, 2^31 - 1), when TSCTRLSSR bit in MAC_Timestamp_Control is reset and 0x3B9A_C9FF (that is, 10^9 - 1), when TSCTRLSSR bit in MAC_Timestamp_Control is set. Value After Reset: 0x0

2.3.108 EQOS_MAC_R_MAC_TIMESTAMP_ADDEND

Access Type: RW

Address Offset: 0xb18

Name	Access	Bit Range	Reset value	Description
TSAR	R/W	[31:0]	0x0	Timestamp Addend Register This field indicates the 32-bit time value to be added to the Accumulator register to achieve time synchronization. Value After Reset: 0x0

2.3.109 EQOS_MAC_R_MAC_SYSTEM_TIME_HIGHER_WORD_SECONDS

Access Type: RW

Address Offset: 0xb1c

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
TSHWR	R/W	[15:0]	0x0	Timestamp Higher Word Register This field contains the most-significant 16-bits of timestamp seconds value. This register is optional. You can add this register by selecting the Add IEEE 1588 Higher Word Register option. This register is directly written to initialize the value and it is incremented when there is an overflow from 32-bits of the System Time Seconds register. Access restriction applies. Updated based on the event. Setting 1 sets. Setting 0 clears. Value After Reset: 0x0

2.3.110 EQOS_MAC_R_MAC_TIMESTAMP_STATUS

Access Type: RW

Address Offset: 0xb20

Name	Access	Bit Range	Reset value	Description
RESERVED_31_30	R	[31:30]	0x0	Reserved. Value After Reset: 0x0
ATSNS	R	[29:25]	0x0	Number of Auxiliary Timestamp Snapshots This field indicates the number of Snapshots available in the FIFO. A value equal to the selected depth of FIFO (4, 8, or 16) indicates that the Auxiliary Snapshot FIFO is full. These bits are cleared (to 00000) when the Auxiliary snapshot FIFO clear bit is set. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected. Value After Reset: 0x0
ATSSTM	R	[24:24]	0x0	Auxiliary Timestamp Snapshot Trigger Missed This bit is set when the Auxiliary timestamp

				snapshot FIFO is full and external trigger was set. This indicates that the latest snapshot is not stored in the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected.Values: 0x0 (INACTIVE): Auxiliary Timestamp Snapshot Trigger Missed status not detected 0x1 (ACTIVE): Auxiliary Timestamp Snapshot Trigger Missed status detected Value After Reset: 0x0
RESERVED_23_20	R	[23:20]	0x0	Reserved. Value After Reset: 0x0
ATSSTN	R	[19:16]	0x0	Auxiliary Timestamp Snapshot Trigger Identifier These bits identify the Auxiliary trigger inputs for which the timestamp available in the Auxiliary Snapshot Register is applicable. When more than one bit is set at the same time, it means that corresponding auxiliary triggers were sampled at the same clock. These bits are applicable only if the number of Auxiliary snapshots is more than one. One bit is assigned for each trigger as shown in the following list: Bit 16: Auxiliary trigger 0 Bit 17: Auxiliary trigger 1 Bit 18: Auxiliary trigger 2 Bit 19: Auxiliary trigger 3 The software can read this register to find the triggers that are set when the timestamp is taken. Access restriction applies. Clears on read. Self-set to 1 on internal event. Value After Reset: 0x0
TXTSSIS	R	[15:15]	0x0	Tx Timestamp Status Interrupt Status

				In non-EQOS_CORE configurations when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers. When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers, for PTO generated Delay Request and Pdelay request packets. This bit is cleared when the MAC_Tx_Timestamp_Status_Seconds register is read (or write to MAC_Tx_Timestamp_Status_Seconds register when RCWE bit of MAC_CSR_SW_Ctrl register is set).Values: 0x0 (INACTIVE): Tx Timestamp Status Interrupt status not detected 0x1 (ACTIVE): Tx Timestamp Status Interrupt status detected Value After Reset: 0x0
RESERVED_14_10	R	[14:10]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[9:4]	0x0	Reserved Field: Yes
TSTRGTERR0	R	[3:3]	0x0	Timestamp Target Time Error This bit is set when the latest target time programmed in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers elapses. This bit is cleared when the application reads this bit. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.Values:

				0x0 (INACTIVE): Timestamp Target Time Error status not detected 0x1 (ACTIVE): Timestamp Target Time Error status detected Value After Reset: 0x0
AUXTSTRIG	R	[2:2]	0x0	Auxiliary Timestamp Trigger Snapshot This bit is set high when the auxiliary snapshot is written to the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.Values: 0x0 (INACTIVE): Auxiliary Timestamp Trigger Snapshot status not detected 0x1 (ACTIVE): Auxiliary Timestamp Trigger Snapshot status detected Value After Reset: 0x0
TSTARGT0	R	[1:1]	0x0	Timestamp Target Time Reached When set, this bit indicates that the value of system time is greater than or equal to the value specified in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.Values: 0x0 (INACTIVE): Timestamp Target Time Reached status not detected 0x1 (ACTIVE): Timestamp Target Time Reached status detected

				Value After Reset: 0x0
TSSOVF	R	[0:0]	0x0	Timestamp Seconds Overflow When this bit is set, it indicates that the seconds value of the timestamp (when supporting version 2 format) has overflowed beyond 32'hFFFF_FFFF. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event.Values: 0x0 (INACTIVE): Timestamp Seconds Overflow status not detected 0x1 (ACTIVE): Timestamp Seconds Overflow status detected Value After Reset: 0x0

2.3.111 EQOS_MAC_R_MAC_TX_TIMESTAMP_STATUS_NANOSECONDS

Access Type: RW

Address Offset: 0xb30

Name	Access	Bit Range	Reset value	Description
TXTSSMIS	R	[31:31]	0x0	Transmit Timestamp Status Missed When this bit is set, it indicates one of the following: The timestamp of the current packet is ignored if TXTSSTSM bit of the MAC_Timestamp_Control register is reset The timestamp of the previous packet is overwritten with timestamp of the current packet if TXTSSTSM bit of the MAC_Timestamp_Control register is set. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): Transmit Timestamp Status Missed status not detected

				0x1 (ACTIVE): Transmit Timestamp Status Missed status detected Value After Reset: 0x0
TXTSSLO	R	[30:0]	0x0	Transmit Timestamp Status Low This field contains the 31 bits of the Nanoseconds field of the Transmit packet's captured timestamp. Value After Reset: 0x0

2.3.112 EQOS_MAC_R_MAC_TX_TIMESTAMP_STATUS_SECONDS

Access Type: RW

Address Offset: 0xb34

Name	Access	Bit Range	Reset value	Description
TXTSSHI	R	[31:0]	0x0	Transmit Timestamp Status High This field contains the lower 32 bits of the Seconds field of Transmit packet's captured timestamp. Value After Reset: 0x0

2.3.113 EQOS_MAC_R_MAC_AUXILIARY_CONTROL

Access Type: RW

Address Offset: 0xb40

Name	Access	Bit Range	Reset value	Description
RESERVED_31_8	R	[31:8]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[7:6]	0x0	Reserved Field: Yes
ATSEN1	R/W	[5:5]	0x0	Auxiliary Snapshot 1 Enable This bit controls the capturing of Auxiliary Snapshot Trigger 1. When this bit is set, the auxiliary snapshot of the event on ptp_aux_trig_i[1] input is enabled. When this bit is reset, the events on this input are ignored.Values: 0x0 (DISABLE): Auxiliary Snapshot $i is disabled 0x1 (ENABLE): Auxiliary Snapshot $i is enabled

				Value After Reset: 0x0
ATSEN0	R/W	[4:4]	0x0	Auxiliary Snapshot 0 Enable This bit controls the capturing of Auxiliary Snapshot Trigger 0. When this bit is set, the auxiliary snapshot of the event on ptp_aux_trig_i[0] input is enabled. When this bit is reset, the events on this input are ignored.Values: 0x0 (DISABLE): Auxiliary Snapshot $i is disabled 0x1 (ENABLE): Auxiliary Snapshot $i is enabled Value After Reset: 0x0
RESERVED_3_1	R	[3:1]	0x0	Reserved. Value After Reset: 0x0
ATSFC	R/W	[0:0]	0x0	Auxiliary Snapshot FIFO Clear When set, this bit resets the pointers of the Auxiliary Snapshot FIFO. This bit is cleared when the pointers are reset and the FIFO is empty. When this bit is high, the auxiliary snapshots are stored in the FIFO. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.Values: 0x0 (DISABLE): Auxiliary Snapshot FIFO Clear is disabled 0x1 (ENABLE): Auxiliary Snapshot FIFO Clear is enabled Value After Reset: 0x0 Testable: untestable

2.3.114 EQOS_MAC_R_MAC_AUXILIARY_TIMESTAMP_NANOSECONDS

Access Type: RW

Address Offset: 0xb48

Name	Access	Bit	Reset	Description

		Range	value	
RESERVED_31	R	[31:31]	0x0	Reserved. Value After Reset: 0x0
AUXTSLO	R	[30:0]	0x0	Auxiliary Timestamp Contains the lower 31 bits (nanoseconds field) of the auxiliary timestamp. Value After Reset: 0x0

2.3.115 EQOS_MAC_R_MAC_AUXILIARY_TIMESTAMP_SECONDS

Access Type: RW

Address Offset: 0xb4c

Name	Access	Bit Range	Reset value	Description
AUXTSHI	R	[31:0]	0x0	Auxiliary Timestamp Contains the lower 32 bits of the Seconds field of the auxiliary timestamp. Value After Reset: 0x0

2.3.116 EQOS_MAC_R_MAC_TIMESTAMP_INGRESS_ASYM_CORR

Access Type: RW

Address Offset: 0xb50

Name	Access	Bit Range	Reset value	Description
OSTIAC	R/W	[31:0]	0x0	One-Step Timestamp Ingress Asymmetry Correction This field contains the ingress path asymmetry value to be added to correctionField of Pdelay_Resp PTP packet. The programmed value should be in units of nanoseconds and multiplied by 2^16. For example, 2.5 ns is represented as 0x00028000. The value can also be negative, which is represented in 2's complement form with bit 31 representing the sign bit. Value After Reset: 0x0

2.3.117 EQOS_MAC_R_MAC_TIMESTAMP_EGRESS_ASYM_CORR

Access Type: RW

Address Offset: 0xb54

Name	Access	Bit Range	Reset value	Description
OSTEAC	R/W	[31:0]	0x0	

				One-Step Timestamp Egress Asymmetry Correction This field contains the egress path asymmetry value to be subtracted from correctionField of Pdelay_Resp PTP packet. The programmed value must be the negated value in units of nanoseconds multiplied by 2^16. For example, if the required correction is +2.5 ns, the programmed value must be 0xFFFD_8000, which is the 2's complement of 0x0002_8000(2.5 * 216). Similarly, if the required correction is -3.3 ns, the programmed value is 0x0003_4CCC (3.3 * 216). Value After Reset: 0x0

2.3.118 EQOS_MAC_R_MAC_TIMESTAMP_INGRESS_CORR_NANOSECOND

Access Type: RW

Address Offset: 0xb58

Name	Access	Bit Range	Reset value	Description
TSIC	R/W	[31:0]	0x0	Timestamp Ingress Correction This field contains the ingress path correction value as defined by the Ingress Correction expression. Value After Reset: 0x0

2.3.119 EQOS_MAC_R_MAC_TIMESTAMP_EGRESS_CORR_NANOSECOND

Access Type: RW

Address Offset: 0xb5c

Name	Access	Bit Range	Reset value	Description
TSEC	R/W	[31:0]	0x0	Timestamp Egress Correction This field contains the nanoseconds part of the egress path correction value as defined by the Egress Correction expression. Value After Reset: 0x0

2.3.120 EQOS_MAC_R_MAC_TIMESTAMP_INGRESS_CORR_SUBNANOSEC

Access Type: RW

Address Offset: 0xb60

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved.

				Value After Reset: 0x0
TSICSNS	R/W	[15:8]	0x0	Timestamp Ingress Correction, sub-nanoseconds This field contains the sub-nanoseconds part of the ingress path correction value as defined by the "Ingress Correction" expression. Value After Reset: 0x0
RESERVED_7_0	R	[7:0]	0x0	Reserved. Value After Reset: 0x0

2.3.121 EQOS_MAC_R_MAC_TIMESTAMP_EGRESS_CORR_SUBNANOSEC

Access Type: RW

Address Offset: 0xb64

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
TSECSNS	R/W	[15:8]	0x0	Timestamp Egress Correction, sub-nanoseconds This field contains the sub-nanoseconds part of the egress path correction value as defined by the "Egress Correction" expression. Value After Reset: 0x0
RESERVED_7_0	R	[7:0]	0x0	Reserved. Value After Reset: 0x0

2.3.122 EQOS_MAC_R_MAC_TIMESTAMP_INGRESS_LATENCY

Access Type: RW

Address Offset: 0xb68

Name	Access	Bit Range	Reset value	Description
RESERVED_31_28	R	[31:28]	0x0	Reserved. Value After Reset: 0x0
ITLNS	R	[27:16]	0x0	Ingress Timestamp Latency, in sub-nanoseconds This register holds the average latency in sub-nanoseconds between the input ports

				(phy_rxd_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken. Ingress correction value is computed as described in the section 7.1.2.4.1 of QoS Databook. Value After Reset: 0x0 Testable: untestable
ITLSNS	R	[15:8]	0x0	Ingress Timestamp Latency, in nanoseconds This register holds the average latency in nanoseconds between the input ports (phy_rxd_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken. Ingress correction value is computed as described in the section 7.1.2.4.1 of QoS Databook. Value After Reset: 0x0 Testable: untestable
RESERVED_7_0	R	[7:0]	0x0	Reserved. Value After Reset: 0x0

2.3.123 EQOS_MAC_R_MAC_TIMESTAMP_EGRESS_LATENCY

Access Type: RW

Address Offset: 0xb6c

Name	Access	Bit Range	Reset value	Description
RESERVED_31_28	R	[31:28]	0x0	Reserved. Value After Reset: 0x0
ETLNS	R	[27:16]	0x0	Egress Timestamp Latency, in nanoseconds This register holds the average latency in nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_txd_o) of the MAC. Ingress correction value is computed as described in the section 7.1.2.4.2 of QoS Databook. Value After Reset: 0x0 Testable: untestable
ETLSNS	R	[15:8]	0x0	Egress Timestamp Latency, in sub-nanoseconds

				This register holds the average latency in sub-nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_txd_o) of the MAC. Ingress correction value is computed as described in the section 7.1.2.4.2 of QoS Databook. Value After Reset: 0x0 Testable: untestable
RESERVED_7_0	R	[7:0]	0x0	Reserved. Value After Reset: 0x0

2.3.124 EQOS_MAC_R_MAC_PPS_CONTROL

Access Type: RW

Address Offset: 0xb70

Name	Access	Bit Range	Reset value	Description
RESERVED	R	[31:29]	0x0	Reserved Field: Yes
RESERVED_28	R	[28:28]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[27:21]	0x0	Reserved Field: Yes
RESERVED_20	R	[20:20]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[19:13]	0x0	Reserved Field: Yes
RESERVED_12	R	[12:12]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[11:4]	0x0	Reserved Field: Yes
PPSCTRL_PPSCMD	R/W	[3:0]	0x0	PPS Output Frequency Control This field controls the frequency of the PPS0 output (ptp_pps_o[0]) signal. The default value of PPSCTRL is 0000, and the PPS output is 1 pulse (of width clk_ptp_i) every second. For other values of PPSCTRL, the PPS output becomes a generated clock of following frequencies: 0001: The binary rollover is 2 Hz, and the digital

				rollover is 1 Hz. 0010: The binary rollover is 4 Hz, and the digital rollover is 2 Hz. 0011: The binary rollover is 8 Hz, and the digital rollover is 4 Hz. 0100: The binary rollover is 16 Hz, and the digital rollover is 8 Hz. .. 1111: The binary rollover is 32.768 KHz and the digital rollover is 16.384 KHz. Note: In the binary rollover mode, the PPS output (ptp_pps_o) has a duty cycle of 50 percent with these frequencies. In the digital rollover mode, the PPS output frequency is an average number. The actual clock is of different frequency that gets synchronized every second. For example: When PPSCTRL = 0001, the PPS (1 Hz) has a low period of 537 ms and a high period of 463 ms When PPSCTRL = 0010, the PPS (2 Hz) is a sequence of One clock of 50 percent duty cycle and 537 ms period Second clock of 463 ms period (268 ms low and 195 ms high) When PPSCTRL = 0011, the PPS (4 Hz) is a sequence of Three clocks of 50 percent duty cycle and 268 ms period Fourth clock of 195 ms period (134 ms low and 61 ms high)

				This behavior is because of the non-linear toggling of bits in the digital rollover mode in the MAC_System_Time_Nanoseconds register. or Flexible PPS Output (ptp_pps_o[0]) Control Programming these bits with a non-zero value instructs the MAC to initiate an event. When the command is transferred or synchronized to the PTP clock domain, these bits get cleared automatically. The software should ensure that these bits are programmed only when they are 'all-zero'. The following list describes the values of PPSCMD0: 0000: No Command 0001: START Single Pulse This command generates single pulse rising at the start point defined in MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds register and of a duration defined in the PPS0 Width Register. 0010: START Pulse Train This command generates the train of pulses rising at the start point defined in the Target Time Registers and of a duration defined in the PPS0 Width Register and repeated at interval defined in the PPS Interval Register. By default, the PPS pulse train is free-running unless stopped by the 'Stop Pulse train at time' or 'Stop Pulse Train immediately' commands. 0011: Cancel START This command cancels the START Single Pulse and START Pulse Train commands if the system time has not crossed the programmed start time. 0100: STOP Pulse train at time

				This command stops the train of pulses initiated by the START Pulse Train command (PPSCMD = 0010) after the time programmed in the Target Time registers elapses. 0101: STOP Pulse Train immediately This command immediately stops the train of pulses initiated by the START Pulse Train command (PPSCMD = 0010). 110: Cancel STOP Pulse train This command cancels the STOP pulse train at time command if the programmed stop time has not elapsed. The PPS pulse train becomes free-running on the successful execution of this command. 0111-1111: Reserved or Presentation Time Control If MCGREN0 is set then these bits are treated as Presentation time control bits. The following list describes the values of PPSCMD0: 0000: MCGR operation is not carried out. If set to this value in the mid of clock recovery or generation, all the processing inputs are flushed 0001: Capture the Presentation time at the rising edge of mcg_pst_trig_i[0] into the MAC_PPS0_Target_Time_Seconds register 0010: Capture the Presentation time at the falling edge of mcg_pst_trig_i[0] into the MAC_PPS0_Target_Time_Seconds register 0011: Capture the Presentation time at both edges of mcg_pst_trig_i[0] into the MAC_PPS0_Target_Time_Seconds register 0100-1000: Reserved

				1001: Toggle output on compare 1010: Pulse output low on compare for one PTP-clock cycle 1011: Pulse output high on compare for one PTP-clock cycle 1100-1111: Reserved Value After Reset: 0x0

2.3.125 EQOS_MAC_R_MAC_PPS(#I)_TARGET_TIME_SECONDS(FORI=0;I<=-1)

Access Type: RW

Address Offset: (0x0010*i)+0x0B80

Name	Access	Bit Range	Reset value	Description
TSTRH0	R/W	[31:0]	0x0	PPS Target Time Seconds Register This field stores the time in seconds. When the timestamp value matches or exceeds both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on Target Time mode selected for the corresponding PPS output in the MAC_PPS_Control register. If DWC_EQOS_FLEXI_PPS_OUT_EN is enabled in the configuration and PTGE field of MAC_Timestamp_Control Register is set with Presentation time control set in recovery mode, then these bits indicate the TPT being programmed by the application and in generation mode it indicates the CPT generated at the sampled trigger. Value After Reset: 0x0

2.3.126 EQOS_MAC_R_MAC_PPS(#I)_TARGET_TIME_NANOSECONDS(FORI=0;I<=-1)

Access Type: RW

Address Offset: (0x0010*i)+0x0B84

Name	Access	Bit Range	Reset value	Description
RESERVED	R	[31:31]	0x0	Reserved Field: Yes
TTSL0	R/W	[30:0]	0x0	

				Target Time Low for PPS Register This register stores the time in (signed) nanoseconds. When the value of the timestamp matches the value in both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on the TRGTMODSEL0 field (Bits [6:5]) in MAC_PPS_Control. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, this value should be (time in ns / 0.465). The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, this value should not exceed 0x3B9A_C9FF. The actual start or stop time of the PPS signal output might have an error margin up to one unit of sub-second increment value. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Value After Reset: 0x0

2.4 EQOS_MTL

Module Name	EQOS_MTL
Sub Module Name	
Data Width	32
Address Width	32
Base Address	0x0

2.4.1 EQOS_MTL_R_MTL_OPERATION_MODE

Access Type: RW

Address Offset: 0xc00

Name	Access	Bit Range	Reset value	Description
RESERVED_31_16	R	[31:16]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[15:15]	0x0	Reserved Field: Yes
RESERVED_14_10	R	[14:10]	0x0	Reserved. Value After Reset: 0x0
CNTCLR	R/W	[9:9]	0x0	

				Counters Reset When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. If this bit is set along with CNT_PRESET bit, CNT_PRESET has precedence. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.Values: 0x0 (DISABLE): Counters are not reset 0x1 (ENABLE): All counters are reset Value After Reset: 0x0 Testable: untestable
CNTPRST	R/W	[8:8]	0x0	Counters Preset When this bit is set, MTL_TxQ[0-7]_Underflow register is initialized/preset to 12'h7F0. Missed Packet and Overflow Packet counters in MTL_RxQ[0-7]_Missed_Packet_Overflow_Cnt register is initialized/preset to 12'h7F0. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.Values: 0x0 (DISABLE): Counters Preset is disabled 0x1 (ENABLE): Counters Preset is enabled Value After Reset: 0x0 Testable: untestable
RESERVED_7	R	[7:7]	0x0	Reserved. Value After Reset: 0x0
SCHALG	R/W	[6:5]	0x0	Tx Scheduling Algorithm This field indicates the algorithm for Tx scheduling:Values:

				0x0 (WRR): WRR algorithm 0x1 (WFQ): WFQ algorithm when DCB feature is selected.Otherwise, Reserved 0x2 (DWRR): DWRR algorithm when DCB feature is selected.Otherwise, Reserved 0x3 (SP): Strict priority algorithm Value After Reset: 0x0
RESERVED_4_3	R	[4:3]	0x0	Reserved. Value After Reset: 0x0
RAA	R/W	[2:2]	0x0	Receive Arbitration Algorithm This field is used to select the arbitration algorithm for the Rx side. 0: Strict priority (SP) Queue 0 has the lowest priority and the last queue has the highest priority. 1: Weighted Strict Priority (WSP) Values: 0x0 (SP): Strict priority (SP) 0x1 (WSP): Weighted Strict Priority (WSP) Value After Reset: 0x0
DTXSTS	R/W	[1:1]	0x0	Drop Transmit Status When this bit is set, the Tx packet status received from the MAC is dropped in the MTL. When this bit is reset, the Tx packet status received from the MAC is forwarded to the application.Values: 0x0 (DISABLE): Drop Transmit Status is disabled

				0x1 (ENABLE): Drop Transmit Status is enabled Value After Reset: 0x0
RESERVED_0	R	[0:0]	0x0	Reserved. Value After Reset: 0x0

2.4.2 EQOS_MTL_R_MTL_DBG_CTL

Access Type: RW

Address Offset: 0xc08

Name	Access	Bit Range	Reset value	Description
RESERVED_31_19	R	[31:19]	0x0	Reserved. Value After Reset: 0x0
EIEC	R/W	[18:17]	0x0	ECC Inject Error Control for Tx, Rx and TSO memories When EIEE bit of this register is set, following are the errors inserted based on the value encoded in this field.Values: 0x0 (M_1BIT): Insert 1 bit error 0x1 (M_2BIT): Insert 2 bit errors 0x2 (M_3BIT): Insert 3 bit errors 0x3 (M_1BIT_ADDR): Insert 1 bit error in address field Value After Reset: 0x0
EIEE	R/W	[16:16]	0x0	ECC Inject Error Enable for Tx, Rx and TSO memories When set, enables the ECC error injection feature. When reset, disables the ECC error injection feature.Values: 0x0 (DISABLE): ECC Inject Error for Tx, Rx and

				TSO memories is disabled 0x1 (ENABLE): ECC Inject Error for Tx, Rx and TSO memories is enabled Value After Reset: 0x0
STSIE	R/W	[15:15]	0x0	Transmit Status Available Interrupt Status Enable When this bit is set, an interrupt is generated when Transmit status is available in slave mode.Values: 0x0 (DISABLE): Transmit Packet Available Interrupt Status is disabled 0x1 (ENABLE): Transmit Packet Available Interrupt Status is enabled Value After Reset: 0x0
PKTIE	R/W	[14:14]	0x0	Receive Packet Available Interrupt Status Enable When this bit is set, an interrupt is generated when EOP of received packet is written to the Rx FIFO.Values: 0x0 (DISABLE): Receive Packet Available Interrupt Status is disabled 0x1 (ENABLE): Receive Packet Available Interrupt Status is enabled Value After Reset: 0x0
FIFOSEL	R/W	[13:12]	0x0	FIFO Selected for Access This field indicates the FIFO selected for debug access:Values: 0x0 (TXFIFO): Tx FIFO 0x1 (TXSTSFIFO): Tx Status FIFO (only read access when SLVMOD is set)

				0x2 (TSOFIFO): TSO FIFO (cannot be accessed when SLVMOD is set) 0x3 (RXFIFO): Rx FIFO Value After Reset: 0x0
FIFOWREN	R/W	[11:11]	0x0	FIFO Write Enable When this bit is set, it enables the Write operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets.Values: 0x0 (DISABLE): FIFO Write is disabled 0x1 (ENABLE): FIFO Write is enabled Value After Reset: 0x0 Testable: untestable
FIFORDEN	R/W	[10:10]	0x0	FIFO Read Enable When this bit is set, it enables the Read operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets.Values: 0x0 (DISABLE): FIFO Read is disabled 0x1 (ENABLE): FIFO Read is enabled Value After Reset: 0x0 Testable: untestable
RSTSEL	R/W	[9:9]	0x0	

				Reset Pointers of Selected FIFO When this bit is set, the pointers of the currently-selected FIFO are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets.Values: 0x0 (DISABLE): Reset Pointers of Selected FIFO is disabled 0x1 (ENABLE): Reset Pointers of Selected FIFO is enabled Value After Reset: 0x0 Testable: untestable
RSTALL	R/W	[8:8]	0x0	Reset All Pointers When this bit is set, the pointers of all FIFOs are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets.Values: 0x0 (DISABLE): Reset All Pointers is disabled 0x1 (ENABLE): Reset All Pointers is enabled Value After Reset: 0x0 Testable: untestable
RESERVED_7	R	[7:7]	0x0	Reserved. Value After Reset: 0x0
PKTSTATE	R/W	[6:5]	0x0	Encoded Packet State This field is used to write the control information to the Tx FIFO or Rx FIFO. Tx FIFO:

				00: Packet Data 01: Control Word 10: SOP Data 11: EOP Data Rx FIFO: 00: Packet Data 01: Normal Status 10: Last Status 11: EOP Values: 0x0 (PKT_DATA): Packet Data 0x1 (CW_NS): Control Word/Normal Status 0x2 (SOP_LS): SOP Data/Last Status 0x3 (EOP): EOP Data/EOP Value After Reset: 0x0
RESERVED_4	R	[4:4]	0x0	Reserved. Value After Reset: 0x0
BYTEEN	R/W	[3:2]	0x0	Byte Enables This field indicates the number of data bytes valid in the data register during Write operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected.Values: 0x0 (B0_VAL): Byte 0 valid 0x1 (B01_VAL): Byte 0 and Byte 1 are valid

				0x2 (B012_VAL): Byte 0, Byte 1, and Byte 2 are valid 0x3 (B0123_VAL): All four bytes are valid Value After Reset: 0x0
DBGMOD	R/W	[1:1]	0x0	Debug Mode Access to FIFO When this bit is set, it indicates that the current access to the FIFO is read, write, and debug access. In this mode, the following access types are allowed: Read and Write access to Tx FIFO, TSO FIFO, and Rx FIFO Read access is allowed to Tx Status FIFO. When this bit is reset, it indicates that the current access to the FIFO is slave access bypassing the DMA. In this mode, the following access are allowed: Write access to the Tx FIFO Read access to the Rx FIFO and Tx Status FIFO Values: 0x0 (DISABLE): Debug Mode Access to FIFO is disabled 0x1 (ENABLE): Debug Mode Access to FIFO is enabled Value After Reset: 0x0
FDBGEN	R/W	[0:0]	0x0	FIFO Debug Access Enable When this bit is set, it indicates that the debug mode access to the FIFO is enabled. When this bit is reset, it indicates that the FIFO can be accessed only through a master interface.Values:

				0x0 (DISABLE): FIFO Debug Access is disabled 0x1 (ENABLE): FIFO Debug Access is enabled Value After Reset: 0x0

2.4.3 EQOS_MTL_R_MTL_DBG_STS

Access Type: RW

Address Offset: 0xc0c

Name	Access	Bit Range	Reset value	Description
LOCR	R	[31:15]	0x0	Remaining Locations in the FIFO Slave Access Mode: This field indicates the space available in selected FIFO. Debug Access Mode: This field contains the Write or Read pointer value of the selected FIFO during Write or Read operation, respectively. Reset: In single Tx Queue configurations, (DWC_EQOS_TXFIFO_SIZE/(DWC_EQOS_DATAWIDTH/8)), Otherwise 0000H Value After Reset: 0x0
RESERVED_14_10	R	[14:10]	0x0	Reserved. Value After Reset: 0x0
STSI	R/W	[9:9]	0x0	Transmit Status Available Interrupt Status When set, this bit indicates that the Slave mode Tx packet is transmitted, and the status is available in Tx Status FIFO. This bit is reset when 1 is written to this bit.Values: 0x0 (INACTIVE): Transmit Status Available Interrupt Status not detected 0x1 (ACTIVE): Transmit Status Available Interrupt Status detected

				Value After Reset: 0x0 Testable: untestable
PKTI	R/W	[8:8]	0x0	Receive Packet Available Interrupt Status When set, this bit indicates that MAC layer has written the EOP of received packet to the Rx FIFO. This bit is reset when 1 is written to this bit.Values: 0x0 (INACTIVE): Receive Packet Available Interrupt Status not detected 0x1 (ACTIVE): Receive Packet Available Interrupt Status detected Value After Reset: 0x0 Testable: untestable
RESERVED_7_5	R	[7:5]	0x0	Reserved. Value After Reset: 0x0
BYTEEN	R	[4:3]	0x3	Byte Enables This field indicates the number of data bytes valid in the data register during Read operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected.Values: 0x0 (B0_VAL): Byte 0 valid 0x1 (B01_VAL): Byte 0 and Byte 1 are valid 0x2 (B012_VAL): Byte 0, Byte 1, and Byte 2 are valid 0x3 (B0123_VAL): All four bytes are valid Value After Reset: 0x3
PKTSTATE	R	[2:1]	0x0	Encoded Packet State This field is used to get the control or status information of the selected FIFO. Tx FIFO:

				00: Packet Data 01: Control Word 10: SOP Data 11: EOP Data Rx FIFO: 00: Packet Data 01: Normal Status 10: Last Status 11: EOP This field is applicable only for Tx FIFO and Rx FIFO during Read operation.Values: 0x0 (PKT_DATA): Packet Data 0x1 (CW_NS): Control Word/Normal Status 0x2 (SOP_LS): SOP Data/Last Status 0x3 (EOP): EOP Data/EOP Value After Reset: 0x0
FIFOBUSY	R	[0:0]	0x0	FIFO Busy When set, this bit indicates that a FIFO operation is in progress in the MAC and content of the following fields is not valid: All other fields of this register All fields of the MTL_FIFO_Debug_Data register Values:

				0x0 (INACTIVE): FIFO Busy not detected 0x1 (ACTIVE): FIFO Busy detected Value After Reset: 0x0

2.4.4 EQOS_MTL_R_MTL_FIFO_DEBUG_DATA

Access Type: RW

Address Offset: 0xc10

Name	Access	Bit Range	Reset value	Description
FDBGDATA	R/W	[31:0]	0x0	FIFO Debug Data During debug or slave access write operation, this field contains the data to be written to the Tx FIFO, Rx FIFO, or TSO FIFO. During debug or slave access read operation, this field contains the data read from the Tx FIFO, Rx FIFO, TSO FIFO, or Tx Status FIFO. Value After Reset: 0x0 Testable: untestable

2.4.5 EQOS_MTL_R_MTL_INTERRUPT_STATUS

Access Type: RW

Address Offset: 0xc20

Name	Access	Bit Range	Reset value	Description
RESERVED_31_24	R	[31:24]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[23:23]	0x0	Reserved Field: Yes
RESERVED_22_19	R	[22:19]	0x0	Reserved. Value After Reset: 0x0
ESTIS	R	[18:18]	0x0	EST (TAS- 802.1Qbv) Interrupt Status This bit indicates an interrupt event during the operation of 802.1Qbv. To reset this bit, the application must clear the error/event that has caused the Interrupt.Values: 0x0 (INACTIVE): EST (TAS- 802.1Qbv) Interrupt status not detected

				0x1 (ACTIVE): EST (TAS- 802.1Qbv) Interrupt status detected Value After Reset: 0x0
DBGIS	R	[17:17]	0x0	Debug Interrupt status This bit indicates an interrupt event during the slave access. To reset this bit, the application must read the FIFO Debug Access Status register to get the exact cause of the interrupt and clear its source.Values: 0x0 (INACTIVE): Debug Interrupt status not detected 0x1 (ACTIVE): Debug Interrupt status detected Value After Reset: 0x0
RESERVED	R	[16:16]	0x0	Reserved Field: Yes
RESERVED_15_8	R	[15:8]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[7:4]	0x0	Reserved Field: Yes
Q3IS	R	[3:3]	0x0	Queue 3 Interrupt status This bit indicates that there is an interrupt from Queue 3. To reset this bit, the application must read the MTL_Q3_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source.Values: 0x0 (INACTIVE): Queue 3 Interrupt status not detected 0x1 (ACTIVE): Queue 3 Interrupt status detected Value After Reset: 0x0
Q2IS	R	[2:2]	0x0	

				Queue 2 Interrupt status This bit indicates that there is an interrupt from Queue 2. To reset this bit, the application must read the MTL_Q2_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source.Values: 0x0 (INACTIVE): Queue 2 Interrupt status not detected 0x1 (ACTIVE): Queue 2 Interrupt status detected Value After Reset: 0x0
Q1IS	R	[1:1]	0x0	Queue 1 Interrupt status This bit indicates that there is an interrupt from Queue 1. To reset this bit, the application must read the MTL_Q1_Interrupt_Control_Status register to get the exact cause of the interrupt and clear its source.Values: 0x0 (INACTIVE): Queue 1 Interrupt status not detected 0x1 (ACTIVE): Queue 1 Interrupt status detected Value After Reset: 0x0
Q0IS	R	[0:0]	0x0	Queue 0 Interrupt status This bit indicates that there is an interrupt from Queue 0. To reset this bit, the application must read Queue 0 Interrupt Control and Status register to get the exact cause of the interrupt and clear its source.Values: 0x0 (INACTIVE): Queue 0 Interrupt status not detected 0x1 (ACTIVE): Queue 0 Interrupt status detected

				Value After Reset: 0x0

2.4.6 EQOS_MTL_R_MTL_RXQ_DMA_MAP0

Access Type: RW

Address Offset: 0xc30

Name	Access	Bit Range	Reset value	Description
RESERVED_31_29	R	[31:29]	0x0	Reserved. Value After Reset: 0x0
Q3DDMACH	R/W	[28:28]	0x0	Queue 3 Enabled for Dynamic (per packet) DMA Channel Selection When set, this bit indicates that the packets received in Queue 3 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 3 are routed to the DMA Channel programmed in the Q3MDMACH field (Bits[26:24]).Values: 0x0 (DISABLE): Queue 3 disabled for DA-based DMA Channel Selection 0x1 (ENABLE): Queue 3 enabled for DA-based DMA Channel Selection Value After Reset: 0x0
RESERVED_27_Y	R	[27:26]	0x0	Reserved. Value After Reset: 0x0
Q3MDMACH	R/W	[25:24]	0x0	Queue 3 Mapped to DMA Channel This field controls the routing of the received packet in Queue 3 to the DMA channel: 000: DMA Channel 0 001: DMA Channel 1

				010: DMA Channel 2 011: DMA Channel 3 100: DMA Channel 4 101: DMA Channel 5 110: DMA Channel 6 111: DMA Channel 7 This field is valid when the Q3DDMACH field is reset. Note: The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the others are reserved Value After Reset: 0x0
RESERVED_23_21	R	[23:21]	0x0	Reserved. Value After Reset: 0x0
Q2DDMACH	R/W	[20:20]	0x0	Queue 2 Enabled for DA-based DMA Channel Selection When set, this bit indicates that the packets received in Queue 2 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 2 are routed to the DMA Channel programmed in the Q2MDMACH field (Bits[18:16]).Values: 0x0 (DISABLE): Queue 2 disabled for DA-based DMA Channel Selection 0x1 (ENABLE): Queue 2 enabled for DA-based DMA Channel Selection

				Value After Reset: 0x0
RESERVED_19_Y	R	[19:18]	0x0	Reserved. Value After Reset: 0x0
Q2MDMACH	R/W	[17:16]	0x0	Queue 2 Mapped to DMA Channel This field controls the routing of the received packet in Queue 2 to the DMA channel: 000: DMA Channel 0 001: DMA Channel 1 010: DMA Channel 2 011: DMA Channel 3 100: DMA Channel 4 101: DMA Channel 5 110: DMA Channel 6 111: DMA Channel 7 This field is valid when the Q2DDMACH field is reset. Value After Reset: 0x0
RESERVED_15_13	R	[15:13]	0x0	Reserved. Value After Reset: 0x0
Q1DDMACH	R/W	[12:12]	0x0	Queue 1 Enabled for DA-based DMA Channel Selection When set, this bit indicates that the packets received in Queue 1 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 1 are routed to the DMA

				Channel programmed in the Q1MDMACH field (Bits[10:8]).Values: 0x0 (DISABLE): Queue 1 disabled for DA-based DMA Channel Selection 0x1 (ENABLE): Queue 1 enabled for DA-based DMA Channel Selection Value After Reset: 0x0
RESERVED_11_Y	R	[11:10]	0x0	Reserved. Value After Reset: 0x0
Q1MDMACH	R/W	[9:8]	0x0	Queue 1 Mapped to DMA Channel This field controls the routing of the received packet in Queue 1 to the DMA channel: 000: DMA Channel 0 001: DMA Channel 1 010: DMA Channel 2 011: DMA Channel 3 100: DMA Channel 4 101: DMA Channel 5 110: DMA Channel 6 111: DMA Channel 7 This field is valid when the Q1DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved. Value After Reset: 0x0

RESERVED_7_5	R	[7:5]	0x0	Reserved. Value After Reset: 0x0
Q0DDMACH	R/W	[4:4]	0x0	Queue 0 Enabled for DA-based DMA Channel Selection When set, this bit indicates that the packets received in Queue 0 are routed to a particular DMA channel as decided in the MAC Receiver based on the DMA channel number programmed in the L3-L4 filter registers, or the Ethernet DA address. When reset, this bit indicates that the packets received in Queue 0 are routed to the DMA Channel programmed in the Q0MDMACH field.Values: 0x0 (DISABLE): Queue 0 disabled for DA-based DMA Channel Selection 0x1 (ENABLE): Queue 0 enabled for DA-based DMA Channel Selection Value After Reset: 0x0
RESERVED_3_Y	R	[3:2]	0x0	Reserved. Value After Reset: 0x0
Q0MDMACH	R/W	[1:0]	0x0	Queue 0 Mapped to DMA Channel This field controls the routing of the packet received in Queue 0 to the DMA channel: 000: DMA Channel 0 001: DMA Channel 1 010: DMA Channel 2 011: DMA Channel 3 100: DMA Channel 4 101: DMA Channel 5

				110: DMA Channel 6 111: DMA Channel 7 This field is valid when the Q0DDMACH field is reset. The width of this field depends on the number of RX DMA channels and not all the values might be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the other bits are reserved. Value After Reset: 0x0

2.4.7 EQOS_MTL_R_MTL_TBS_CTRL

Access Type: RW

Address Offset: 0xc40

Name	Access	Bit Range	Reset value	Description
LEOS	R/W	[31:8]	0x0	Launch Expiry Offset The value in units of 256 nanoseconds that has to be added to the Launch time to compute the Launch Expiry time. Value valid only when LEOV is set. Max value: 999,999,999 ns, additionally should be smaller than CTR-1 value when ESTM mode is set since this value is a modulo CTR value. Value After Reset: 0x0
RESERVED_7	R	[7:7]	0x0	Reserved. Value After Reset: 0x0
LEGOS	R/W	[6:4]	0x0	Launch Expiry GSN Offset The number GSN slots that has to be added to the Launch GSN to compute the Launch Expiry time. Value valid only when LEOV is set. Value After Reset: 0x0
RESERVED_3_2	R	[3:2]	0x0	Reserved. Value After Reset: 0x0
LEOV	R/W	[1:1]	0x0	Launch Expiry Offset Valid When set indicates the LEOS field is valid. When not

				set, indicates the Launch Expiry Offset is not valid and the MTL must not check for Launch expiry time.Values: 0x0 (INVALID): LEOS field is invalid 0x1 (VALID): LEOS field is valid Value After Reset: 0x0
ESTM	R/W	[0:0]	0x0	EST offset Mode When this bit is set, the Launch Time value used in Time Based Scheduling is interpreted as an EST offset value and is added to the Base Time Register (BTR) of the current list. When reset, the Launch Time value is used as an absolute value that should be compared with the System time [39:8].Values: 0x0 (DISABLE): EST offset Mode is disabled 0x1 (ENABLE): EST offset Mode is enabled Value After Reset: 0x0

2.4.8 EQOS_MTL_R_MTL_EST_CONTROL

Access Type: RW

Address Offset: 0xc50

Name	Access	Bit Range	Reset value	Description
PTOV	R/W	[31:24]	0x0	PTP Time Offset Value The value of PTP Clock period multiplied by 6 in nanoseconds. This value is needed to avoid transmission overruns at the beginning of the installation of a new GCL. Value After Reset: 0x0
CTOV	R/W	[23:12]	0x0	Current Time Offset Value Provides a 12 bit time offset value in nano second that is added to the current time to compensate for all the

				implementation pipeline delays such as the CDC sync delay, buffering delays, data path delays etc. This offset helps to ensure that the impact of gate controls is visible on the line exactly at the pre-determined schedule (or as close to the schedule as possible). Value After Reset: 0x0
RESERVED_11	R	[11:11]	0x0	Reserved. Value After Reset: 0x0
TILS	R/W	[10:8]	0x0	Time Interval Left Shift Amount This field provides the left shift amount for the programmed Time Interval values used in the Gate Control Lists. 000: No left shift needed (equal to x1ns) 001: Left shift TI by 1 bit (equal to x2ns) 010: Left shift TI by 2 bits (equal to x4ns) . . 100: Left shift TI by 7 bits (equal to x128ns) Based on the configuration one or more bits of this field should be treated as Reserved/Read-Only. Value After Reset: 0x0
LCSE	R/W	[7:6]	0x0	Loop Count to report Scheduling Error Programmable number of GCL list iterations before reporting an HLBS error defined in EST_Status register.Values: 0x0 (M_4_ITERNS): 4 iterations 0x1 (M_8_ITERNS): 8 iterations 0x2 (M_16_ITERNS): 16 iterations 0x3 (M_32_ITERNS): 32 iterations

				Value After Reset: 0x0
DFBS	R/W	[5:5]	0x0	Drop Frames causing Scheduling Error When set frames reported to cause HOL Blocking due to not getting scheduled (HLBS field of EST_Status register) after 4,8,16,32 (based on LCSE field of this register) GCL iterations are dropped.Values: 0x0 (DONT_DROP): Do not Drop Frames causing Scheduling Error 0x1 (DROP): Drop Frames causing Scheduling Error Value After Reset: 0x0
DDBF	R/W	[4:4]	0x0	Do not Drop frames during Frame Size Error When set, frames are not be dropped during Head-of-Line blocking due to Frame Size Error (HLBF field of EST_Status register).Values: 0x0 (DROP): Drop frames during Frame Size Error 0x1 (DONT_DROP): Do not Drop frames during Frame Size Error Value After Reset: 0x0
RESERVED_2_3	R	[3:2]	0x0	Reserved. Value After Reset: 0x0
SSWL	R/W	[1:1]	0x0	Switch to S/W owned list When set indicates that the software has programmed that list that it currently owns (SWOL) and the hardware should switch to the new list based on the new BTR. Hardware clears this bit when the switch to the SWOL happens to indicate the completion of the switch or when an BTR error (BTRE in Status register) is set. When BTRE is set this bit is cleared

				but SWOL is not updated as the switch was not successful. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.Values: 0x0 (DISABLE): Switch to S/W owned list is disabled 0x1 (ENABLE): Switch to S/W owned list is enabled Value After Reset: 0x0
EEST	R/W	[0:0]	0x0	Enable EST When reset, the gate control list processing is halted and all gates are assumed to be in Open state. Should be set for the hardware to start processing the gate control lists. During the toggle from 0 to 1, the gate control list processing starts only after the SSWL bit it set. When DWC_EQOS_ASP_ECC is selected during the configuration, if any uncorrectable error is detected in the EST memory the hardware resets this bit and disables the EST function.Values: 0x0 (DISABLE): EST is disabled 0x1 (ENABLE): EST is enabled Value After Reset: 0x0

2.4.9 EQOS_MTL_R_MTL_EST_STATUS

Access Type: RW

Address Offset: 0xc58

Name	Access	Bit Range	Reset value	Description
RESERVED_31_20	R	[31:20]	0x0	Reserved. Value After Reset: 0x0
CGSN	R	[19:16]	0x0	Current GCL Slot Number Indicates the slot number of the GCL list. Slot

				number is a modulo 16 count of the GCL List loops executed so far. Even if a new GCL list is installed, the count is incremental. Value After Reset: 0x0
RESERVED_15_12	R	[15:12]	0x0	Reserved. Value After Reset: 0x0
BTRL	R	[11:8]	0x0	BTR Error Loop Count Provides the minimum count (N) for which the equation Current Time =< New BTR + (N * New Cycle Time) becomes true. N = "1111" indicates the iterations exceeded the value of 8 and the hardware was not able to update New BTR to be equal to or greater than Current Time. Software intervention is needed to update the New BTR. Value cleared when BTRE field of this register is cleared. Value After Reset: 0x0
SWOL	R	[7:7]	0x0	S/W owned list When '0' indicates Gate control list number "0" is owned by software and when "1" indicates the Gate Control list "1" is owned by the software. Any reads/writes by the software (using indirect access via GCL_Control) is directed to the list indicated by this value by default. The inverse of this value is treated as HWOL. R/W operations performed by hardware are directed to the list pointed by HWOL by default.Values: 0x0 (INACTIVE): Gate control list number "0" is owned by software 0x1 (ACTIVE): Gate control list number "1" is owned by software Value After Reset: 0x0
RESERVED_6_5	R	[6:5]	0x0	Reserved. Value After Reset: 0x0

CGCE	R/W	[4:4]	0x0	Constant Gate Control Error This error occurs when the list length (LLR) is 1 and the Cycle Time (CTR) is less than or equal to the programmed Time Interval (TI) value after the optional Left Shifting. The above programming implies Gates are either always Closed or always Open based on the Gate Control values; the same effect can be achieved by other simpler (non TSN) programming mechanisms. Since the implementation does not support such a programming an error is reported. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.Values: 0x0 (INACTIVE): Constant Gate Control Error not detected 0x1 (ACTIVE): Constant Gate Control Error detected Value After Reset: 0x0
HLBS	R	[3:3]	0x0	Head-Of-Line Blocking due to Scheduling Set when the frame is not able to win arbitration and get scheduled even after 4 iterations of the GCL. Indicates to software a potential programming error. The one hot encoded values of the Queue Numbers that are not able to make progress are indicated in the MTL_EST_Sch_Error register. Bit cleared when MTL_EST_Sch_Error register is all zeros.Values: 0x0 (INACTIVE): Head-Of-Line Blocking due to Scheduling not detected 0x1 (ACTIVE): Head-Of-Line Blocking due to Scheduling detected Value After Reset: 0x0
HLBF	R	[2:2]	0x0	

				Head-Of-Line Blocking due to Frame Size Set when HOL Blocking is noticed on one or more Queues as a result of none of the Time Intervals of gate open in the GCL being greater than or equal to the duration needed for frame size (or frame fragment size when preemption is enabled) transmission. The one hot encoded Queue numbers that are experiencing HLBF are indicated in the MTL_EST_Frm_Size_Error register. Additionally, the first Queue number that experienced HLBF along with the frame size is captured in MTL_EST_Frm_Size_Capture register. Bit cleared when MTL_EST_Frame_Size_ Error register is all zeros.Values: 0x0 (INACTIVE): Head-Of-Line Blocking due to Frame Size not detected 0x1 (ACTIVE): Head-Of-Line Blocking due to Frame Size detected Value After Reset: 0x0
BTRE	R/W	[1:1]	0x0	BTR Error When "1" indicates a programming error in the BTR of SWOL where the programmed value is less than current time. If the BTRL = "1111", SWOL is not updated and Software should reprogram the BTR to a value greater than current time and then set SSWL to reinitiate the switch to SWOL. Else if the value of BTRL < "1111", SWOL is updated and this field indicates the number of iterations (of + CycleTime) taken by hardware to update the BTR to a value greater than Current Time. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.Values: 0x0 (INACTIVE): BTR Error not detected 0x1 (ACTIVE): BTR Error detected

				Value After Reset: 0x0
SWLC	R/W	[0:0]	0x0	Switch to S/W owned list Complete When "1" indicates the hardware has successfully switched to the SWOL, and the SWOL bit has been updated to that effect. Cleared when the SSWL of EST_Control register transitions from 0 to 1, or on a software write. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.Values: 0x0 (INACTIVE): Switch to S/W owned list Complete not detected 0x1 (ACTIVE): Switch to S/W owned list Complete detected Value After Reset: 0x0

2.4.10 EQOS_MTL_R_MTL_EST_SCH_ERROR

Access Type: RW

Address Offset: 0xc60

Name	Access	Bit Range	Reset value	Description
RESERVED_31_X	R	[31:4]	0x0	Reserved. Value After Reset: 0x0
SEQN	R/W	[3:0]	0x0	Schedule Error Queue Number The One Hot Encoded Queue Numbers that have experienced error/timeout described in HLBS field of status register. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. Value After Reset: 0x0

2.4.11 EQOS_MTL_R_MTL_EST_FRM_SIZE_ERROR

Access Type: RW

Address Offset: 0xc64

Name	Access	Bit Range	Reset value	Description

RESERVED_31_X	R	[31:4]	0x0	Reserved. Value After Reset: 0x0
FEQN	R/W	[3:0]	0x0	Frame Size Error Queue Number The One Hot Encoded Queue Numbers that have experienced error described in HLBF field of status register. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. Value After Reset: 0x0

2.4.12 EQOS_MTL_R_MTL_EST_FRM_SIZE_CAPTURE

Access Type: RW

Address Offset: 0xc68

Name	Access	Bit Range	Reset value	Description
RESERVED_31_X	R	[31:18]	0x0	Reserved. Value After Reset: 0x0
HBFQ	R	[17:16]	0x0	Queue Number of HLBF Captures the binary value of the of the first Queue (number) experiencing HLBF error (see HLBF field of status register). Value once written is not altered by any subsequent queue errors of similar nature. Once cleared the queue number of the next occurring HLBF error is captured. Width is based on the number of Tx Queues configured; remaining bits are Read-Only. Cleared when MTL_EST_Frm_Size_Error register is all zeros. Value After Reset: 0x0
RESERVED_15	R	[15:15]	0x0	Reserved. Value After Reset: 0x0
HBFS	R	[14:0]	0x0	Frame Size of HLBF Captures the Frame Size of the dropped frame related to queue number indicated in HBFQ field of this register. Contents of this register should be considered invalid, if this field is zero. Cleared when MTL_EST_Frm_Size_Error register

				is all zeros. Value After Reset: 0x0

2.4.13 EQOS_MTL_R_MTL_EST_INTR_ENABLE

Access Type: RW

Address Offset: 0xc70

Name	Access	Bit Range	Reset value	Description
RESERVED_31_5	R	[31:5]	0x0	Reserved. Value After Reset: 0x0
CGCE	R/W	[4:4]	0x0	Interrupt Enable for CGCE When set, generates interrupt when the Constant Gate Control Error occurs and is indicated in the status. When reset this event does not generate an interruptValues: 0x0 (DISABLE): Interrupt for CGCE is disabled 0x1 (ENABLE): Interrupt for CGCE is enabled Value After Reset: 0x0
IEHS	R/W	[3:3]	0x0	Interrupt Enable for HLBS When set, generates interrupt when the Head-of-Line Blocking due to Scheduling issue and is indicated in the status. When reset this event does not generate an interrupt.Values: 0x0 (DISABLE): Interrupt for HLBS is disabled 0x1 (ENABLE): Interrupt for HLBS is enabled Value After Reset: 0x0
IEHF	R/W	[2:2]	0x0	Interrupt Enable for HLBF When set, generates interrupt when the Head-of-Line Blocking due to Frame Size error occurs and is indicated in the status. When reset this event does not generate an interrupt.Values:

				0x0 (DISABLE): Interrupt for HLBF is disabled 0x1 (ENABLE): Interrupt for HLBF is enabled Value After Reset: 0x0
IEBE	R/W	[1:1]	0x0	Interrupt Enable for BTR Error When set, generates interrupt when the BTR Error occurs and is indicated in the status. When reset this event does not generate an interrupt.Values: 0x0 (DISABLE): Interrupt for BTR Error is disabled 0x1 (ENABLE): Interrupt for BTR Error is enabled Value After Reset: 0x0
IECC	R/W	[0:0]	0x0	Interrupt Enable for Switch List When set, generates interrupt when the configuration change is successful and the hardware has switched to the new list. When reset this event does not generate an interrupt.Values: 0x0 (DISABLE): Interrupt for Switch List is disabled 0x1 (ENABLE): Interrupt for Switch List is enabled Value After Reset: 0x0

2.4.14 EQOS_MTL_R_MTL_EST_GCL_CONTROL

Access Type: RW

Address Offset: 0xc80

Name	Access	Bit Range	Reset value	Description
RESERVED_31_24	R	[31:24]	0x0	Reserved. Value After Reset: 0x0
ESTEIEC	R/W	[23:22]	0x0	

				ECC Inject Error Control for EST Memory When EIEE bit of this register is set, following are the errors inserted based on the value encoded in this field. This field is valid only if DWC_EQOS_ASP_ECC feature is selected during the configuration, else it is reserved.Values: 0x0 (M_1BIT): Insert 1 bit error 0x1 (M_2BIT): Insert 2 bit errors 0x2 (M_3BIT): Insert 3 bit errors 0x3 (M_1BIT_ADDR): Insert 1 bit error in address field Value After Reset: 0x0
ESTEIEE	R/W	[21:21]	0x0	EST ECC Inject Error Enable When set along with EEST bit of MTL_EST_Control register, enables the ECC error injection feature. When reset, disables the ECC error injection feature.Values: 0x0 (DISABLE): EST ECC Inject Error is disabled 0x1 (ENABLE): EST ECC Inject Error is enabled Value After Reset: 0x0
ERR0	R/W	[20:20]	0x0	When set indicates the last write operation was aborted as software writes to GCL and GCL registers is prohibited when SSWL bit of MTL_EST_Control Register is set. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.Values:

				0x0 (DISABLE): ERR0 is disabled 0x1 (ENABLE): ERR1 is enabled Value After Reset: 0x0
RESERVED_19_Y	R	[19:16]	0x0	Reserved. Value After Reset: 0x0
ADDR	R/W	[15:8]	0x0	Gate Control List Address: (GCLA when GCRR is "0"). Provides the address (row number) of the Gate Control List at which the R/W operation has to be performed. By default the Gate Control List pointed by SWOL of MTL_EST_Status is selected for R/W, however if the DBGM bit of this register is set, a debug mode access is given to R/W from DBGB. The width of this field is dependent on DWC_EQOS_EST_DEP; unused bits should be treated as read only. Gate Control list Related Registers Address: (GCRA when GCRR is "1"). By default the GCL related register set pointed by SWOL of MTL_EST_Status is selected for R/W, however if the DBGM bit of this register is set, a debug mode access is given to R/W from DBGB. Lower 3 bits are only used in this mode, higher order bits are treated as dont cares. 000: BTR Low (31:0) 001: BTR High (63:31) 010: CTR Low (31:0) 011: CTR High (39:32) 100: TER (31:0) 101: LLR (n:0) (where n is (log{DWC_EQOS_EST_DEP} / log2))

				Others: Reserved Value After Reset: 0x0
RESERVED_7_6	R/W	[7:6]	0x0	Reserved. Value After Reset: 0x0
DBGB	R/W	[5:5]	0x0	Debug Mode Bank Select When set to "0" indicates R/W in debug mode should be directed to Bank 0 (GCL0 and corresponding Time related registers). When set to "1" indicates R/W in debug mode should be directed to Bank 1 (GCL1 and corresponding Time related registers). This value is used when DBGM is set and overrides by value of SWOL which is normally used.Values: 0x0 (BANK0): R/W in debug mode should be directed to Bank 0 0x1 (BANK1): R/W in debug mode should be directed to Bank 1 Value After Reset: 0x0
DBGM	R/W	[4:4]	0x0	Debug Mode When set to "1" indicates R/W in debug mode where the memory bank (for GCL and Time related registers) is explicitly provided by DBGB value, when set to "0" SWOL bit is used to determine which bank to use.Values: 0x0 (DISABLE): Debug Mode is disabled 0x1 (ENABLE): Debug Mode is enabled Value After Reset: 0x0
RESERVED_3	R/W	[3:3]	0x0	Reserved. Value After Reset: 0x0

GCRR	R/W	[2:2]	0x0	Gate Control Related Registers When set to "1" indicates the R/W access is for the GCL related registers (BTR, CTR, TER, LLR) whose address is provided by GCRA. When "0" indicates R/W should be directed to GCL from the address provided by GCLA.Values: 0x0 (DISABLE): Gate Control Related Registers are disabled 0x1 (ENABLE): Gate Control Related Registers are enabled Value After Reset: 0x0
R1W0	R/W	[1:1]	0x0	Read '1', Write '0': When set to '1': Read Operation When set to '0': Write Operation.Values: 0x0 (WRITE): Write Operation 0x1 (READ): Read Operation Value After Reset: 0x0
SRWO	R/W	[0:0]	0x0	Start Read/Write Op When set indicates a Read/Write Op has started and is in progress. When reset by hardware indicates the R/W Op has completed or an error has occurred (when bit 20 is set) Reads: Data can be read from MTL_EST_GCL_Data register after this bit is reset Writes: MTL_EST_GCL_Data should be programmed with write data before setting SRWO. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.Values: 0x0 (DISABLE): Start Read/Write Op disabled

				0x1 (ENABLE): Start Read/Write Op enabled Value After Reset: 0x0

2.4.15 EQOS_MTL_R_MTL_EST_GCL_DATA

Access Type: RW

Address Offset: 0xc84

Name	Access	Bit Range	Reset value	Description
GCD	R/W	[31:0]	0x0	Gate Control Data The data corresponding to the address selected in the GCL_Control register. Used for both Read and Write operations. Value After Reset: 0x0

2.4.16 EQOS_MTL_R_MTL_FPE_CTRL_STS

Access Type: RW

Address Offset: 0xc90

Name	Access	Bit Range	Reset value	Description
RESERVED_31_29	R	[31:29]	0x0	Reserved. Value After Reset: 0x0
HRS	R	[28:28]	0x0	Hold/Release Status 1: Indicates a Set-and-Hold-MAC operation was last executed and the pMAC is in Hold State. 0: Indicates a Set-and-Release-MAC operation was last executed and the pMAC is in Release State. Values: 0x0 (SET_REL): Indicates a Set-and-Release-MAC operation was last executed and the pMAC is in Release State 0x1 (SET_HOLD): Indicates a Set-and-Hold-MAC operation was last executed and the pMAC is in Hold State

				Value After Reset: 0x0
RESERVED_27_16	R	[27:16]	0x0	Reserved. Value After Reset: 0x0
RESERVED_15_Y	R	[15:12]	0x0	Reserved. Value After Reset: 0x0
PEC	R/W	[11:8]	0x0	Preemption Classification When set indicates the corresponding Queue must be classified as preemptable, when '0' Queue is classified as express. When both EST (Qbv) and Preemption are enabled, Queue-0 is always assumed to be preemptable. When EST (Qbv) is enabled Queues categorized as preemptable here are always assumed to be in "Open" state in the Gate Control List. Value After Reset: 0x0
RESERVED_7_2	R	[7:2]	0x0	Reserved. Value After Reset: 0x0
AFSZ	R/W	[1:0]	0x0	Additional Fragment Size used to indicate, in units of 64 bytes, the minimum number of bytes over 64 bytes required in non-final fragments of preempted frames. The minimum non-final fragment size is (AFSZ +1) * 64 bytes Value After Reset: 0x0

2.4.17 EQOS_MTL_R_MTL_FPE_ADVANCE

Access Type: RW

Address Offset: 0xc94

Name	Access	Bit Range	Reset value	Description
RADV	R/W	[31:16]	0x0	Release Advance The maximum time in nanoseconds that can elapse between issuing a RELEASE to the MAC and the MAC being ready to resume transmission of preemptable frames, in the absence of there being any express frames available for transmission. Value After Reset: 0x0
HADV	R/W	[15:0]	0x0	

				Hold Advance The maximum time in nanoseconds that can elapse between issuing a HOLD to the MAC and the MAC ceasing to transmit any preemptable frame that is in the process of transmission or any preemptable frames that are queued for transmission. Value After Reset: 0x0

2.4.18 EQOS_MTL_R_MTL_ECC_CONTROL

Access Type: RW

Address Offset: 0xcc0

Name	Access	Bit Range	Reset value	Description
RESERVED_31_9	R	[31:9]	0x0	Reserved. Value After Reset: 0x0
MEEAO	R/W	[8:8]	0x0	MTL ECC Error Address Status Over-ride When set, the following error address fields hold the last valid address where the error is detected. When reset, the following error address fields hold the first address where the error is detected. EUEAS/ECEAS of MTL_ECC_Err_Addr_Status register.Values: 0x0 (DISABLE): MTL ECC Error Address Status Over-ride is disabled 0x1 (ENABLE): MTL ECC Error Address Status Over-ride is enabled Value After Reset: 0x0
RESERVED_7_5	R	[7:5]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[4:3]	0x0	Reserved Field: Yes
MESTEE	R/W	[2:2]	0x0	MTL EST ECC Enable When set to 1, enables the ECC feature for EST memory. When set to zero, disables the ECC feature for EST memory.Values:

				0x0 (DISABLE): MTL EST ECC is disabled 0x1 (ENABLE): MTL EST ECC is enabled Value After Reset: 0x0
MRXEE	R/W	[1:1]	0x0	MTL Rx FIFO ECC Enable When set to 1, enables the ECC feature for MTL Rx FIFO memory. When set to zero, disables the ECC feature for MTL Rx FIFO memory.Values: 0x0 (DISABLE): MTL Rx FIFO ECC is disabled 0x1 (ENABLE): MTL Rx FIFO ECC is enabled Value After Reset: 0x0
MTXEE	R/W	[0:0]	0x0	MTL Tx FIFO ECC Enable When set to 1, enables the ECC feature for MTL Tx FIFO memory. When set to zero, disables the ECC feature for MTL Tx FIFO memory.Values: 0x0 (DISABLE): MTL Tx FIFO ECC is disabled 0x1 (ENABLE): MTL Tx FIFO ECC is enabled Value After Reset: 0x0

2.4.19 EQOS_MTL_R_MTL_SAFETY_INTERRUPT_STATUS

Access Type: RW

Address Offset: 0xcc4

Name	Access	Bit Range	Reset value	Description
RESERVED	R	[31:31]	0x0	Reserved Field: Yes
RESERVED_30_2	R	[30:2]	0x0	Reserved. Value After Reset: 0x0
MEUIS	R	[1:1]	0x0	MTL ECC Uncorrectable error Interrupt Status

				This bit indicates that an uncorrectable error interrupt event in the MTL ECC safety feature. To get the exact cause of the interrupt the application should read the MTL_ECC_Interrupt_Status register.Values: 0x0 (INACTIVE): MTL ECC Uncorrectable error Interrupt Status not detected 0x1 (ACTIVE): MTL ECC Uncorrectable error Interrupt Status detected Value After Reset: 0x0
MECIS	R	[0:0]	0x0	MTL ECC Correctable error Interrupt Status This bit indicates that a correctable error interrupt event in the MTL ECC safety feature. To get the exact cause of the interrupt the application should read the MTL_ECC_Interrupt_Status register.Values: 0x0 (INACTIVE): MTL ECC Correctable error Interrupt Status not detected 0x1 (ACTIVE): MTL ECC Correctable error Interrupt Status detected Value After Reset: 0x0

2.4.20 EQOS_MTL_R_MTL_ECC_INTERRUPT_ENABLE

Access Type: RW

Address Offset: 0xcc8

Name	Access	Bit Range	Reset value	Description
RESERVED_31_13	R	[31:13]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[12:12]	0x0	Reserved Field: Yes
RESERVED_11_9	R	[11:9]	0x0	Reserved. Value After Reset: 0x0

ECEIE	R/W	[8:8]	0x0	EST memory Correctable Error Interrupt Enable When set, generates an interrupt when a correctable error is detected at the MTL EST memory interface. It is indicated in the ECES bit of MTL_ECC_Interrupt_Status register. When reset this event does not generates an interrupt.Values: 0x0 (DISABLE): EST memory Correctable Error Interrupt is disabled 0x1 (ENABLE): EST memory Correctable Error Interrupt is enabled Value After Reset: 0x0
RESERVED_7_5	R	[7:5]	0x0	Reserved. Value After Reset: 0x0
RXCEIE	R/W	[4:4]	0x0	Rx memory Correctable Error Interrupt Enable When set, generates an interrupt when a correctable error is detected at the MTL Rx memory interface. It is indicated in the RXCES bit of MTL_ECC_Interrupt_Status register. When reset this event does not generates an interrupt.Values: 0x0 (DISABLE): Rx memory Correctable Error Interrupt is disabled 0x1 (ENABLE): Rx memory Correctable Error Interrupt is enabled Value After Reset: 0x0
RESERVED_3_1	R	[3:1]	0x0	Reserved. Value After Reset: 0x0
TXCEIE	R/W	[0:0]	0x0	Tx memory Correctable Error Interrupt Enable When set, generates an interrupt when a correctable

				error is detected at the MTL Tx memory interface. It is indicated in the TXCES bit of MTL_ECC_Interrupt_Status register. When reset this event does not generates an interrupt.Values: 0x0 (DISABLE): Tx memory Correctable Error Interrupt is disabled 0x1 (ENABLE): Tx memory Correctable Error Interrupt is enabled Value After Reset: 0x0

2.4.21 EQOS_MTL_R_MTL_ECC_INTERRUPT_STATUS

Access Type: RW

Address Offset: 0xccc

Name	Access	Bit Range	Reset value	Description
RESERVED_31_15	R	[31:15]	0x0	Reserved. Value After Reset: 0x0
RESERVED	R	[14:12]	0x0	Reserved Field: Yes
RESERVED_11	R	[11:11]	0x0	Reserved. Value After Reset: 0x0
EUES	R/W	[10:10]	0x0	MTL EST memory Uncorrectable Error Status When set, indicates that an uncorrectable error is detected at MTL EST memory interface.Values: 0x0 (INACTIVE): MTL EST memory Uncorrectable Error Status not detected 0x1 (ACTIVE): MTL EST memory Uncorrectable Error Status detected Value After Reset: 0x0 Testable: untestable
EAMS	R/W	[9:9]	0x0	MTL EST memory Address Mismatch Status

				This bit when set indicates that address mismatch is found for address bus of MTL EST memory.Values: 0x0 (INACTIVE): MTL EST memory Address Mismatch Status not detected 0x1 (ACTIVE): MTL EST memory Address Mismatch Status detected Value After Reset: 0x0 Testable: untestable
ECES	R/W	[8:8]	0x0	MTL EST memory Correctable Error Status This bit when set indicates that correctable error is detected at the MTL EST memory.Values: 0x0 (INACTIVE): MTL EST memory Correctable Error Status not detected 0x1 (ACTIVE): MTL EST memory Correctable Error Status detected Value After Reset: 0x0 Testable: untestable
RESERVED_7	R	[7:7]	0x0	Reserved. Value After Reset: 0x0
RXUES	R/W	[6:6]	0x0	MTL Rx memory Uncorrectable Error Status When set, indicates that an uncorrectable error is detected at the MTL Rx memory interface.Values: 0x0 (INACTIVE): MTL Rx memory Uncorrectable Error Status not detected 0x1 (ACTIVE): MTL Rx memory Uncorrectable Error Status detected Value After Reset: 0x0

				Testable: untestable
RXAMS	R/W	[5:5]	0x0	MTL Rx memory Address Mismatch Status This bit when set indicates that address mismatch is found for address bus of the MTL Rx memory.Values: 0x0 (INACTIVE): MTL Rx memory Address Mismatch Status not detected 0x1 (ACTIVE): MTL Rx memory Address Mismatch Status detected Value After Reset: 0x0 Testable: untestable
RXCES	R/W	[4:4]	0x0	MTL Rx memory Correctable Error Status This bit when set indicates that correctable error is detected at the MTL Rx memory.Values: 0x0 (INACTIVE): MTL Rx memory correctable Error Status not detected 0x1 (ACTIVE): MTL Rx memory correctable Error Status detected Value After Reset: 0x0 Testable: untestable
RESERVED_3	R	[3:3]	0x0	Reserved. Value After Reset: 0x0
TXUES	R/W	[2:2]	0x0	MTL Tx memory Uncorrectable Error Status When set, indicates that an uncorrectable error is detected at the MTL TX memory interface.Values: 0x0 (INACTIVE): MTL Tx memory Uncorrectable Error Status not detected 0x1 (ACTIVE): MTL Tx memory Uncorrectable

				Error Status detected Value After Reset: 0x0 Testable: untestable
TXAMS	R/W	[1:1]	0x0	MTL Tx memory Address Mismatch Status This bit when set indicates that address mismatch is found for address bus of the MTL Tx memory.Values: 0x0 (INACTIVE): MTL Tx memory Address Mismatch Status not detected 0x1 (ACTIVE): MTL Tx memory Address Mismatch Status detected Value After Reset: 0x0 Testable: untestable
TXCES	R/W	[0:0]	0x0	MTL Tx memory Correctable Error Status This bit when set indicates that a correctable error is detected at the MTL Tx memory.Values: 0x0 (INACTIVE): MTL Tx memory Correctable Error Status not detected 0x1 (ACTIVE): MTL Tx memory Correctable Error Status detected Value After Reset: 0x0 Testable: untestable

2.4.22 EQOS_MTL_R_MTL_ECC_ERR_STS_RCTL

Access Type: RW

Address Offset: 0xcd0

Name	Access	Bit Range	Reset value	Description
RESERVED_31_6	R	[31:6]	0x0	Reserved. Value After Reset: 0x0

CUES	R/W	[5:5]	0x0	Clear Uncorrectable Error Status When this bit is set along with EESRE bit of this register, based on the EMS field of this register, the respective memory's uncorrectable error address and uncorrectable error count values are cleared upon reading. Hardware resets this bit when all the error status values are cleared.Values: 0x0 (INACTIVE): Clear Uncorrectable Error Status not detected 0x1 (ACTIVE): Clear Uncorrectable Error Status detected Value After Reset: 0x0 Testable: untestable
CCES	R/W	[4:4]	0x0	Clear Correctable Error Status When this bit is set along with EESRE bit of this register, based on the EMS field of this register, the respective memory's correctable error address and correctable error count values are cleared upon reading. Hardware resets this bit when all the error status values are cleared.Values: 0x0 (INACTIVE): Clear Correctable Error Status not detected 0x1 (ACTIVE): Clear Correctable Error Status detected Value After Reset: 0x0 Testable: untestable
EMS	R/W	[3:1]	0x0	MTL ECC Memory Selection When EESRE bit of this register is set, this field

				indicates which memory's error status value to be read. The memory selection encoding is as described below.Values: 0x0 (TX_MEM): MTL Tx memory 0x1 (RX_MEM): MTL Rx memory 0x2 (EST_MEM): MTL EST memory 0x3 (RXP_MEM): MTL Rx Parser memory 0x4 (TSO_MEM): DMA TSO memory Value After Reset: 0x0
EESRE	R/W	[0:0]	0x0	MTL ECC Error Status Read Enable When this bit is set, based on the EMS field of this register, the respective memory's error status values are captured as described: The correctable and uncorrectable error count values are captured into MTL_ECC_Err_Cnt_Status register The address location's of correctable and uncorrectable errors are captured into MTL_ECC_Err_Addr_Status register. Hardware resets this bit when all the status values are captured into the MTL_ECC_Err_Cnt_Status and MTL_ECC_Err_Addr_Status registers.Values: 0x0 (DISABLE): MTL ECC Error Status Read is disabled 0x1 (ENABLE): MTL ECC Error Status Read is enabled Value After Reset: 0x0 Testable: untestable

2.4.23 EQOS_MTL_R_MTL_ECC_ERR_ADDR_STATUS

Access Type: RW

Address Offset: 0xcd4

Name	Access	Bit Range	Reset value	Description
EUEAS	R	[31:16]	0x0	MTL ECC Uncorrectable Error Address Status Based on the EMS field of MTL_ECC_Err_Sts_Rctl register, this field holds the respective memory's address locations for which an uncorrectable error or address mismatch is detected. When MEEAO bit of MTL_ECC_Control register is set, this field holds the last valid address of memory for which either an uncorrectable error or an address mismatch is detected. When MEEAO bit of MTL_ECC_Control register is reset, this field holds the first address of the memory for which either an uncorrectable error or address mismatch is detected. Value After Reset: 0x0
ECEAS	R	[15:0]	0x0	MTL ECC Correctable Error Address Status Based on the EMS field of MTL_ECC_Err_Sts_Rctl register, this field holds the respective memory's address locations for which a correctable error is detected. When MEEAO bit of MTL_ECC_Control register is set, this field holds the last valid address of memory for which correctable error or address mismatch is detected. When MEEAO bit of MTL_ECC_Control register is reset, this field holds the first address of the memory for which correctable error is detected. Value After Reset: 0x0

2.4.24 EQOS_MTL_R_MTL_ECC_ERR_CNTR_STATUS

Access Type: RW

Address Offset: 0xcd8

Name	Access	Bit Range	Reset value	Description
RESERVED_31_20	R	[31:20]	0x0	Reserved. Value After Reset: 0x0
EUECS	R	[19:16]	0x0	MTL ECC Uncorrectable Error Counter Status Based on the EMS field of MTL_ECC_Err_Cntr_Rctl register, this field holds

				the respective memory's uncorrectable error count value. Value After Reset: 0x0
RESERVED_15_8	R	[15:8]	0x0	Reserved. Value After Reset: 0x0
ECECS	R	[7:0]	0x0	MTL ECC Correctable Error Counter Status Based on the EMS field of MTL_ECC_Err_Cntr_Rctl register, this field holds the respective memory's correctable error count value. Value After Reset: 0x0

2.4.25 EQOS_MTL_R_MTL_DPP_CONTROL

Access Type: RW

Address Offset: 0xce0

Name	Access	Bit Range	Reset value	Description
RESERVED_31_14	R	[31:14]	0x0	Reserved. Value After Reset: 0x0
IPECW	R/W	[13:13]	0x0	Insert Parity error in CSR Read data parity generator When set to 1, parity bit of first valid data generated by the CSR parity generator (or at PG10 as shown in AXI slave Interface Data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped.Values: 0x0 (DISABLE): Insert Parity error in CSR Read data parity generator is disabled 0x1 (ENABLE): Insert Parity error in CSR Read data parity generator is enabled Value After Reset: 0x0 Testable: untestable
RESERVED	R	[12:12]	0x0	Reserved Field: Yes

IPERD	R/W	[11:11]	0x0	Insert Parity error in Rx write-back Descriptor parity generator When set to 1, parity bit of first valid data generated by the DMA Rx write-back descriptor parity generator(or at PG8 as shown in Receive data path parity protection diagram) is flipped.Values: 0x0 (DISABLE): Insert Parity error in Rx write-back Descriptor parity generator is disabled 0x1 (ENABLE): Insert Parity error in Rx write-back Descriptor parity generator is enabled Value After Reset: 0x0 Testable: untestable
IPETD	R/W	[10:10]	0x0	Insert Parity error in Tx write-back Descriptor parity generator When set to 1, parity bit of first valid data generated by the DMA Tx write-back descriptor parity generator(or at PG4 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped.Values: 0x0 (DISABLE): Insert Parity error in Tx write-back Descriptor parity generator is disabled 0x1 (ENABLE): Insert Parity error in Tx write-back Descriptor parity generator is enabled Value After Reset: 0x0 Testable: untestable
RESERVED	R	[9:9]	0x0	Reserved Field: Yes
IPEDDC	R/W	[8:8]	0x0	Insert Parity Error in DMA DTX Control word parity generator When set to 1, parity bit of first valid data generated by the DMA DTX Control word parity generator (or at PG2 as shown in Transmit data path

				parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped.Values: 0x0 (DISABLE): Insert Parity Error in DMA DTX Control word parity generator is disabled 0x1 (ENABLE): Insert Parity Error in DMA DTX Control word parity generator is enabled Value After Reset: 0x0 Testable: untestable
IPEMRF	R/W	[7:7]	0x0	Insert Parity Error in MTL Rx FIFO read control parity generator When set to 1, parity bit of first valid data generated by the MTL Rx FIFO read control parity generator (or at PG7 as shown in Receive data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped.Values: 0x0 (DISABLE): Insert Parity Error in MTL Rx FIFO read control parity generator is disabled 0x1 (ENABLE): Insert Parity Error in MTL Rx FIFO read control parity generator is enabled Value After Reset: 0x0 Testable: untestable
IPEMTS	R/W	[6:6]	0x0	Insert Parity Error in MTL Tx Status parity generator When set to 1, parity bit of first valid data generated by the MTL Tx Status parity generator (or at PG6 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once respective parity bit is flipped.Values: 0x0 (DISABLE): Insert Parity Error in MTL Tx

				Status parity generator is disabled 0x1 (ENABLE): Insert Parity Error in MTL Tx Status parity generator is enabled Value After Reset: 0x0 Testable: untestable
IPEMC	R/W	[5:5]	0x0	Insert Parity Error in MTL checksum parity generator When set to 1, parity bit of first valid data generated by the MTL checksum parity generator (or at PG5 as shown in Transmit data path parity protection diagram) is flipped. Hardware clears this bit once the respective parity bit is flipped.Values: 0x0 (DISABLE): Insert Parity Error in MTL checksum parity generator is disabled 0x1 (ENABLE): Insert Parity Error in MTL checksum parity generator is enabled Value After Reset: 0x0 Testable: untestable
RESERVED	R	[4:4]	0x0	Reserved Field: Yes
RESERVED_3	R	[3:3]	0x0	Reserved. Value After Reset: 0x0
EPSI	R/W	[2:2]	0x0	Enable Parity on Slave Interface port When set to 1, enables the parity check for the slave interface ports and disables the internal generation of parity for the input slave data port. When set to 0, disables the parity check for the slave interface ports and enables the internal parity generation for the input slave data port.Values: 0x0 (DISABLE): Parity on Slave Interface port is disabled

				0x1 (ENABLE): Parity on Slave Interface port is enabled Value After Reset: 0x0 Testable: untestable
OPE	R/W	[1:1]	0x0	Odd Parity Enable When set to 1, enables odd parity protection on all the external interfaces and when set to 0, enables even parity protection on all the external interfaces.Values: 0x0 (DISABLE): Odd Parity is disabled 0x1 (ENABLE): Odd Parity is enabled Value After Reset: 0x0
EDPP	R/W	[0:0]	0x0	Enable Data path Parity Protection When set to 1, enables the parity protection for EQOS datapath by generating and checking the parity on EQOS datapath. When set to 0, disables the parity protection for EQOS datapath.Values: 0x0 (DISABLE): Data path Parity Protection is disabled 0x1 (ENABLE): Data path Parity Protection is enabled Value After Reset: 0x0

2.5 EQOS_MTL_Q0

Module Name	EQOS_MTL_Q0
Sub Module Name	
Data Width	32
Address Width	32

Base Address	0x0

2.5.1 EQOS_MTL_Q0_R_MTL_TXQ0_OPERATION_MODE

Access Type: RW

Address Offset: 0xd00

Name	Access	Bit Range	Reset value	Description
RESERVED_31_Y	R	[31:22]	0x0	Reserved. Value After Reset: 0x0
TQS	R/W	[21:16]	0x0	Transmit Queue Size This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits Value After Reset: 0x0
RESERVED_15_7	R	[15:7]	0x0	Reserved. Value After Reset: 0x0
TTC	R/W	[6:4]	0x0	Transmit Threshold Control These bits control the threshold level of the MTL Tx Queue. The transmission starts when the packet size within the MTL Tx Queue is larger than the threshold. In addition, full packets with length less than the threshold are also transmitted. These bits are used only when the TSF bit is reset.Values: 0x0 (M_32BYTES): 32

				0x1 (M_64BYTES): 64 0x2 (M_96BYTES): 96 0x3 (M_128BYTES): 128 0x4 (M_192BYTES): 192 0x5 (M_256BYTES): 256 0x6 (M_384BYTES): 384 0x7 (M_512BYTES): 512 Value After Reset: 0x0
TXQEN	R/W	[3:2]	0x0	Transmit Queue Enable This field is used to enable/disable the transmit queue 0. 2'b00: Not enabled 2'b01: Reserved 2'b10: Enabled 2'b11: Reserved This field is Read Only in Single Queue configurations and Read Write in Multiple Queue configurations. Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field.Values: 0x0 (DISABLE): Not enabled 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV) 0x2 (ENABLE): Enabled

				0x3 (RSVD2): Reserved Value After Reset: 0x0
TSF	R/W	[1:1]	0x0	Transmit Store and Forward When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped.Values: 0x0 (DISABLE): Transmit Store and Forward is disabled 0x1 (ENABLE): Transmit Store and Forward is enabled Value After Reset: 0x0
FTQ	R/W	[0:0]	0x0	Flush Transmit Queue When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.Values: 0x0 (DISABLE): Flush Transmit Queue is disabled 0x1 (ENABLE): Flush Transmit Queue is enabled

				Value After Reset: 0x0 Testable: untestable

2.5.2 EQOS_MTL_Q0_R_MTL_TXQ0_UNDERFLOW

Access Type: RW

Address Offset: 0xd04

Name	Access	Bit Range	Reset value	Description
RESERVED_31_12	R	[31:12]	0x0	Reserved. Value After Reset: 0x0
UFCNTOVF	R	[11:11]	0x0	Overflow Bit for Underflow Packet Counter This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter 0x1 (ACTIVE): Overflow detected for Underflow Packet Counter Value After Reset: 0x0
UFFRMCNT	R	[10:0]	0x0	Underflow Packet Counter This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event. Value After Reset: 0x0

2.5.3 EQOS_MTL_Q0_R_MTL_TXQ0_DEBUG

Access Type: RW

Address Offset: 0xd08

Name	Access	Bit Range	Reset value	Description
RESERVED_31_23	R	[31:23]	0x0	Reserved. Value After Reset: 0x0
STXSTSF	R	[22:20]	0x0	Number of Status Words in Tx Status FIFO of Queue This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO. Value After Reset: 0x0
RESERVED_19	R	[19:19]	0x0	Reserved. Value After Reset: 0x0
PTXQ	R	[18:16]	0x0	Number of Packets in the Transmit Queue This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue. Value After Reset: 0x0
RESERVED_15_6	R	[15:6]	0x0	Reserved. Value After Reset: 0x0
TXSTSFSTS	R	[5:5]	0x0	MTL Tx Status FIFO Full Status When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission.Values: 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected

				Value After Reset: 0x0
TXQSTS	R	[4:4]	0x0	MTL Tx Queue Not Empty Status When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission.Values: 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected Value After Reset: 0x0
TWCSTS	R	[3:3]	0x0	MTL Tx Queue Write Controller Status When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue.Values: 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected Value After Reset: 0x0
TRCSTS	R	[2:1]	0x0	MTL Tx Queue Read Controller Status This field indicates the state of the Tx Queue Read Controller:Values: 0x0 (IDLE): Idle state 0x1 (READ): Read state (transferring data to the MAC transmitter) 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter

				0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC Value After Reset: 0x0
TXQPAUSED	R	[0:0]	0x0	Transmit Queue in Pause When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled Reception of 802.3x Pause packet when PFC is disabled Values: 0x0 (INACTIVE): Transmit Queue in Pause status is not detected 0x1 (ACTIVE): Transmit Queue in Pause status is detected Value After Reset: 0x0

2.5.4 EQOS_MTL_Q0_R_MTL_TXQ0_ETS_STATUS

Access Type: RW

Address Offset: 0xd14

Name	Access	Bit Range	Reset value	Description
RESERVED_31_24	R	[31:24]	0x0	Reserved. Value After Reset: 0x0
ABS	R	[23:0]	0x0	Average Bits per Slot This field contains the average transmitted bits per slot. When the DCB operation is enabled for Queue 0, this field is computed over every 10 million bit

				times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680. Value After Reset: 0x0

2.5.5 EQOS_MTL_Q0_R_MTL_TXQ0_QUANTUM_WEIGHT

Access Type: RW

Address Offset: 0xd18

Name	Access	Bit Range	Reset value	Description
RESERVED_31_21	R	[31:21]	0x0	Reserved. Value After Reset: 0x0
ISCQW	R/W	[20:0]	0x0	Quantum or Weights When the DCB operation is enabled with DWRR algorithm for Queue 0 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. When DCB operation is enabled with WFQ algorithm for Queue 0 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. The higher the programmed weights lesser the bandwidth allocated for the particular Transmit Queue. This is because the weights are used to compute the packet finish time (weights*packet_size). Lesser the finish time, higher the probability of the packet getting scheduled first and using more bandwidth. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 0 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero. Value After Reset: 0x0

2.5.6 EQOS_MTL_Q0_R_MTL_Q0_INTERRUPT_CONTROL_STATUS

Access Type: RW

Address Offset: 0xd2c

Name	Access	Bit Range	Reset value	Description

RESERVED_31_25	R	[31:25]	0x0	Reserved. Value After Reset: 0x0
RXOIE	R/W	[24:24]	0x0	Receive Queue Overflow Interrupt Enable When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled.Values: 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled Value After Reset: 0x0
RESERVED_23_17	R	[23:17]	0x0	Reserved. Value After Reset: 0x0
RXOVFIS	R/W	[16:16]	0x0	Receive Queue Overflow Interrupt Status This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.Values: 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected 0x1 (ACTIVE): Receive Queue Overflow Interrupt Status detected Value After Reset: 0x0 Testable: untestable
RESERVED_15_10	R	[15:10]	0x0	

				Reserved. Value After Reset: 0x0
ABPSIE	R/W	[9:9]	0x0	Average Bits Per Slot Interrupt Enable When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event.Values: 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled Value After Reset: 0x0
TXUIE	R/W	[8:8]	0x0	Transmit Queue Underflow Interrupt Enable When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled.Values: 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled Value After Reset: 0x0
RESERVED_7_2	R	[7:2]	0x0	Reserved. Value After Reset: 0x0
ABPSIS	R/W	[1:1]	0x0	Average Bits Per Slot Interrupt Status When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal

				event. Setting 1 clears. Setting 0 has no effect.Values: 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected Value After Reset: 0x0 Testable: untestable
TXUNFIS	R/W	[0:0]	0x0	Transmit Queue Underflow Interrupt Status This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.Values: 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected Value After Reset: 0x0 Testable: untestable

2.5.7 EQOS_MTL_Q0_R_MTL_RXQ0_OPERATION_MODE

Access Type: RW

Address Offset: 0xd30

Name	Access	Bit Range	Reset value	Description
RESERVED_31_Y	R	[31:26]	0x0	Reserved. Value After Reset: 0x0
RQS	R/W	[25:20]	0x0	Receive Queue Size

				This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits Value After Reset: 0x0
RESERVED_19_Y	R	[19:19]	0x0	Reserved. Value After Reset: 0x0
RFD	R/W	[18:14]	0x0	Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: 0: Full minus 1 KB, that is, FULL 1 KB 1: Full minus 1.5 KB, that is, FULL 1.5 KB 2: Full minus 2 KB, that is, FULL 2 KB 3: Full minus 2.5 KB, that is, FULL 2.5 KB ... 30: Full minus 16 KB, that is, FULL 16 KB 31: Full minus 16.5 KB, that is, FULL 16.5 KB

				The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only. Value After Reset: 0x0
RESERVED_13_Y	R	[13:13]	0x0	Reserved. Value After Reset: 0x0
RFA	R/W	[12:8]	0x0	Threshold for Activating Flow Control (in half-duplex and full-duplex These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD. Value After Reset: 0x0
EHFC	R/W	[7:7]	0x0	Enable Hardware Flow Control When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled.Values: 0x0 (DISABLE): Hardware Flow Control is disabled 0x1 (ENABLE): Hardware Flow Control is enabled Value After Reset: 0x0

DIS_TCP_EF	R/W	[6:6]	0x0	Disable Dropping of TCP/IP Checksum Error Packets When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset.Values: 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled Value After Reset: 0x0
RSF	R/W	[5:5]	0x0	Receive Queue Store and Forward When this bit is set, the DWC_ether_qos reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register.Values: 0x0 (DISABLE): Receive Queue Store and Forward is disabled 0x1 (ENABLE): Receive Queue Store and Forward is enabled Value After Reset: 0x0
FEP	R/W	[4:4]	0x0	Forward Error Packets When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte

				(write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA.Values: 0x0 (DISABLE): Forward Error Packets is disabled 0x1 (ENABLE): Forward Error Packets is enabled Value After Reset: 0x0
FUP	R/W	[3:3]	0x0	Forward Undersized Good Packets When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01.Values: 0x0 (DISABLE): Forward Undersized Good Packets is disabled 0x1 (ENABLE): Forward Undersized Good Packets is enabled Value After Reset: 0x0
RESERVED_2	R	[2:2]	0x0	Reserved. Value After Reset: 0x0
RTC	R/W	[1:0]	0x0	Receive Queue Threshold Control These bits control the threshold level of the MTL Rx queue (in bytes):

				The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1.Values: 0x0 (M_64BYTE): 64 0x1 (M_32BYTE): 32 0x2 (M_96BYTE): 96 0x3 (M_128BYTE): 128 Value After Reset: 0x0

2.5.8 EQOS_MTL_Q0_R_MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT

Access Type: RW

Address Offset: 0xd34

Name	Access	Bit Range	Reset value	Description
RESERVED_31_28	R	[31:28]	0x0	Reserved. Value After Reset: 0x0
MISCNTOVF	R	[27:27]	0x0	Missed Packet Counter Overflow Bit When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): Missed Packet Counter overflow not detected 0x1 (ACTIVE): Missed Packet Counter overflow detected Value After Reset: 0x0

MISPKTCNT	R	[26:16]	0x0	Missed Packet Counter This field indicates the number of packets missed by the DWC_ether_qos because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event. Value After Reset: 0x0
RESERVED_15_12	R	[15:12]	0x0	Reserved. Value After Reset: 0x0
OVFCNTOVF	R	[11:11]	0x0	Overflow Counter Overflow Bit When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): Overflow Counter overflow not detected 0x1 (ACTIVE): Overflow Counter overflow detected Value After Reset: 0x0
OVFPKTCNT	R	[10:0]	0x0	Overflow Packet Counter This field indicates the number of packets discarded by the DWC_ether_qos because of Receive queue overflow. This counter is incremented each time the DWC_ether_qos discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event. Value After Reset: 0x0

2.5.9 EQOS_MTL_Q0_R_MTL_RXQ0_DEBUG

Access Type: RW

Address Offset: 0xd38

Name	Access	Bit Range	Reset value	Description
RESERVED_31_30	R	[31:30]	0x0	Reserved. Value After Reset: 0x0
PRXQ	R	[29:16]	0x0	Number of Packets in Receive Queue This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/Min_Packet_Size. Value After Reset: 0x0
RESERVED_15_6	R	[15:6]	0x0	Reserved. Value After Reset: 0x0
RXQSTS	R	[5:4]	0x0	MTL Rx Queue Fill-Level Status This field gives the status of the fill-level of the Rx Queue:Values: 0x0 (EMPTY): Rx Queue empty 0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold 0x3 (FULL): Rx Queue full Value After Reset: 0x0
RESERVED_3	R	[3:3]	0x0	Reserved. Value After Reset: 0x0
RRCSTS	R	[2:1]	0x0	MTL Rx Queue Read Controller State This field gives the state of the Rx queue Read controller:Values:

				0x0 (IDLE): Idle state 0x1 (READ_DATA): Reading packet data 0x2 (READ_STS): Reading packet status (or timestamp) 0x3 (FLUSH): Flushing the packet data and status Value After Reset: 0x0
RWCSTS	R	[0:0]	0x0	MTL Rx Queue Write Controller Active Status When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue.Values: 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected Value After Reset: 0x0

2.5.10 EQOS_MTL_Q0_R_MTL_RXQ0_CONTROL

Access Type: RW

Address Offset: 0xd3c

Name	Access	Bit Range	Reset value	Description
RESERVED_31_4	R	[31:4]	0x0	Reserved. Value After Reset: 0x0
RXQ_FRM_ARBIT	R/W	[3:3]	0x0	Receive Queue Packet Arbitration When this bit is set, the DWC_ether_qos drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the DWC_ether_qos drives the

				packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: PBL amount of data (indicated by ari_qN_pbl_i[]) or Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the DWC_ether_qos drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode).Values: 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled Value After Reset: 0x0
RXQ_WEGT	R/W	[2:0]	0x0	Receive Queue Weight This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode

				register. Value After Reset: 0x0

2.6 EQOS_MTL_Q1

Module Name	EQOS_MTL_Q1
Sub Module Name	
Data Width	32
Address Width	32
Base Address	0x0

2.6.1 EQOS_MTL_Q1_R_MTL_TXQ(#I)_OPERATION_MODE(FORI=1;I<=3)

Access Type: RW

Address Offset: (0x0040*i)+0x0D00

Name	Access	Bit Range	Reset value	Description
RESERVED_31_Y	R	[31:22]	0x0	Reserved. Value After Reset: 0x0
TQS	R/W	[21:16]	0x0	Transmit Queue Size This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming TQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (TQS+1)*256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits Value After Reset: 0x0
RESERVED_15_7	R	[15:7]	0x0	Reserved. Value After Reset: 0x0

TTC	R/W	[6:4]	0x0	Transmit Threshold Control These bits control the threshold level of the MTL Tx Queue. The transmission starts when the packet size within the MTL Tx Queue is larger than the threshold. In addition, full packets with length less than the threshold are also transmitted. These bits are used only when the TSF bit is reset.Values: 0x0 (M_32BYTES): 32 0x1 (M_64BYTES): 64 0x2 (M_96BYTES): 96 0x3 (M_128BYTES): 128 0x4 (M_192BYTES): 192 0x5 (M_256BYTES): 256 0x6 (M_384BYTES): 384 0x7 (M_512BYTES): 512 Value After Reset: 0x0
TXQEN	R/W	[3:2]	0x0	Transmit Queue Enable This field is used to enable/disable the transmit queue 0. 2'b00: Not enabled 2'b01: Enable in AV mode 2'b10: Enabled 2'b11: Reserved Note: In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field.Values:

				0x0 (DISABLE): Not enabled 0x1 (EN_IF_AV): Enable in AV mode (Reserved in non-AV) 0x2 (ENABLE): Enabled 0x3 (RSVD2): Reserved Value After Reset: 0x0
TSF	R/W	[1:1]	0x0	Transmit Store and Forward When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped.Values: 0x0 (DISABLE): Transmit Store and Forward is disabled 0x1 (ENABLE): Transmit Store and Forward is enabled Value After Reset: 0x0
FTQ	R/W	[0:0]	0x0	Flush Transmit Queue When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock

				(clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.Values: 0x0 (DISABLE): Flush Transmit Queue is disabled 0x1 (ENABLE): Flush Transmit Queue is enabled Value After Reset: 0x0 Testable: untestable

2.6.2 EQOS_MTL_Q1_R_MTL_TXQ(#I)_UNDERFLOW(FORI=1;I<=3)

Access Type: RW

Address Offset: (0x0040*i)+0x0D04

Name	Access	Bit Range	Reset value	Description
RESERVED_31_12	R	[31:12]	0x0	Reserved. Value After Reset: 0x0
UFCNTOVF	R	[11:11]	0x0	Overflow Bit for Underflow Packet Counter This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): Overflow not detected for Underflow Packet Counter 0x1 (ACTIVE): Overflow detected for Underflow Packet Counter Value After Reset: 0x0
UFFRMCNT	R	[10:0]	0x0	Underflow Packet Counter This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC

				aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event. Value After Reset: 0x0

2.6.3 EQOS_MTL_Q1_R_MTL_TXQ(#I)_DEBUG(FORI=1;I<=3)

Access Type: RW

Address Offset: (0x0040*i)+0x0D08

Name	Access	Bit Range	Reset value	Description
RESERVED_31_23	R	[31:23]	0x0	Reserved. Value After Reset: 0x0
STXSTSF	R	[22:20]	0x0	Number of Status Words in Tx Status FIFO of Queue This field indicates the current number of status in the Tx Status FIFO of this queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO. Value After Reset: 0x0
RESERVED_19	R	[19:19]	0x0	Reserved. Value After Reset: 0x0
PTXQ	R	[18:16]	0x0	Number of Packets in the Transmit Queue This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue. Value After Reset: 0x0
RESERVED_15_6	R	[15:6]	0x0	Reserved. Value After Reset: 0x0
TXSTSFSTS	R	[5:5]	0x0	MTL Tx Status FIFO Full Status When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot

				accept any more packets for transmission.Values: 0x0 (INACTIVE): MTL Tx Status FIFO Full status is not detected 0x1 (ACTIVE): MTL Tx Status FIFO Full status is detected Value After Reset: 0x0
TXQSTS	R	[4:4]	0x0	MTL Tx Queue Not Empty Status When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission.Values: 0x0 (INACTIVE): MTL Tx Queue Not Empty status is not detected 0x1 (ACTIVE): MTL Tx Queue Not Empty status is detected Value After Reset: 0x0
TWCSTS	R	[3:3]	0x0	MTL Tx Queue Write Controller Status When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue.Values: 0x0 (INACTIVE): MTL Tx Queue Write Controller status is not detected 0x1 (ACTIVE): MTL Tx Queue Write Controller status is detected Value After Reset: 0x0
TRCSTS	R	[2:1]	0x0	MTL Tx Queue Read Controller Status This field indicates the state of the Tx Queue Read Controller:Values:

				0x0 (IDLE): Idle state 0x1 (READ): Read state (transferring data to the MAC transmitter) 0x2 (WAIT): Waiting for pending Tx Status from the MAC transmitter 0x3 (FLUSH): Flushing the Tx queue because of the Packet Abort request from the MAC Value After Reset: 0x0
TXQPAUSED	R	[0:0]	0x0	Transmit Queue in Pause When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled Reception of 802.3x Pause packet when PFC is disabled Values: 0x0 (INACTIVE): Transmit Queue in Pause status is not detected 0x1 (ACTIVE): Transmit Queue in Pause status is detected Value After Reset: 0x0

2.6.4 EQOS_MTL_Q1_R_MTL_TXQ(#I)_ETS_CONTROL(FORI=1;I<=3)

Access Type: RW

Address Offset: (0x0040*i)+0x0D10

Name	Access	Bit Range	Reset value	Description
RESERVED_31_7	R	[31:7]	0x0	Reserved. Value After Reset: 0x0

SLC	R/W	[6:4]	0x0	Slot Count If the credit-based shaper algorithm is enabled, the software can program the number of slots (of duration programmed in DMA_CH(#i)_Slot_Interval register) over which the average transmitted bits per slot, provided in the MTL_TxQ(#i)_ETS_Status register, need to be computed for Queue. The encoding is as follows:Values: 0x0 (M_1_SLOT): 1 slot 0x1 (M_2_SLOT): 2 slots 0x2 (M_4_SLOT): 4 slots 0x3 (M_8_SLOT): 8 slots 0x4 (M_16_SLOT): 16 slots 0x5 (RSVD): Reserved Value After Reset: 0x0
CC	R/W	[3:3]	0x0	Credit Control When this bit is set, the accumulated credit parameter in the credit-based shaper algorithm logic is not reset to zero when there is positive credit and no packet to transmit in Channel 1. The credit accumulates even when there is no packet waiting in Channel 1 and another channel is transmitting. When this bit is reset, the accumulated credit parameter in the credit-based shaper algorithm logic is set to zero when there is positive credit and no packet to transmit in Channel 1. When there is no packet waiting in Channel 1 and other channel is transmitting, no credit is accumulated.Values: 0x0 (DISABLE): Credit Control is disabled 0x1 (ENABLE): Credit Control is enabled

				Value After Reset: 0x0
AVALG	R/W	[2:2]	0x0	AV Algorithm When Queue 1 is programmed for AV, this field configures the scheduling algorithm for this queue: This bit when set, indicates credit based shaper algorithm (CBS) is selected for Queue 1 traffic. When reset, strict priority is selected.Values: 0x0 (DISABLE): CBS Algorithm is disabled 0x1 (ENABLE): CBS Algorithm is enabled Value After Reset: 0x0
RESERVED_1_0	R	[1:0]	0x0	Reserved. Value After Reset: 0x0

2.6.5 EQOS_MTL_Q1_R_MTL_TXQ(#I)_ETS_STATUS(FORI=1;I<=3)

Access Type: RW

Address Offset: (0x0040*i)+0x0D14

Name	Access	Bit Range	Reset value	Description
RESERVED_31_24	R	[31:24]	0x0	Reserved. Value After Reset: 0x0
ABS	R	[23:0]	0x0	Average Bits per Slot This field contains the average transmitted bits per slot. If AV operation is enabled, this field is computed over number of slots, programmed in the SLC field of MTL_TxQ(#i)_ETS_CONTROL register. The maximum value of this field is 0x6_4000 in 100 Mbps, 0x3E_8000 in 1000 Mbps and 9C_4000 in 2500 Mbps mode respectively. When the DCB operation is enabled for Queue, this field is computed over every 10 million bit times slot (4 ms in 2500 Mbps; 10 ms in 1000 Mbps; 100 ms in 100 Mbps). The maximum value is 0x989680. Value After Reset: 0x0

2.6.6 EQOS_MTL_Q1_R_MTL_TXQ(#I)_QUANTUM_WEIGHT(FORI=1;I<=3)

Access Type: RW

Address Offset: (0x0040*i)+0x0D18

Name	Access	Bit Range	Reset value	Description
RESERVED_31_21	R	[31:21]	0x0	Reserved. Value After Reset: 0x0
ISCQW	R/W	[20:0]	0x0	idleSlopeCredit, Quantum or Weights idleSlopeCredit When AV feature is enabled, this field contains the idleSlopeCredit value required for the credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns for 100 Mbps; 8 ns for 1000 Mbps; 3.2 ns for 2500 Mbps) when the credit is increasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. Bits[20:14] must be written to zero. Quantum When the DCB operation is enabled with DWRR algorithm for Queue 1 traffic, this field contains the quantum value in bytes to be added to credit during every queue scanning cycle. The maximum value is 0x1312D0 bytes. Weights When DCB operation is enabled with WFQ algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x3FFF where weight of 0 indicates 100% bandwidth. Bits[20:14] must be written to zero. When DCB operation or generic queuing operation is enabled with WRR algorithm for Queue 1 traffic, this field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero. Note 1: In multiple Queue configuration this field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled.

				This field need not be programmed when only Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register. Note 2: For WFQ algorithm, higher the programmed weights lesser the bandwidth allocated for that Transmit Queue. The finish time is not a function of particular packet alone but it is as per the formula: (previous_finish_time of particular Transmit Queue + (weights*packet_size)) Note 3: The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time. Value After Reset: 0x0

2.6.7 EQOS_MTL_Q1_R_MTL_TXQ(#I)_SENDSLOPECREDIT(FORI=1;I<=3)

Access Type: RW

Address Offset: (0x0040*i)+0x0D1C

Name	Access	Bit Range	Reset value	Description
RESERVED_31_14	R	[31:14]	0x0	Reserved. Value After Reset: 0x0
SSC	R/W	[13:0]	0x0	sendSlopeCredit Value When AV operation is enabled, this field contains the sendSlopeCredit value required for credit-based shaper algorithm for Queue 1. This is the rate of change of credit in bits per cycle (40 ns, 8 ns and 3.2 ns for 100 Mbps, 1000 Mbps and 2500 Mbps respectively) when the credit is decreasing. The software should program this field with computed credit in bits per cycle scaled by 1,024. The maximum value is portTransmitRate, that is, 0x2000 in 1000/2500 Mbps mode and 0x1000 in 100 Mbps mode. This field should be programmed with absolute sendSlopeCredit value. The credit-based shaper logic subtracts it from the accumulated credit when Channel 1 is selected for transmission. Value After Reset: 0x0

2.6.8 EQOS_MTL_Q1_R_MTL_TXQ(#I)_HICREDIT(FORI=1;I<=3)

Access Type: RW

Address Offset: (0x0040*i)+0x0D20

Name	Access	Bit Range	Reset value	Description
RESERVED_31_29	R	[31:29]	0x0	Reserved. Value After Reset: 0x0
HC	R/W	[28:0]	0x0	hiCredit Value When the AV feature is enabled, this field contains the hiCredit value required for the credit-based shaper algorithm. This is the maximum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value is maxInterferenceSize, that is, best-effort maximum packet size (16,384 bytes or 131,072 bits). The value to be specified is 131,072 * 1,024 = 134,217,728 or 0x0800_0000. Value After Reset: 0x0

2.6.9 EQOS_MTL_Q1_R_MTL_TXQ(#I)_LOCREDIT(FORI=1;I<=3)

Access Type: RW

Address Offset: (0x0040*i)+0x0D24

Name	Access	Bit Range	Reset value	Description
RESERVED_31_29	R	[31:29]	0x0	Reserved. Value After Reset: 0x0
LC	R/W	[28:0]	0x0	loCredit Value When AV operation is enabled, this field contains the loCredit value required for the credit-based shaper algorithm. This is the minimum value that can be accumulated in the credit parameter. This is specified in bits scaled by 1,024. The maximum value to be programmed is corresponds to twice the maxFrameSize transmitted from this queue. If the maxFrameSize is 8192 bytes, then (8192*2) * 8 * 1024 = 134,217,728 or 0x0800_0000. Because it is a negative value, the programmed value is 2's complement of the value, that is, 0x1800_0000. Value After Reset: 0x0

2.6.10 EQOS_MTL_Q1_R_MTL_Q(#I)_INTERRUPT_CONTROL_STATUS)(FORI=1;I<=3)

Access Type: RW

Address Offset: (0x0040*i)+0x0D2C

Name	Access	Bit Range	Reset value	Description
RESERVED_31_25	R	[31:25]	0x0	Reserved. Value After Reset: 0x0
RXOIE	R/W	[24:24]	0x0	Receive Queue Overflow Interrupt Enable When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled.Values: 0x0 (DISABLE): Receive Queue Overflow Interrupt is disabled 0x1 (ENABLE): Receive Queue Overflow Interrupt is enabled Value After Reset: 0x0
RESERVED_23_17	R	[23:17]	0x0	Reserved. Value After Reset: 0x0
RXOVFIS	R/W	[16:16]	0x0	Receive Queue Overflow Interrupt Status This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.Values: 0x0 (INACTIVE): Receive Queue Overflow Interrupt Status not detected 0x1 (ACTIVE): Receive Queue Overflow Interrupt

				Status detected Value After Reset: 0x0 Testable: untestable
RESERVED_15_10	R	[15:10]	0x0	Reserved. Value After Reset: 0x0
ABPSIE	R/W	[9:9]	0x0	Average Bits Per Slot Interrupt Enable When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. When this bit is cleared, the interrupt is not asserted for such an event.Values: 0x0 (DISABLE): Average Bits Per Slot Interrupt is disabled 0x1 (ENABLE): Average Bits Per Slot Interrupt is enabled Value After Reset: 0x0
TXUIE	R/W	[8:8]	0x0	Transmit Queue Underflow Interrupt Enable When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled.Values: 0x0 (DISABLE): Transmit Queue Underflow Interrupt Status is disabled 0x1 (ENABLE): Transmit Queue Underflow Interrupt Status is enabled Value After Reset: 0x0
RESERVED_7_2	R	[7:2]	0x0	Reserved. Value After Reset: 0x0

ABPSIS	R/W	[1:1]	0x0	Average Bits Per Slot Interrupt Status When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.Values: 0x0 (INACTIVE): Average Bits Per Slot Interrupt Status not detected 0x1 (ACTIVE): Average Bits Per Slot Interrupt Status detected Value After Reset: 0x0 Testable: untestable
TXUNFIS	R/W	[0:0]	0x0	Transmit Queue Underflow Interrupt Status This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect.Values: 0x0 (INACTIVE): Transmit Queue Underflow Interrupt Status not detected 0x1 (ACTIVE): Transmit Queue Underflow Interrupt Status detected Value After Reset: 0x0 Testable: untestable

2.6.11 EQOS_MTL_Q1_R_MTL_RXQ(#I)_OPERATION_MODE(FORI=1;I<=3)

Access Type: RW

Address Offset: (0x0040*i)+0x0D30

Name	Access	Bit Range	Reset value	Description

RESERVED_31_Y	R	[31:26]	0x0	Reserved. Value After Reset: 0x0
RQS	R/W	[25:20]	0x0	Receive Queue Size This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The RQS field is read-write only if the number of Rx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. This means that value of 0x0 = 256 bytes, 0x1 = 512 bytes and so on, so user should be programming RQS [5:0] = 6'b001111 to allocate queue size of 4096 (4K) bytes. In general, the size of the Queue = (RQS+1)*256 bytes. When the number of Rx Queues is one, the field is read-only and the configured RX FIFO size in blocks of 256 bytes is reflected in the reset value. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits Value After Reset: 0x0
RESERVED_19_Y	R	[19:19]	0x0	Reserved. Value After Reset: 0x0
RFD	R/W	[18:14]	0x0	Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: 0: Full minus 1 KB, that is, FULL 1 KB 1: Full minus 1.5 KB, that is, FULL 1.5 KB 2: Full minus 2 KB, that is, FULL 2 KB 3: Full minus 2.5 KB, that is, FULL 2.5 KB ...

				30: Full minus 16 KB, that is, FULL 16 KB 31: Full minus 16.5 KB, that is, FULL 16.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only. Value After Reset: 0x0
RESERVED_13_Y	R	[13:13]	0x0	Reserved. Value After Reset: 0x0
RFA	R/W	[12:8]	0x0	Threshold for Activating Flow Control (in half-duplex and full-duplex These bits control the threshold (fill-level of Rx queue) at which the flow control is activated: For more information on encoding for this field, see RFD. Value After Reset: 0x0
EHFC	R/W	[7:7]	0x0	Enable Hardware Flow Control When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled.Values: 0x0 (DISABLE): Hardware Flow Control is disabled

				0x1 (ENABLE): Hardware Flow Control is enabled Value After Reset: 0x0
DIS_TCP_EF	R/W	[6:6]	0x0	Disable Dropping of TCP/IP Checksum Error Packets When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset.Values: 0x0 (ENABLE): Dropping of TCP/IP Checksum Error Packets is enabled 0x1 (DISABLE): Dropping of TCP/IP Checksum Error Packets is disabled Value After Reset: 0x0
RSF	R/W	[5:5]	0x0	Receive Queue Store and Forward When this bit is set, the DWC_ether_qos reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register.Values: 0x0 (DISABLE): Receive Queue Store and Forward is disabled 0x1 (ENABLE): Receive Queue Store and Forward is enabled Value After Reset: 0x0
FEP	R/W	[4:4]	0x0	

				Forward Error Packets When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet might be forwarded to the application or DMA.Values: 0x0 (DISABLE): Forward Error Packets is disabled 0x1 (ENABLE): Forward Error Packets is enabled Value After Reset: 0x0
FUP	R/W	[3:3]	0x0	Forward Undersized Good Packets When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01.Values: 0x0 (DISABLE): Forward Undersized Good Packets is disabled 0x1 (ENABLE): Forward Undersized Good Packets is enabled Value After Reset: 0x0
RESERVED_2	R	[2:2]	0x0	Reserved. Value After Reset: 0x0

RTC	R/W	[1:0]	0x0	Receive Queue Threshold Control These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1.Values: 0x0 (M_64BYTE): 64 0x1 (M_32BYTE): 32 0x2 (M_96BYTE): 96 0x3 (M_128BYTE): 128 Value After Reset: 0x0

2.6.12 EQOS_MTL_Q1_R_MTL_RXQ(#I)_MISSED_PACKET_OVERFLOW_CNT(FORI=1;I<=3)

Access Type: RW

Address Offset: (0x0040*i)+0x0D34

Name	Access	Bit Range	Reset value	Description
RESERVED_31_28	R	[31:28]	0x0	Reserved. Value After Reset: 0x0
MISCNTOVF	R	[27:27]	0x0	Missed Packet Counter Overflow Bit When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): Missed Packet Counter overflow not detected 0x1 (ACTIVE): Missed Packet Counter overflow

				detected Value After Reset: 0x0
MISPKTCNT	R	[26:16]	0x0	Missed Packet Counter This field indicates the number of packets missed by the DWC_ether_qos because the application asserted ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event. Value After Reset: 0x0
RESERVED_15_12	R	[15:12]	0x0	Reserved. Value After Reset: 0x0
OVFCNTOVF	R	[11:11]	0x0	Overflow Counter Overflow Bit When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event.Values: 0x0 (INACTIVE): Overflow Counter overflow not detected 0x1 (ACTIVE): Overflow Counter overflow detected Value After Reset: 0x0
OVFPKTCNT	R	[10:0]	0x0	Overflow Packet Counter This field indicates the number of packets discarded by the DWC_ether_qos because of Receive queue overflow. This counter is incremented each time the DWC_ether_qos discards an incoming packet because of overflow. This counter is reset when this

				register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event. Value After Reset: 0x0

2.6.13 EQOS_MTL_Q1_R_MTL_RXQ(#I)_DEBUG(FORI=1;I<=3)

Access Type: RW

Address Offset: (0x0040*i)+0x0D38

Name	Access	Bit Range	Reset value	Description
RESERVED_31_30	R	[31:30]	0x0	Reserved. Value After Reset: 0x0
PRXQ	R	[29:16]	0x0	Number of Packets in Receive Queue This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/Min_Packet_Size. Value After Reset: 0x0
RESERVED_15_6	R	[15:6]	0x0	Reserved. Value After Reset: 0x0
RXQSTS	R	[5:4]	0x0	MTL Rx Queue Fill-Level Status This field gives the status of the fill-level of the Rx Queue:Values: 0x0 (EMPTY): Rx Queue empty 0x1 (BLW_THR): Rx Queue fill-level below flow-control deactivate threshold 0x2 (ABV_THR): Rx Queue fill-level above flow-control activate threshold 0x3 (FULL): Rx Queue full Value After Reset: 0x0
RESERVED_3	R	[3:3]	0x0	Reserved.

				Value After Reset: 0x0
RRCSTS	R	[2:1]	0x0	MTL Rx Queue Read Controller State This field gives the state of the Rx queue Read controller:Values: 0x0 (IDLE): Idle state 0x1 (READ_DATA): Reading packet data 0x2 (READ_STS): Reading packet status (or timestamp) 0x3 (FLUSH): Flushing the packet data and status Value After Reset: 0x0
RWCSTS	R	[0:0]	0x0	MTL Rx Queue Write Controller Active Status When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue.Values: 0x0 (INACTIVE): MTL Rx Queue Write Controller Active Status not detected 0x1 (ACTIVE): MTL Rx Queue Write Controller Active Status detected Value After Reset: 0x0

2.6.14 EQOS_MTL_Q1_R_MTL_RXQ(#I)_CONTROL(FORI=1;I<=3)

Access Type: RW

Address Offset: (0x0040*i)+0x0D3C

Name	Access	Bit Range	Reset value	Description
RESERVED_31_4	R	[31:4]	0x0	Reserved. Value After Reset: 0x0
RXQ_FRM_ARBIT	R/W	[3:3]	0x0	Receive Queue Packet Arbitration

				When this bit is set, the DWC_ether_qos drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. When this bit is reset, the DWC_ether_qos drives the packet data to the ARI interface such that the following amount of data of currently-selected queue is transmitted before switching to other queue: PBL amount of data (indicated by ari_qN_pbl_i[]) or Complete data of a packet The status and the timestamp are not a part of the PBL data. Therefore, the DWC_ether_qos drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode).Values: 0x0 (DISABLE): Receive Queue Packet Arbitration is disabled 0x1 (ENABLE): Receive Queue Packet Arbitration is enabled Value After Reset: 0x0
RXQ_WEGT	R/W	[2:0]	0x0	Receive Queue Weight This field indicates the weight assigned to the Rx Queue 0. This field needs to be programmed with one value less than the required weight, i.e. reset value of 0 indicates weight of 1, value of 1 indicates weight of 2, and so on. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle. Note: The change in value of RXQ_WEGT takes effect only after the completion of current service round or when there is change from RAA=SP to RAA=WSP algorithm. This approach is taken so that

				there is smooth transition. For the RXQ_WEGT value to take effect at the start, the MTL_RxQ(#i)_Control registers must be programmed before the MTL_Operation_Mode register. Value After Reset: 0x0