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## 2.1 Simple execution, without data forwarding techniques

f)	Clock cycles	377	Stalls: - Data	192
	Instructions	166	- Structural	0
	Average CPI	2.271	- Branch Taken	15

- g) Ao analisar a execução do programa, podemos concluir que a branch prediction policy é branch not taken porque, pela pipeline, antes de saber o resultado do branch, começamos a executar a instrução 'halt' que é a instrução que se executaria caso o salto não fosse tomado.

## 2.2 Application of data forwarding techniques

c)	Clock cycles	297
	Instructions	166
	Average CPI	1.789

Stalls:	- Data	112
	- Structural	16
	- Branch Taken	15

d)

$$\text{speedup} = \frac{\text{Time base}}{\text{Time run forwarding}} = \frac{(\text{CPI}_{\text{base}} \times \# \text{inst}_{\text{base}}) / \text{clock rate}_{\text{base}}}{(\text{CPI}_{\text{forwarding}} \times \# \text{inst}_{\text{forwarding}}) / \text{clock rate}_{\text{forwarding}}} = \frac{\text{CPI}_{\text{base}}}{\text{CPI}_{\text{forwarding}}} = \frac{2.271}{1.789} = 1.269$$

→ como a arquitetura, o compilador e o programa são iguais, #inst e clock rate são iguais

## 2.3 Source code optimization: minimization of data and structural hazards

- a) Attach a copy of the new assembly program.

c)

Clock cycles	233
Instructions	166
Average CPI	1.404

Stalls:	- Data	48
	- Structural	16
	- Branch Taken	15

d)

$$\text{speedup} = \frac{\text{Time base}}{\text{Time opt}} = \frac{(\text{CPI}_{\text{base}} \times \# \text{inst}_{\text{base}}) / \text{clock rate}_{\text{base}}}{(\text{CPI}_{\text{opt}} \times \# \text{inst}_{\text{opt}}) / \text{clock rate}_{\text{opt}}} = \frac{\text{CPI}_{\text{base}}}{\text{CPI}_{\text{opt}}} = \frac{2.271}{1.404} = 1.618$$

→ como a arquitetura, o compilador e o programa são iguais, #inst e clock rate são iguais

## 2.4 Source code optimization: loop unrolling

a) Attach a copy of the new assembly program.

c)

Clock cycles	153
Instructions	126
Average CPI	1.214

Stalls: - Data	0
- Structural	16
- Branch Taken	7

d)

$$\text{speedup} = \frac{\text{Time}_{\text{base}}}{\text{Time}_{\text{otim}}} = \frac{(\text{CPI}_{\text{base}} \times \# \text{inst}_{\text{base}}) / \text{clock rate}_{\text{base}}}{(\text{CPI}_{\text{otim}} \times \# \text{inst}_{\text{otim}}) / \text{clock rate}_{\text{otim}}} = \rightarrow \text{como a arquitetura é igual, clock rate é igual}$$

$$= \frac{\text{CPI}_{\text{base}} \times \# \text{inst}_{\text{base}}}{\text{CPI}_{\text{otim}} \times \# \text{inst}_{\text{otim}}} = \frac{2.271 \times 166}{1.214 \times 126} = 2.465$$

## 2.5 Source code optimization: branch delay slot

a) Attach a copy of the new assembly program.

d)

Clock cycles	218
Instructions	166
Average CPI	1.313

Stalls: - Data	48
- Structural	16
- Branch Taken	0

e)

$$\text{speedup} = \frac{\text{Time}_{\text{base}}}{\text{Time}_{\text{otim}}} = \frac{(\text{CPI}_{\text{base}} \times \# \text{inst}_{\text{base}}) / \text{clock rate}_{\text{base}}}{(\text{CPI}_{\text{otim}} \times \# \text{inst}_{\text{otim}}) / \text{clock rate}_{\text{otim}}} = \rightarrow \text{como arquitetura, compilador e programa são iguais, \#inst e clock rate são iguais}$$

$$= \frac{\text{CPI}_{\text{base}}}{\text{CPI}_{\text{otim}}} = \frac{2.271}{1.313} = 1.730$$

1. *Staphylococcus aureus* (100%)

$$CPI = \frac{23}{11} = 2.091$$

**Table 1:** Pipeline time diagram, without data forwarding techniques.

[illegible]

próxima  
iteração



Table 3: Pipeline time diagram, with minimization techniques to reduce the data and structural hazards.

INSTRUCTIONS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40		
1 lw \$t0, 0(\$t2)	F	D	X	M	W																																					
2 lw \$t1, 0(\$t3)		F	D	X	M	W																																				
3 jmul \$t2, \$t0, \$t1			F	D	X	M	W																																			
4 daddi \$t, \$t, 4				F	D	X	M	W																																		
5 daddi \$t, \$t, 8					F	D	X	M	W																																	
6 daddi \$t, \$t, 8						F	D	X	M	W																																
7 daddi \$t, \$t, 8							F	D	X	M	W																															
8 jaddi \$t2, \$t2, \$t0								F	D	X	M	W																														
9 sw \$t2, -8(\$t4)									F	D	X	M	W																													
10 bne \$t, \$t, loop										F	D	X	M	W																												
11 halt														F																												
12 lw \$t0, 0(\$t2)															F	D	X	M	W																							
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**Table 5:** Pipeline time diagram: usage of branch delay slot techniques to reduce the control hazards.

[illegible]