Tiago Gomes Castro

Brazilian, 35 years old

Actually living in Porto, Portugal Email: tiagogomes.ti@gmail.com

Linkedin: https://www.linkedin.com/in/tiagogomescastro

Degree

• Teleinformatics Engineering with Emphasis at Computers Systems

Conclusion: 2015.2

Federal University of Ceará (UFC)

Professional Experience

- November/2021 Actually: Capgemini Engineering
 - o Location: Porto Portugal
 - o Position: Consultant Advance Engineer
 - Website: https://www.capgemini-engineering.com
 - Main Activities:
 - 1. Embedded Automotive Development Powertrain domain
 - 2. Project's benches maintainer
 - 3. Team technical leader
- January/2021 October/2021: Systronix
 - o Location: Fortaleza/Ceará Brazil
 - o **Position**: Firmware Developer
 - Main Activity: Firmware development of traffic speed measurement devices, using FreeRTOS available on STM32cubelde environment.
- September/2019 January/2021: Eletra Energy Solutions(Hexing Group)
 - o Location: Fortaleza/Ceará Brazil
 - **Position**: Firmware Analyst
 - Website: http://www.eletraenergy.com
 - Main Activity: Firmware developing for a Nic(Network interface card) aiming communication to smart electric meters using LoRa communication protocols.
- April/2017 September/2019: Atlanta Information Technology
 - Location: Fortaleza/Ceará Brazil
 - o **Position**: Firmware Developer
 - Website: https://www.atlantatecnologia.com.br
 - Main Activity: Firmware developing of traffic speed measurement device based on PIC micro controller
- May/2016 March/2017: INPE National Spacial Research Institute
 - o Location: Fortaleza/Ceará Brazil
 - **Position**: Model Based Designer CNPQ Internship

- Website: https://www.gov.br/inpe/pt-br
- Main Activity: Development and implementing, on Xilinx FPGA device, a system to process messages of Brazilian Spacial Data Collect program
- February/2014 September/2015: LESC Computing Systems Engineering Laboratory
 - o **Location**: Fortaleza/Ceará Brazil
 - **Position**: Firmware Developer.
 - Website: http://site.lesc.freeddns.org/
 - Main Activity: Firmware development of a core used to signal processing of analogical telephony system. The code was written in assembly language of proprietary softcore processor made by Siemens.
- July/2010 December/2013: LESC Computing Systems Engineering Laboratory
 - o Location: Fortaleza/Ceará Brazil
 - Website: http://site.lesc.freeddns.org/
 - **Position**: R&D Internship.
 - Main Activity: Research and Development in Networking on Chip (NoC) using VHDL and C as developing languages

Qualifications

- English Level: Actually coursing B2
- Experience at Embedded Systems development
- Experience at ST microelectronics micro controllers projects
- Intermediate experience on FREERTOS
- Git versioning
- Laboratory measurements equipments handling (Oscilloscope, Signals generator, Multimeters, etc...)
- Operational Systems: Linux and Windows.

Courses

• May/2018

Embedded Systems - Shape The World: Micro controller Input/Output

Workload: 40 hours Provider: EDX

Link: https://www.edx.org/es/course/embedded-systems-shape-the-world-microcontroller-in putoutput

• February/2016

Introducing of Embedded Linux

Provider: Professor at University of Nice Sophia-Antipolis (https://www.linkedin.com/in/luc-deneire-7116051)

• September/2010

VHDL Language Workload: 20 Hours

• July/2010

Object Oriented Programming using Java

Workload: 40 Hours.

Extracurricular Experiences

• October/2014

Instructor: VHDL Course Workload: 12 Hours.

• November/2013

Instructor: VHDL Course Workload: 14 Hours.

• August/2013 - November/2013

Teaching Assistance: Computer Systems

• April/2013 - November/2013

Teaching Assistance: Digital Electronic

• April/2013 - July/2013

Teaching Assistance: Microprocessor Systems

October/2013

University meetings 2011 – Federal University from Ceará Work: THOR: A network intra chip for real time systems

Link to resume: http://sysprppg.ufc.br/eu/2011/Resumos/wrappers/MostrarResumo.php?cpf =44100353391&cod=002

Participated as Co-Author

October/2013

University meetings 2011 – Federal University from Ceará

Work: Simulation of intra chip networks using OMNET++

Link to resume: http://sysprppg.ufc.br/eu/2011/Resumos/wrappers/MostrarResumo.php?cpf =44100353391&cod=003

Participated as Co-Author

October/2013

University meetings 2011 - Federal University from Ceará

Work: Generator environment and analysis of intra chip network traffic

 $Link\ to\ resume: \underline{http://sysprppg.ufc.br/eu/2011/Resumos/wrappers/MostrarResumo.php?cpf}$

=44100353391&cod=004 Participated as Co-Author