

Tiago Gomes Castro

Brazilian, 36 years old

Actually living in Porto, Portugal

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Degree

- Teleinformatics Engineering with Emphasis at Computers Systems
Conclusion: 2015.2
Federal University of Ceará (UFC)
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Professional Experience

- **November/2021 - Actually:** Capgemini Engineering
 - **Location:** Porto - Portugal
 - **Position:** Professional B2 Engineer
 - **Website:** <https://www.capgemini-engineering.com>
 - **Main Activities:**
 - Embedded Automotive Development - Powertrain Domain
 - Team technical leader
 - Architecture
 - Development
 - Unit Test
 - Project Benches Maintainer
- **January/2021 - October/2021:** Systronix
 - **Location:** Fortaleza/Ceará - Brazil
 - **Position:** Firmware Developer
 - **Main Activities:**
 - Firmware development to traffic speed measurement devices
 - FREERTOS Firmware development to a STM micro controller
 - Digital signal processing to interpret voltage signal from ADC micro controller interface
- **September/2019 – January/2021:** Eletra Energy Solutions(Hexing Group)
 - **Location:** Fortaleza/Ceará - Brazil
 - **Position:** Firmware Analyst
 - **Website:** <http://www.eletraenergy.com>
 - **Main Activities:**

- Porting from LoRaWAN library to a NiC(Network interface card) interfacing SX1276 LoRa tranceiver and STM32L071cz micro controller
 - Interfaces used in this work: RTC, SPI, UART, Timers, Interrupts, DMA, I2C
 - Used Cosem/DLMS protocols to interface NiC with Electric Smart Meter
- **April/2017 – September/2019: Atlanta Information Technology**
 - **Location:** Fortaleza/Ceará - Brazil
 - **Position:** Firmware Developer
 - **Website:** <https://www.atlantatecnologia.com.br>
 - **Main Activities:**
 - Used digital signal processing methods to interpret a RLC circuit aiming to measure vehicle speed
 - Firmware developing using PIC18F micro controller
- **May/2016 – March/2017: INPE – National Spatial Research Institute**
 - **Location:** Fortaleza/Ceará - Brazil
 - **Position:** Model Based Designer - CNPQ Internship
 - **Website:** <https://www.gov.br/inpe/pt-br>
 - **Main Activity:** Development and implementing, on Xilinx FPGA device, a system to process messages of Brazilian Spatial Data Collect program
- **February/2014 - September/2015: LESC - Computing Systems Engineering Laboratory**
 - **Location:** Fortaleza/Ceará - Brazil
 - **Position:** Firmware Developer.
 - **Website:** <http://site.lesc.freedomdns.org/>
 - **Main Activity:** Firmware development of a core used to signal processing of analogical telephony system. The code was written in assembly language of proprietary softcore processor made by Siemens.
- **July/2010 - December/2013: LESC - Computing Systems Engineering Laboratory**
 - **Location:** Fortaleza/Ceará - Brazil
 - **Website:** <http://site.lesc.freedomdns.org/>
 - **Position:** R&D Internship.
 - **Main Activity:** Research and Development in Networking on Chip (NoC) using VHDL and C as developing languages

Hard Skills

- Experience in C Development
- Beginner/Intermediary in C++ Development
- Using of Python Language to write some scripts
- CMake
- Intermediate knowledge in FREERTOS
- Operational Systems: Linux and Windows.
- ARM Architecture
- STM32 ARM based Micro Controllers
- PIC Micro Controllers
- Git versioning
- Laboratory measurements equipments handling (Oscilloscope, Signals generator, Multimeter, etc...)

- English Level: Actually coursing B2
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Soft Skills

- Problem-solving
 - Teamwork
 - Leadership
 - Attention to detail
 - Time management
 - Interpersonal Skills
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Courses

- **May/2018**
Embedded Systems - Shape The World: Micro controller Input/Output
Workload: 40 hours
Provider: EDX
Link: <https://www.edx.org/es/course/embedded-systems-shape-the-world-microcontroller-in-putoutput>
 - **February/2016**
Introducing of Embedded Linux
Provider: Professor at University of Nice Sophia-Antipolis (<https://www.linkedin.com/in/luc-deneire-7116051>)
 - **September/2010**
VHDL Language
Workload: 20 Hours
 - **July/2010**
Object Oriented Programming using Java
Workload: 40 Hours.
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Extracurricular Experiences

- **October/2014**
Instructor: VHDL Course
Workload: 12 Hours.
- **November/2013**
Instructor: VHDL Course
Workload: 14 Hours.
- **August/2013 – November/2013**
Teaching Assistance: Computer Systems
- **April/2013 – November/2013**
Teaching Assistance: Digital Electronic
- **April/2013 – July/2013**
Teaching Assistance: Microprocessor Systems
- **October/2013**
University meetings 2011 – Federal University from Ceará
Work: THOR: A network intra chip for real time systems
Link to resume: <http://sysprppg.ufc.br/eu/2011/Resumos/wrappers/MostrarResumo.php?cpf>

[=44100353391&cod=002](#)

Participated as Co-Author

- **October/2013**

University meetings 2011 – Federal University from Ceará

Work: Simulation of intra chip networks using OMNET++

Link to resume: <http://sysprppg.ufc.br/eu/2011/Resumos/wrappers/MostrarResumo.php?cpf=44100353391&cod=003>

Participated as Co-Author

- **October/2013**

University meetings 2011 – Federal University from Ceará

Work: Generator environment and analysis of intra chip network traffic

Link to resume: <http://sysprppg.ufc.br/eu/2011/Resumos/wrappers/MostrarResumo.php?cpf=44100353391&cod=004>

Participated as Co-Author