# **Tiago Gomes Castro**

Brazilian, 37 years old

Actually living in Porto, Portugal Email: <u>tiagogomes.ti@gmail.com</u>

Linkedin: <a href="https://www.linkedin.com/in/tiagogomescastro">https://www.linkedin.com/in/tiagogomescastro</a>

GitHub: https://github.com/tiagogomesti

# **Degree**

• Teleinformatics Engineering with Emphasis at Computers Systems

Conclusion: 2015.2

Federal University of Ceará (UFC)

Degree validated in Portugal under 220230069052 registration number. It can

be checked at <a href="https://www.dges.gov.pt/RecOn/Validacao">https://www.dges.gov.pt/RecOn/Validacao</a>

### **Courses**

### October/2023

TESSY 4

Workload: 20h

Provider: Hitex Embedded Tools & Solutions

Certificate Link: <a href="https://bit.ly/Tessy-4-Certificate">https://bit.ly/Tessy-4-Certificate</a>

### October/2023

Functional Safety Training - Modules 1 and 4

Workload: 16h

Provider: TÜV SÜD Rail GmbH

Certificate Link: https://bit.ly/FuSa Training

#### May/2018

Embedded Systems - Shape The World: Micro controller Input/Output

Workload: 40 hours

Provider: EDX

Course Link: <a href="https://www.edx.org/es/course/embedded-systems-shape-the-w">https://www.edx.org/es/course/embedded-systems-shape-the-w</a>

orld-microcontroller-inputoutput

#### • February/2016

Introducing of Embedded Linux

Provider: Professor at University of Nice Sophia-Antipolis (<a href="https://www.linkedi">https://www.linkedi</a>

n.com/in/luc-deneire-7116051)

• September/2010

VHDL Language Workload: 20 Hours

• July/2010

Object Oriented Programming using Java

Workload: 40 Hours.

# **Professional Experience**

- July/2023 Actually: Intellias
  - Location: Porto Portugal
  - Position: Strong Middle Embedded Engineer
  - Website: <a href="https://intellias.com/">https://intellias.com/</a>
  - Main Activities:
    - Automotive Embedded Ultrasonic sensors
      - Detail Design
      - Development
      - Unit Test
- November/2021 July/2023: Capgemini Engineering
  - Location: Porto Portugal
  - **Position**: Professional B2 Engineer
  - Website: <a href="https://www.capgemini-engineering.com">https://www.capgemini-engineering.com</a>
  - Main Activities:
    - Automotive Embedded HMI Domain
      - Team technical leader
      - Detail Design
      - Development
      - Unit Test
    - Automotive Embedded Development Powertrain Domain
      - Team technical leader
      - Development
      - Unit Test
    - Project Benches Maintainer
- January/2021 October/2021: Systronix
  - **Location**: Fortaleza/Ceará Brazil
  - **Position**: Firmware Developer

#### • Main Activities:

- Firmware development to traffic speed measurement devices
- FREERTOS Firmware development to a STM micro controller
- Digital signal processing to interpret voltage signal from ADC micro controller interface
- September/2019 January/2021: Eletra Energy Solutions(Hexing Group)
  - Location: Fortaleza/Ceará Brazil
  - **Position**: Firmware Analyst
  - Website: <a href="http://www.eletraenergy.com">http://www.eletraenergy.com</a>
  - Main Activities:
    - Porting from LoRaWAN library to a NiC(Network interface card) interfacing SX1276 LoRa transceiver and STM32l071cz micro controller
      - Interfaces used in this work: RTC, SPI, UART, Timers, Interrupts, DMA, I2C
    - Used Cosem/DLMS protocols to interface NiC with Electric Smart Meter
- April/2017 September/2019: Atlanta Information Technology
  - Location: Fortaleza/Ceará Brazil
  - **Position**: Firmware Developer
  - Website: https://www.atlantatecnologia.com.br
  - Main Activities:
    - Used digital signal processing methods to interpret a RLC circuit aiming to measure vehicle speed
    - Firmware developing using PIC18F micro controller
- May/2016 March/2017: INPE National Spacial Research Institute
  - Location: Fortaleza/Ceará Brazil
  - **Position**: Model Based Designer CNPQ Internship
  - Website: https://www.gov.br/inpe/pt-br
  - Main Activity: Development and implementing, on Xilinx FPGA device, a system to process messages of Brazilian Spacial Data Collect program
- February/2014 September/2015: LESC Computing Systems Engineering Laboratory
  - Location: Fortaleza/Ceará Brazil
  - **Position**: Firmware Developer.
  - Website: <a href="http://site.lesc.freeddns.org/">http://site.lesc.freeddns.org/</a>

- Main Activity: Firmware development of a core used to signal processing
  of analogical telephony system. The code was written in assembly
  language of proprietary softcore processor made by Siemens.
- July/2010 December/2013: LESC Computing Systems Engineering Laboratory

• **Location**: Fortaleza/Ceará - Brazil

• Website: <a href="http://site.lesc.freeddns.org/">http://site.lesc.freeddns.org/</a>

• **Position**: R&D Internship.

• **Main Activity**: Research and Development in Networking on Chip (NoC) using VHDL and C as developing languages

### **Hard Skills**

- Experience in C Embedded Development
- Beginner/Intermediary in C++ Development
- Python Language to write tests scripts when necessary
- CMake
- Intermediate knowledge in FREERTOS
- Operational Systems: Linux and Windows.
- ARM Architecture
- STM32 ARM based Micro Controllers
- PIC Micro Controllers
- Git versioning
- SVN versioning
- Laboratory measurements equipments handling (Oscilloscope, Signals generator, Multimeter, etc...)
- English Level: B2

### **Soft Skills**

- Problem-solving
- Teamwork
- Leadership
- Attention to detail
- Time management
- Interpersonal Skills

## **Extracurricular Experiences**

### • October/2014

Instructor: VHDL Course Workload: 12 Hours.

### • November/2013

Instructor: VHDL Course Workload: 14 Hours.

### • August/2013 - November/2013

Teaching Assistance: Computer Systems

#### • April/2013 - November/2013

Teaching Assistance: Digital Electronic

### • April/2013 - July/2013

Teaching Assistance: Microprocessor Systems

#### October/2013

University meetings 2011 – Federal University from Ceará

Work: THOR: A network intra chip for real time systems

Link to resume: <a href="http://sysprppg.ufc.br/eu/2011/Resumos/wrappers/MostrarRes">http://sysprppg.ufc.br/eu/2011/Resumos/wrappers/MostrarRes</a>

umo.php?cpf=44100353391&cod=002

Participated as Co-Author

### October/2013

University meetings 2011 – Federal University from Ceará

Work: Simulation of intra chip networks using OMNET++

Link to resume: <a href="http://sysprppg.ufc.br/eu/2011/Resumos/wrappers/MostrarRes">http://sysprppg.ufc.br/eu/2011/Resumos/wrappers/MostrarRes</a>

<u>umo.php?cpf=44100353391&cod=003</u>

Participated as Co-Author

### October/2013

University meetings 2011 – Federal University from Ceará

Work: Generator environment and analysis of intra chip network traffic

Link to resume: <a href="http://sysprppg.ufc.br/eu/2011/Resumos/wrappers/MostrarResumo.php?cpf=44100353391&cod=004">http://sysprppg.ufc.br/eu/2011/Resumos/wrappers/MostrarResumo.php?cpf=44100353391&cod=004</a>

Participated as Co-Author