Ergonomic C/C++ source-to-source analysis and transformations for HLS using Clava

35th ACM SIGDA/IEEE CEDA University Demonstration at Design Automation Conference (UDDAC 2025) June 22-25, San Francisco, California, USA

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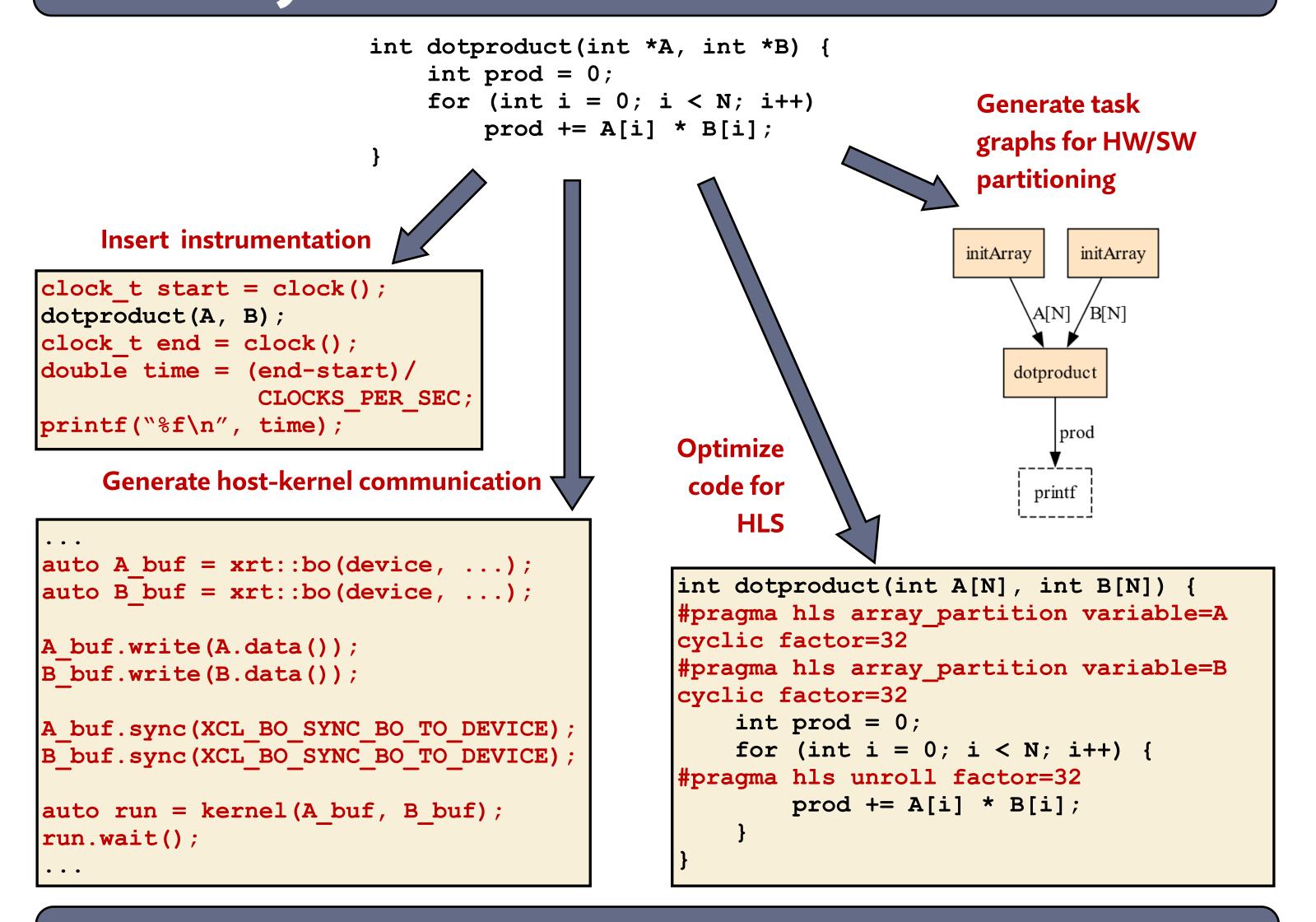
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Why source-to-source for HLS?



Why Clava?







High productivity

High composability

A single, flexible AST



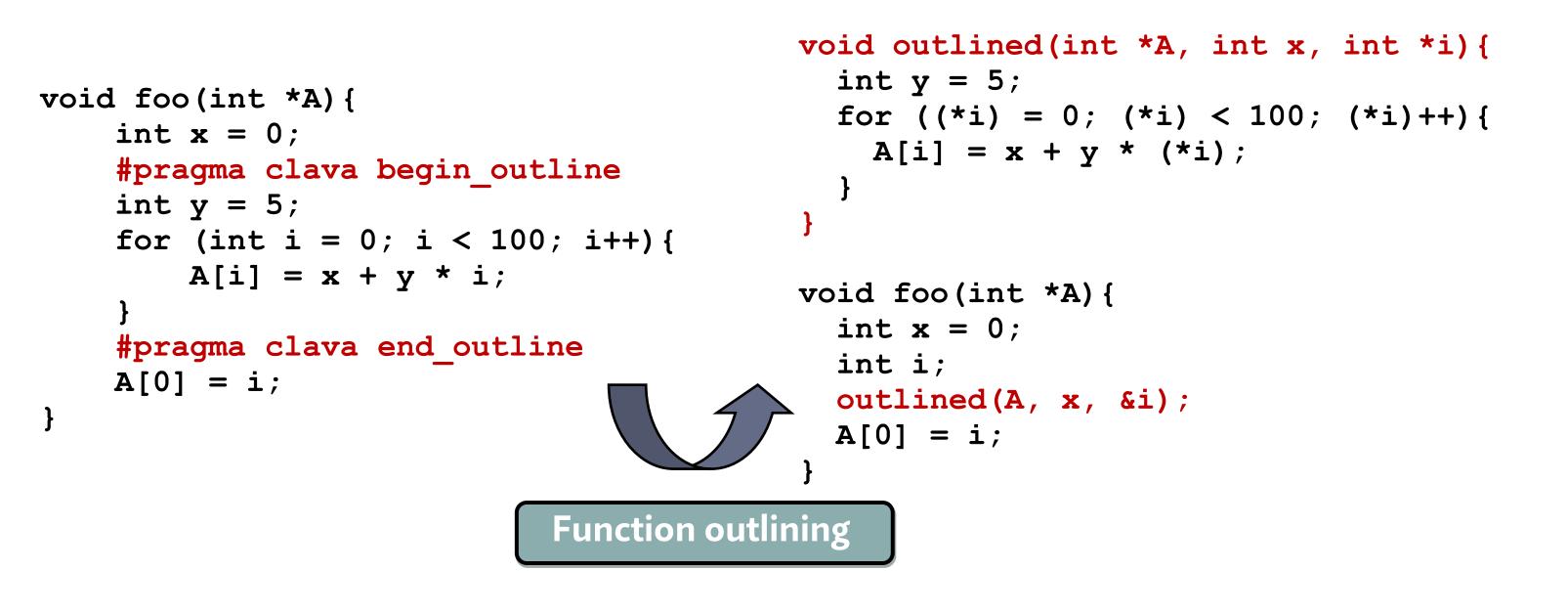


AST-based transformations Easily reuse, distribute and view the whole input combine analysis passes and program as a single cohesive transformations through entity, abstracting the notion NPM of file/translation unit

Write transformations using modern JIT-compiled

languages (JavaScript or TypeScript)

Demo: generating task graphs



Demo: code transformations

Array flattening

Struct flattening

Function inlining

Call hoisting

Reduction to a C subset

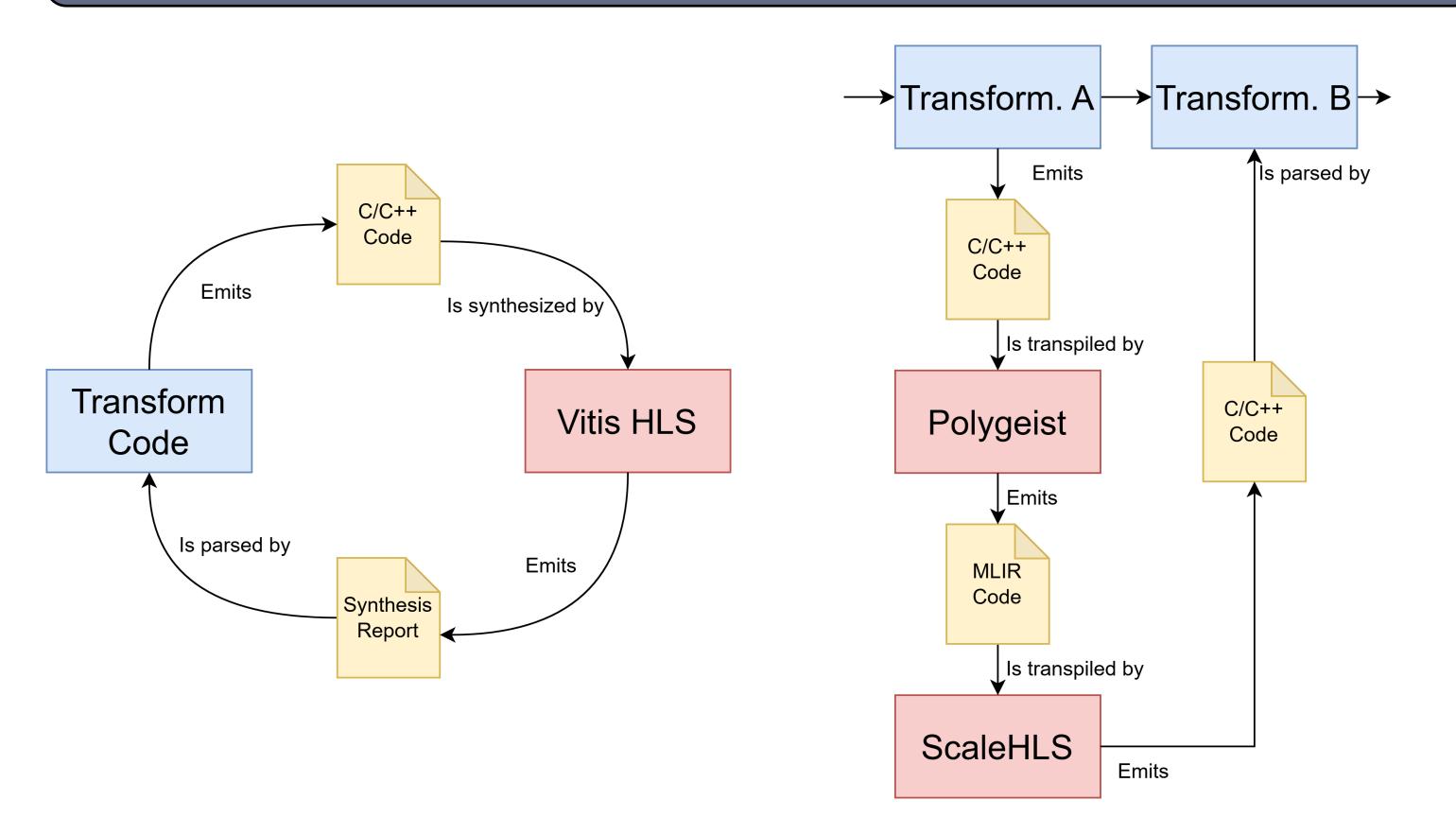
Single file amalgamation

void edge_detect(int image_rgb[H][W * 3], TSrc: <task_graph_source> int image_gray[H][W], int temp_buf[H][W], int filter[K][K], int output[H][W]) rgbToGrayscale(image_rgb, image_gray); T0.1: setFilter filter[0][0] = 1; //... filter[2][2] = 1; T0.3: setFilter T0.0: rgbToGrayscale convolve2d(image gray, filter, output); filter[0][0] = 1; T0.2: convolve2d T0.5: setFilter //... filter[2][2] = -1;T0.6: convolve2d_ T0.4: convolve2d_ convolve2d(output, filter, image gray); filter[0][0] = 1; //... T0.7: combthreshold filter[2][2] = -1; convolve2d(output, filter, temp buf);

combthreshold(image_gray, temp_buf, output);

++++ TSink: <task_graph_sink>

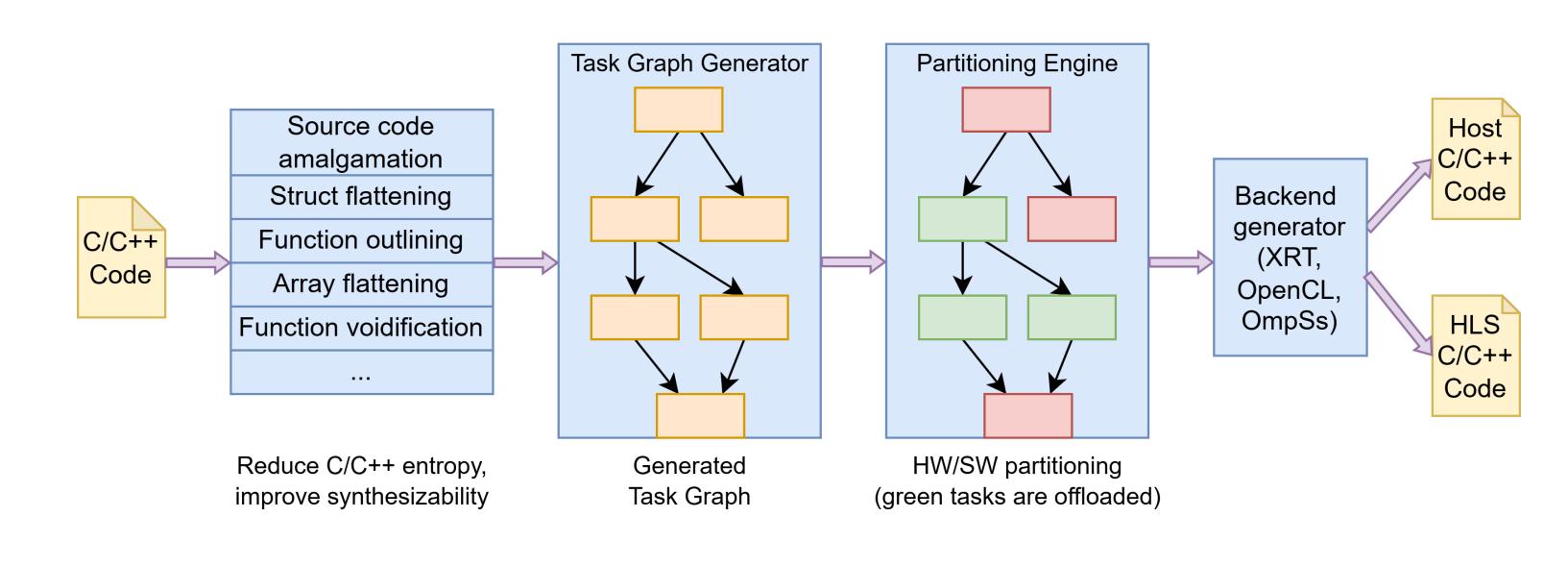
Demo: integration with HLS tools



Design-space-exploration using Vitis HLS

Seamless HLS optimization using ScaleHLS

Demo: full HW/SW partitioning flow



By combining the code optimizations, task graph generation, and HLS tools packages with a partitioning algorithm and backend generator, we can compose a full CPU-FPGA HW/SW partitioning and optimization flow for a C/C++ application