

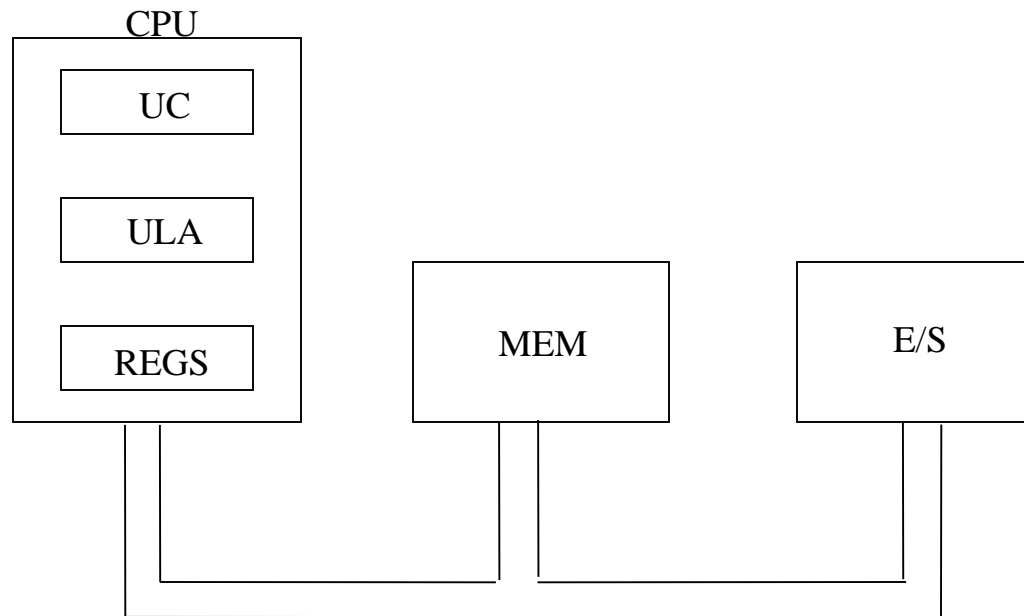
UNIOESTE – Universidade Estadual do Oeste do Paraná
Centro de Engenharias e Ciências Exatas
Campus de Foz do Iguaçu

Arquitetura MIPS

Prof.: Fabiana Frata Furlan Peres

Foz do Iguaçu

Organização Interna de um Computador



Formato das Instruções

- Formato R:

<i>op</i>	<i>rs</i>	<i>rt</i>	<i>rd</i>	<i>shamt</i>	<i>funct</i>
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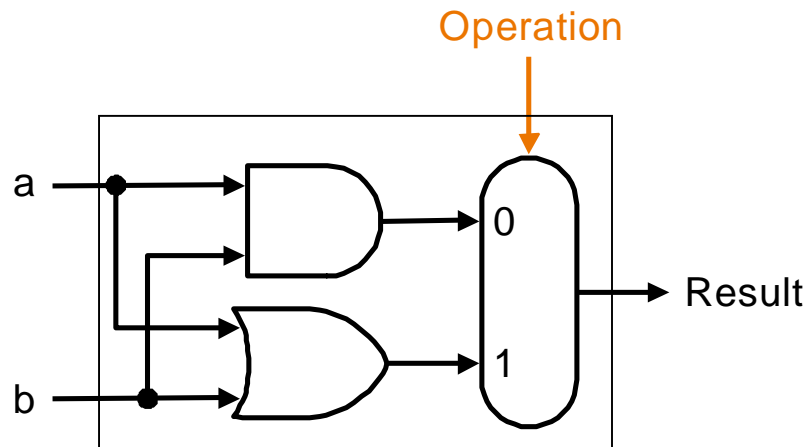
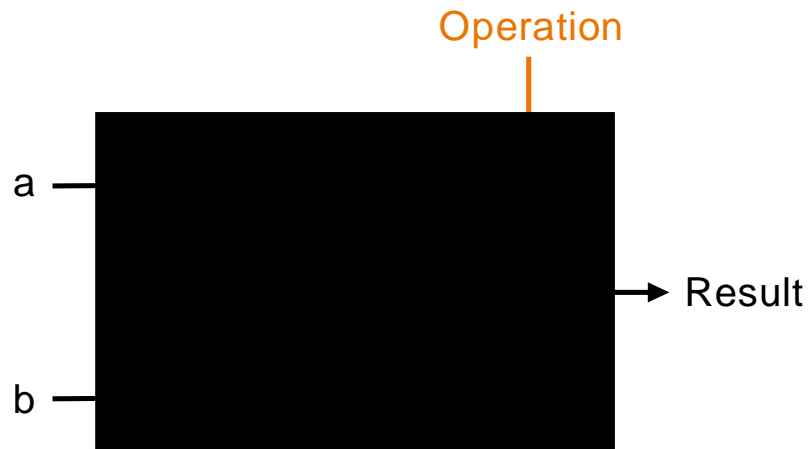
- Formato I:

<i>op</i>	<i>rs</i>	<i>rt</i>	<i>const/end</i>
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- Formato J:

<i>op</i>	<i>end</i>
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Implementação da ULA (operações de AND e OR)



Multiplexador com 8 entradas

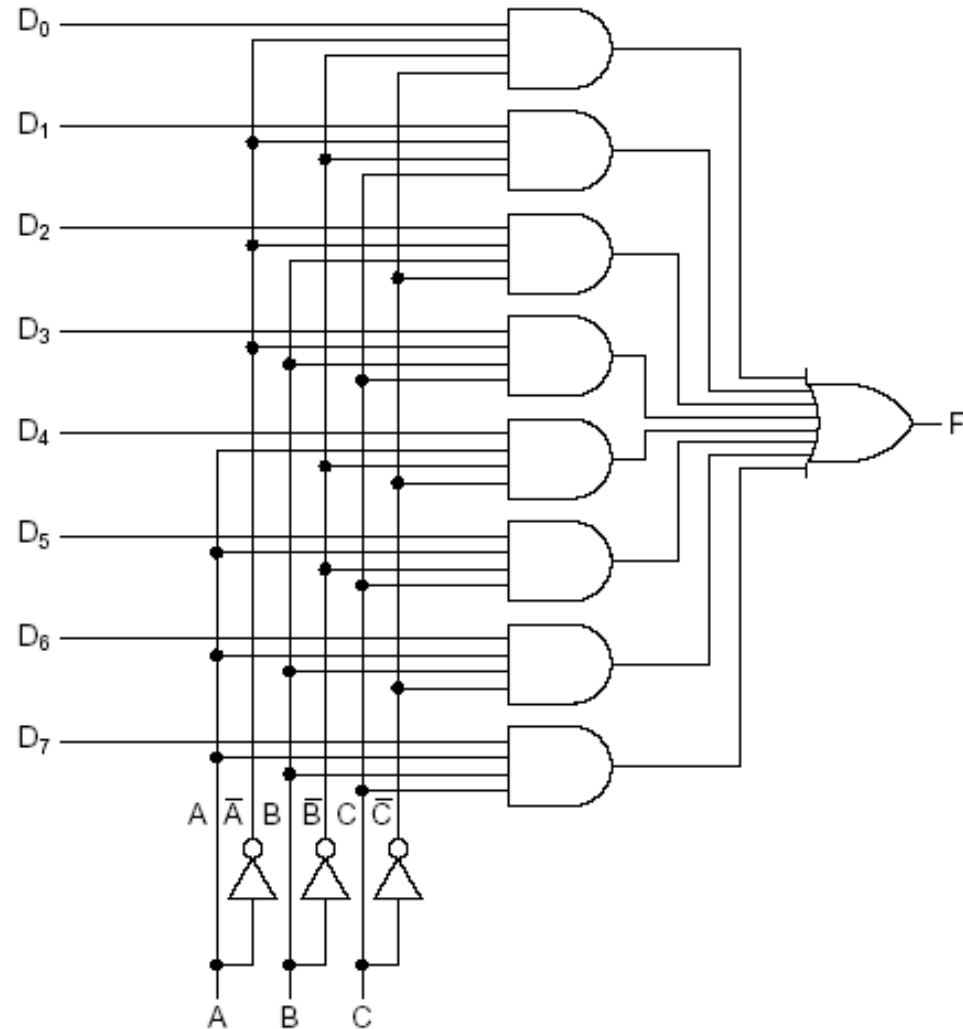


Figure 3-11. An eight-input multiplexer circuit.

Decodificador 3x8

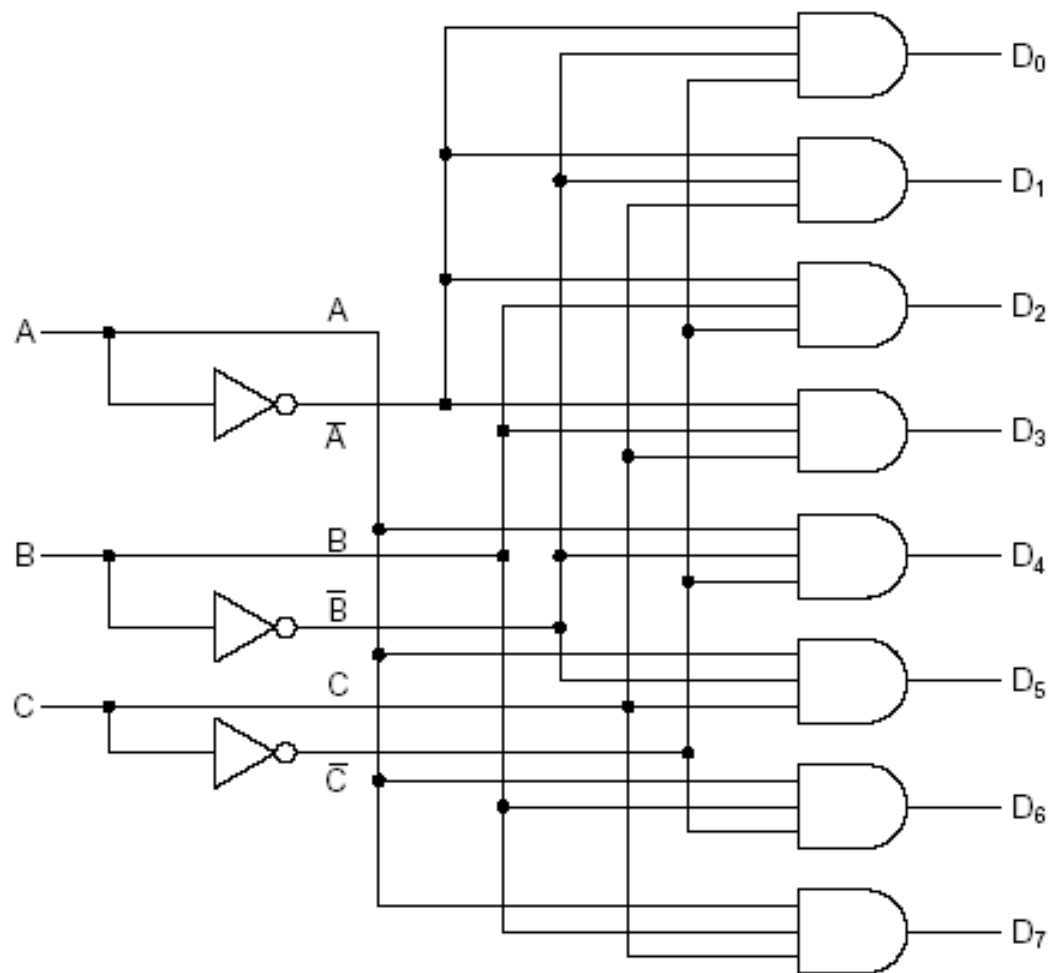
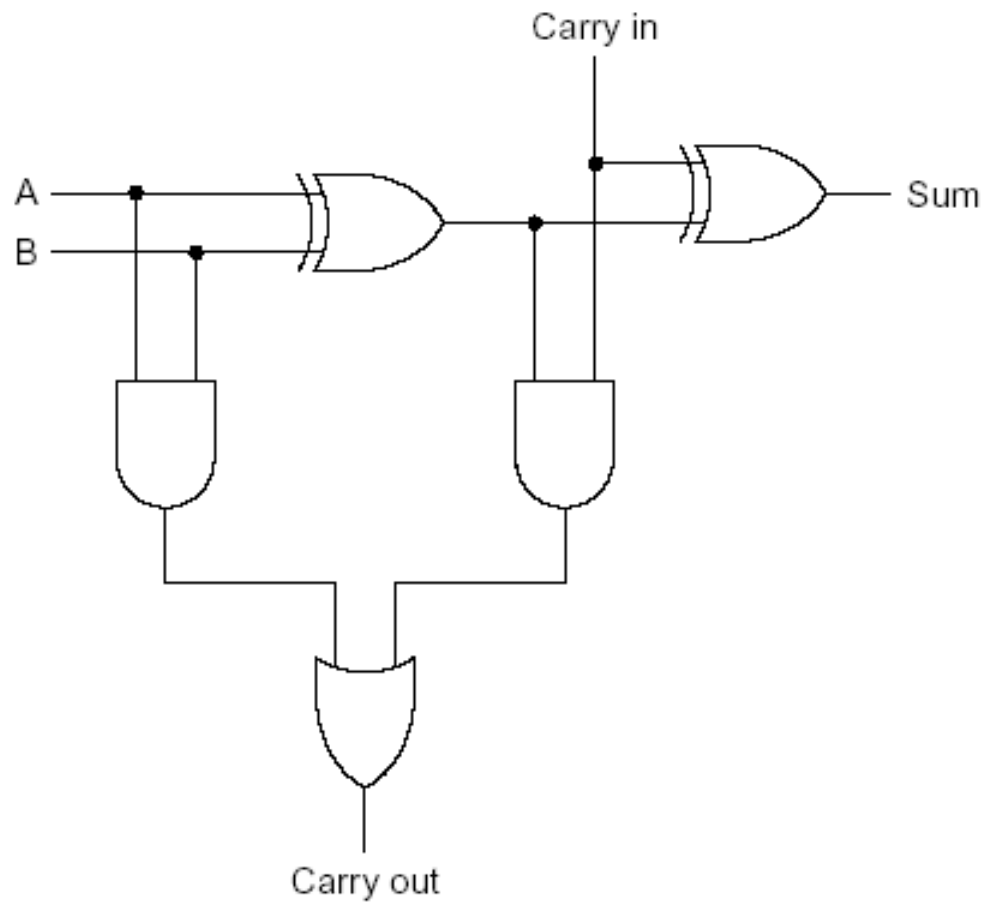


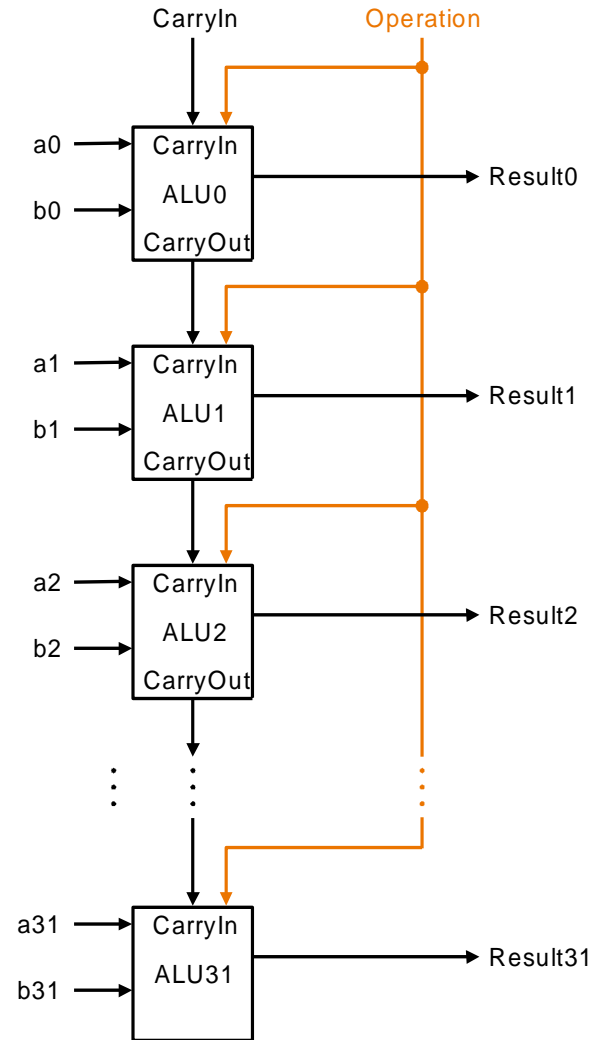
Figure 3-13. A 3-to-8 decoder circuit.

Implementação da ULA (operação de soma com 1 bit)



Implementação da ULA

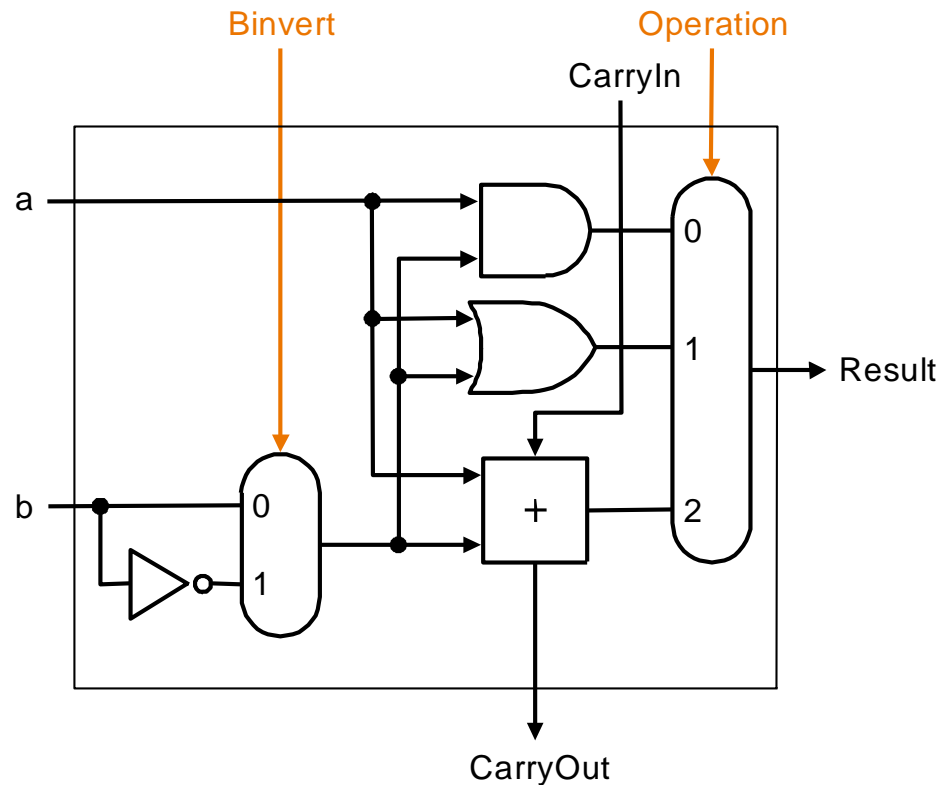
(operação de soma com 32 bits)



Implementação da ULA

(operação de soma, subtração, AND e OR)

- $a - b \Rightarrow a + (-b) \Rightarrow a + \bar{b} + 1$



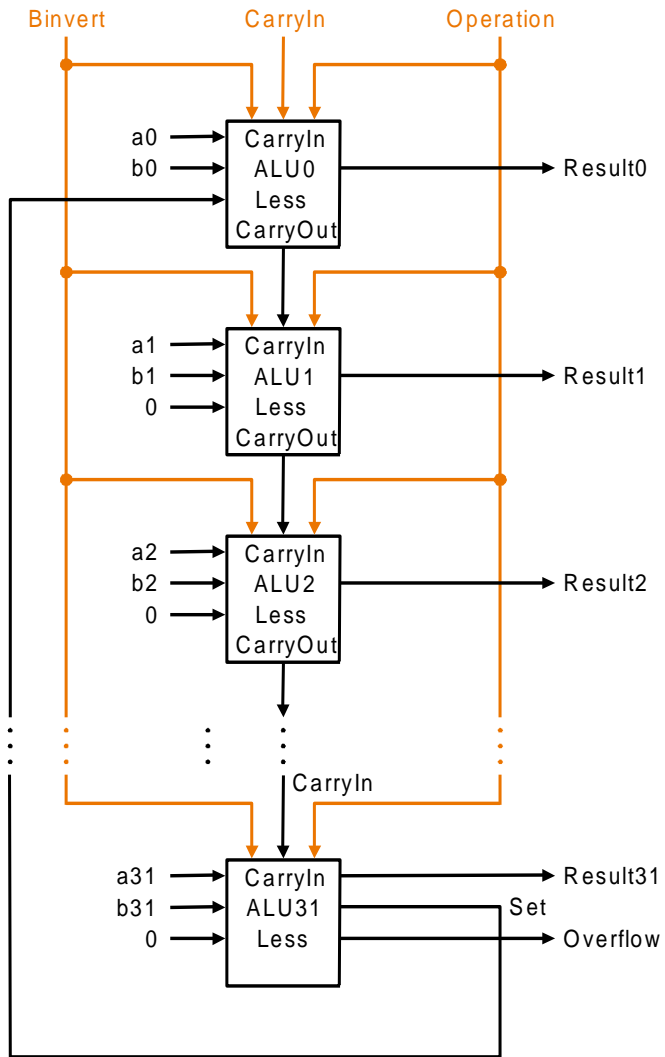
Implementação da ULA (operação de slt)

- slt c, a, b //if $a < b$ then $c=1$; else $c=0$;
1) se $a-b = \text{numero negativo}$ then $c=1$;
2) se $a-b = \text{numero positivo}$ then $c= 0$;

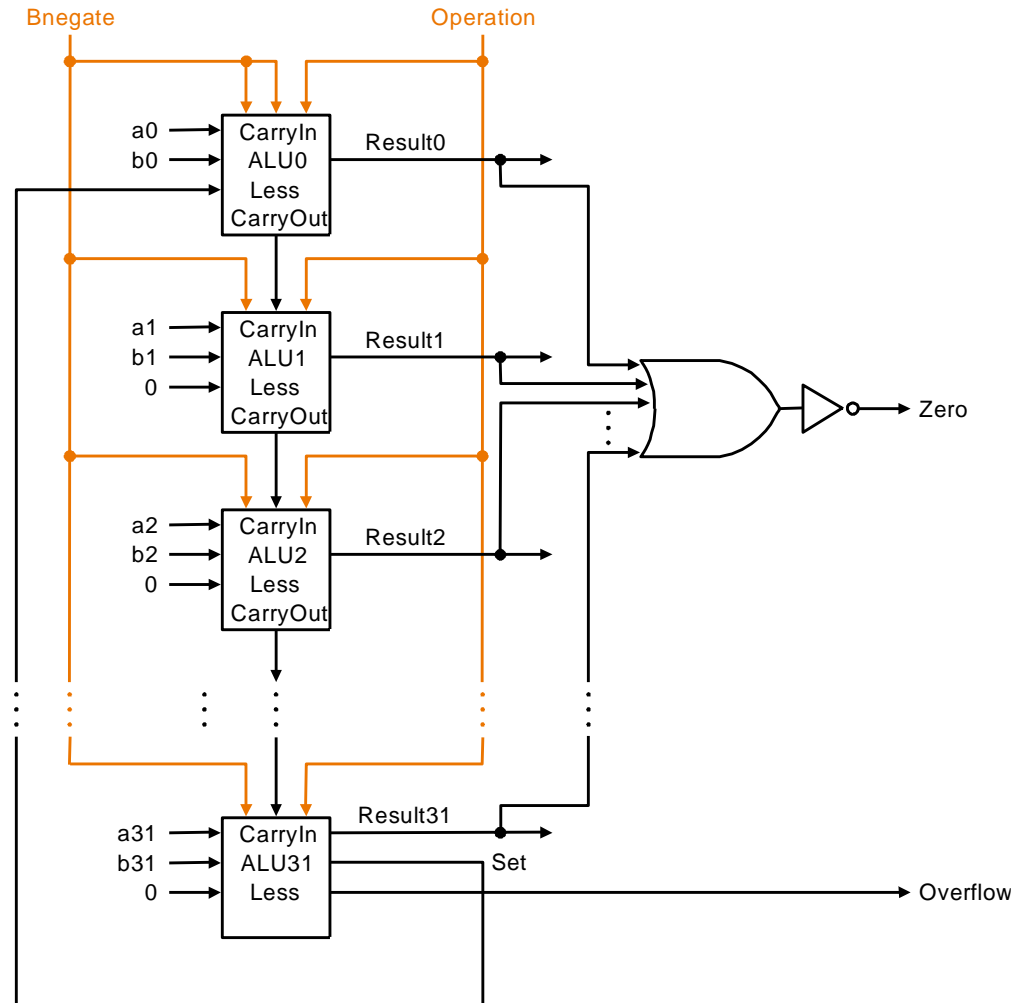
Implementação da ULA (executa operação de slt)



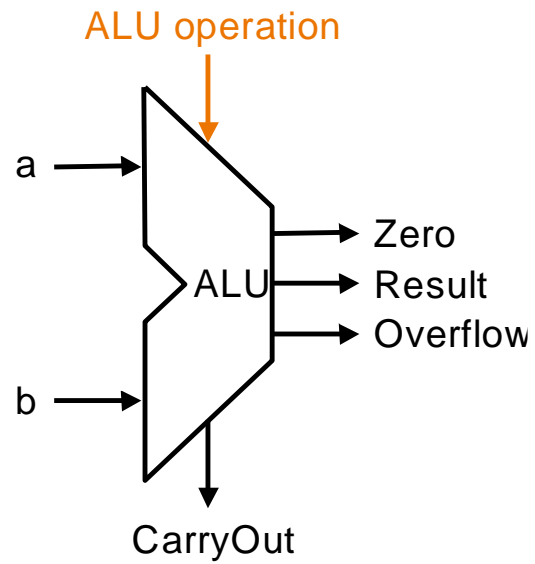
Implementação da ULA (operação de slt)



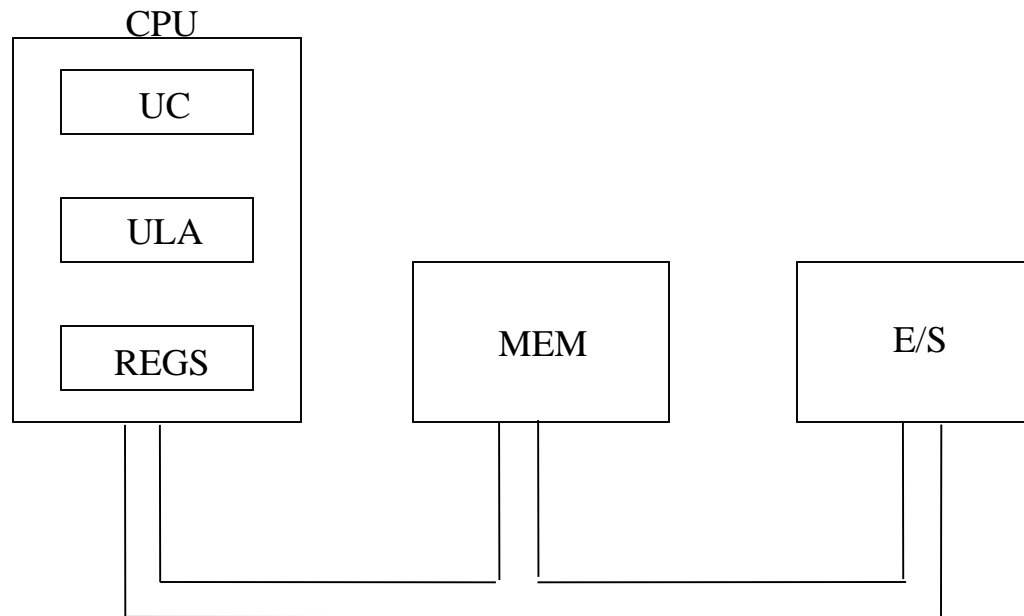
Implementação da ULA



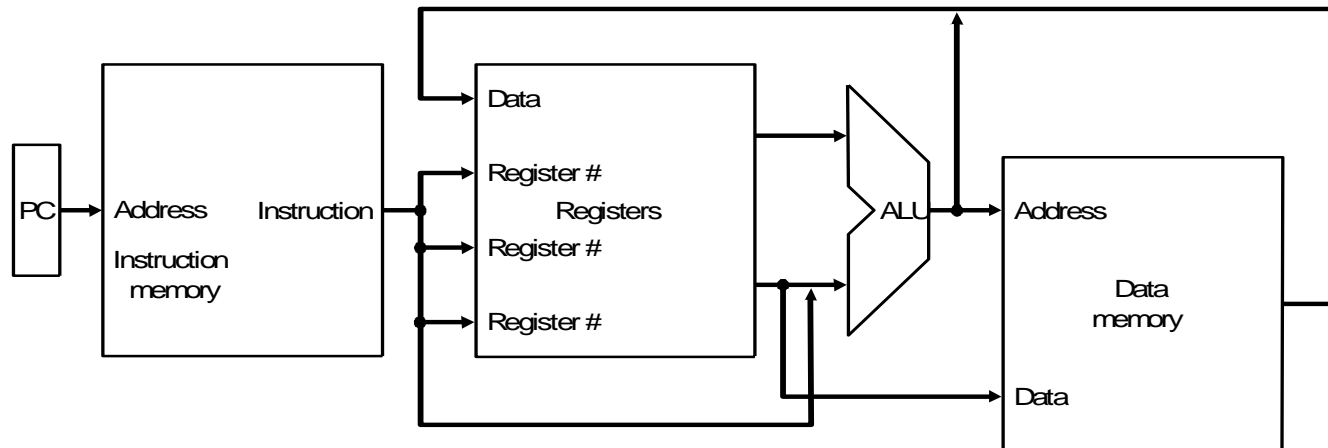
Implementação da ULA



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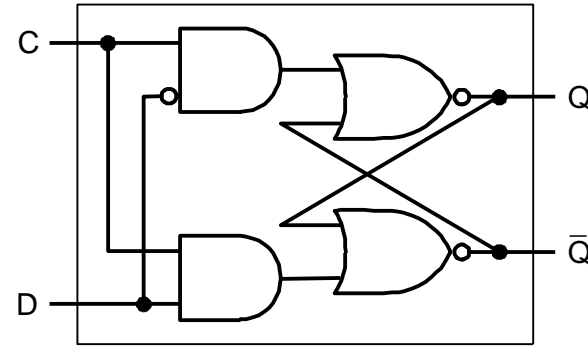


Visão abstrata da Implementação do Sub conjunto da MIPS

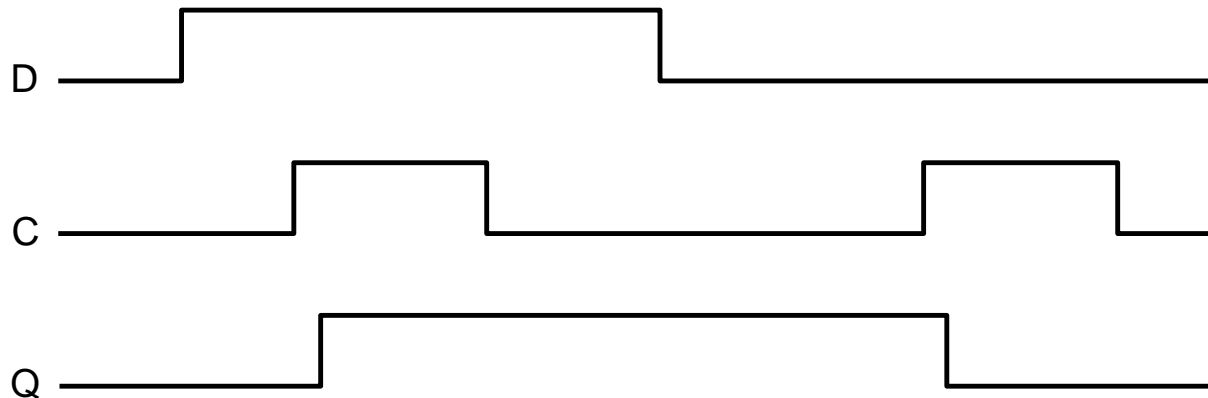


Implementação do conjunto de Registradores

- Estrutura básica:
 - Latches

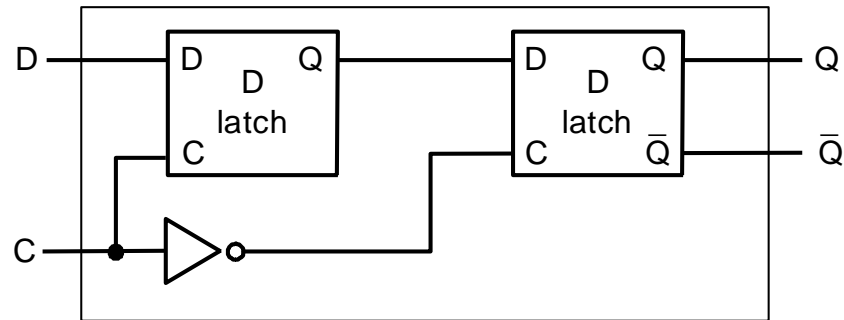


- O estado muda sempre que a entrada mudar e o sinal de clock estiver ativo;

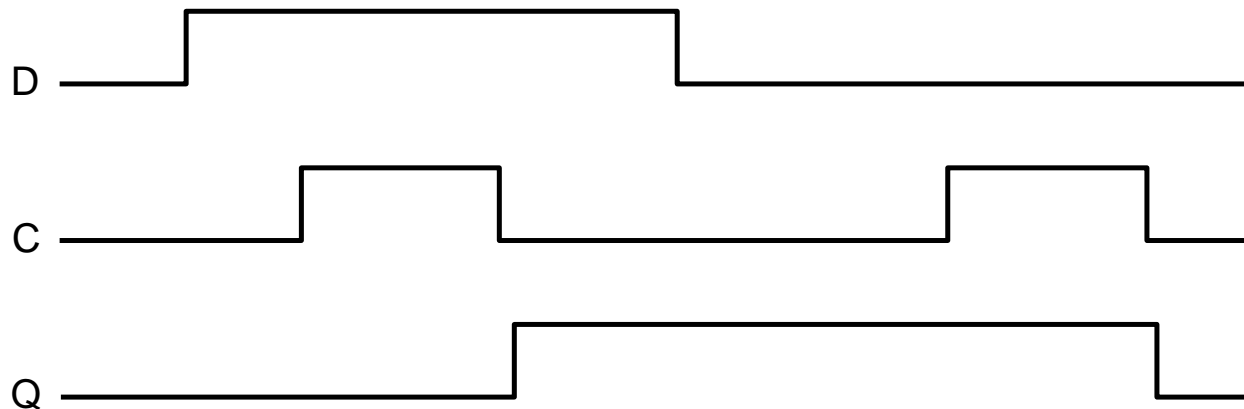


Implementação do conjunto de Registradores

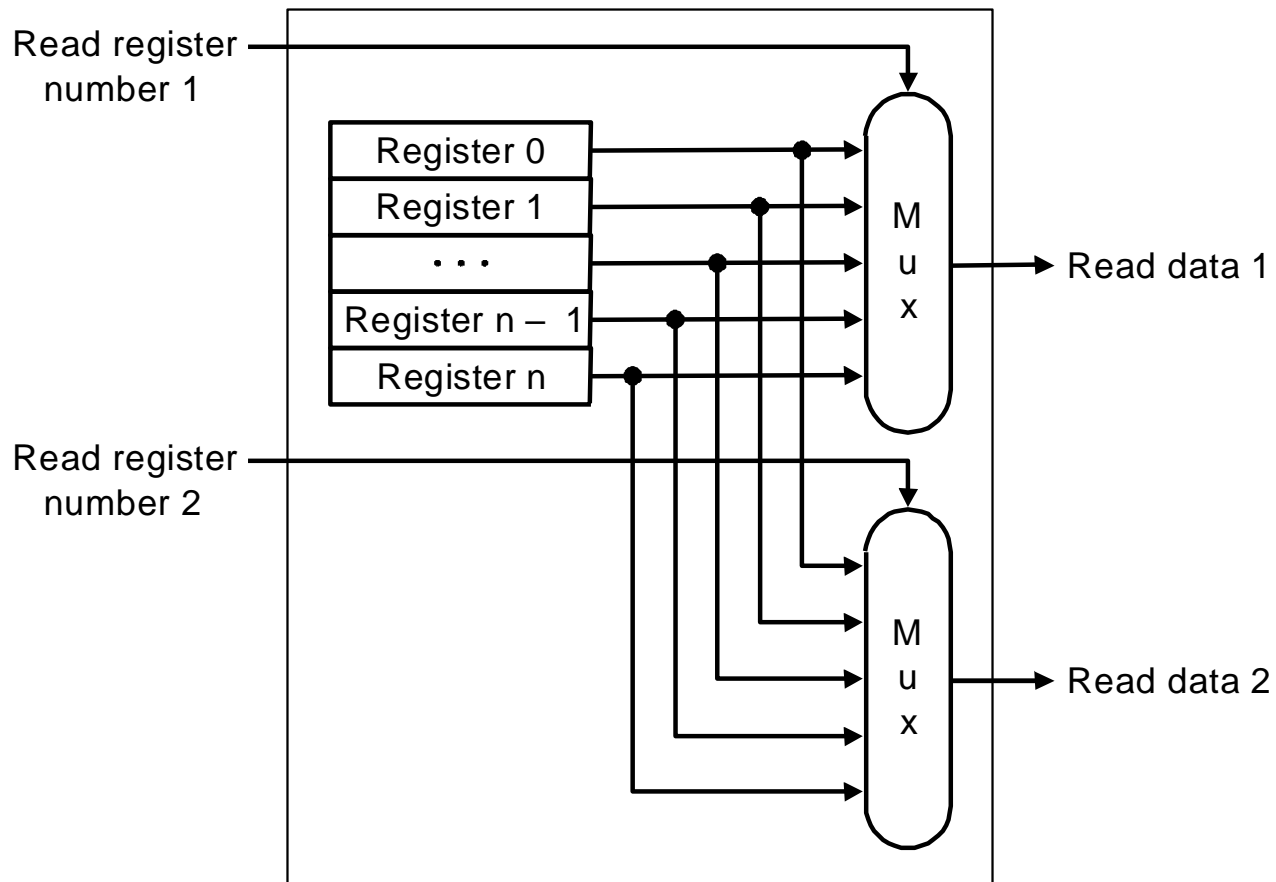
- Estrutura básica:
 - flip-flops



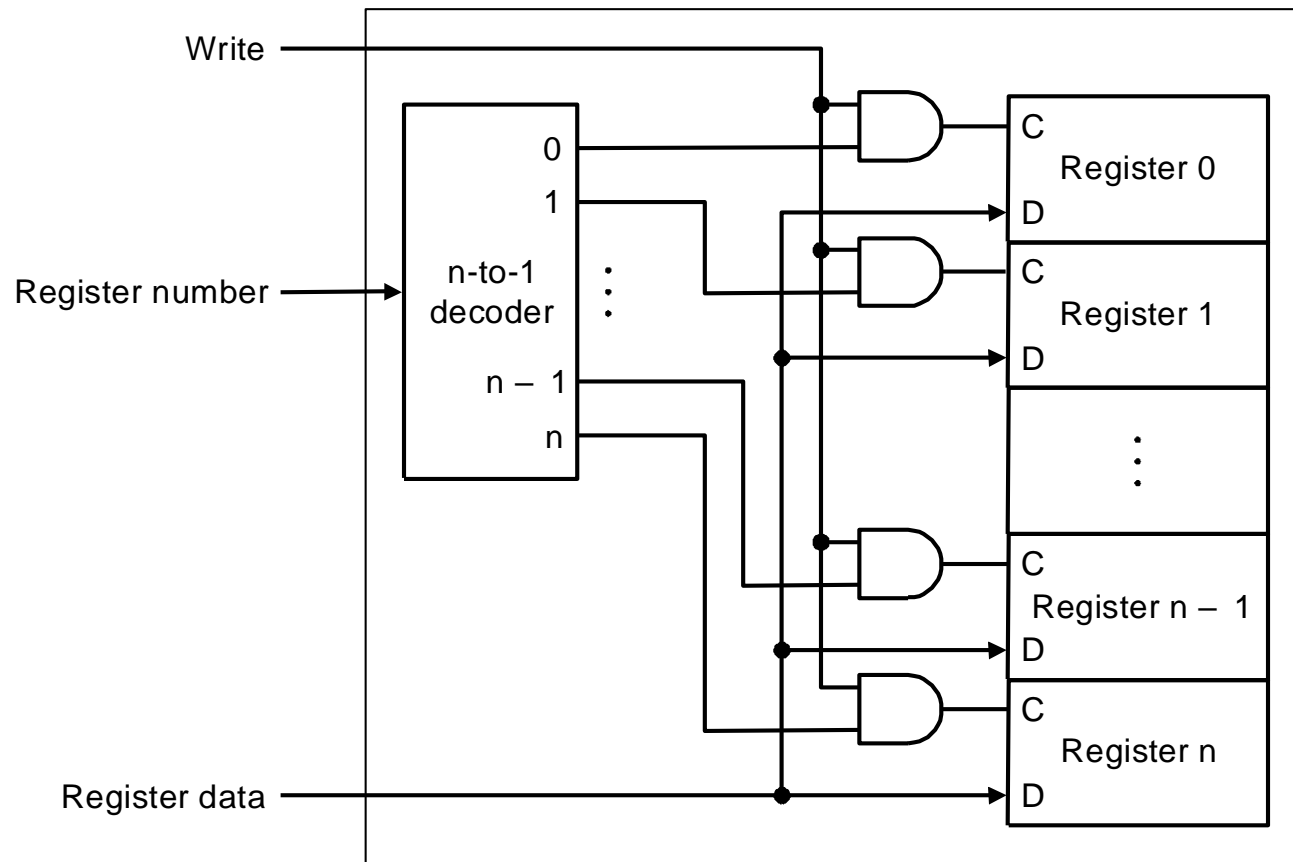
- o estado muda somente na transição do clock



Implementação do conjunto de Registradores (leitura)



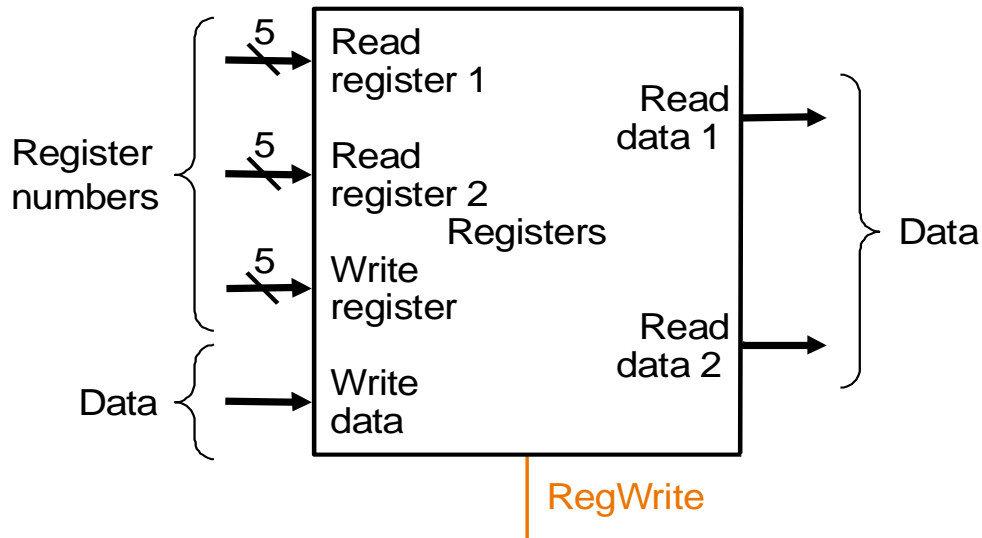
Implementação do conjunto de Registradores (escrita)



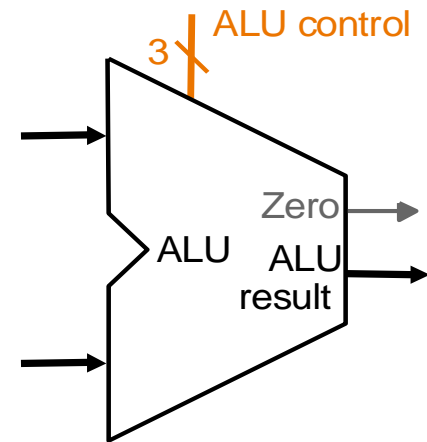
The diagram illustrates a 4x32-bit parallel adder implemented with D flip-flops and 3-to-8 decoders. The circuit has four data inputs (I_2, I_1, I_0 and an implied I_3), four data outputs (O_1, O_2, O_3 and an implied O_0), and four word select lines (A_1, A_0 and two implied lines). The control signals are CS (Chip Select), RD (Read Enable), and OE (Output Enable). The circuit is organized into four rows, each representing a word (Word 0 to Word 3). Each row contains three D flip-flops, each with a clock input (CK) and a data input (D). The data inputs are connected to the flip-flops through a network of 3-to-8 decoders and AND gates. The output of each flip-flop is connected to the data outputs through a network of 3-to-8 decoders and OR gates. The output enable signal is calculated as $Output\ enable = CS \cdot RD \cdot OE$.

Figure 3-29. Logic diagram for a 4×3 memory. Each row is one of the four 3-bit words. A read or write operation always reads or writes a complete word.

Elementos necessários para a implementação do Sub conjunto da MIPS



a. Registers



b. ALU