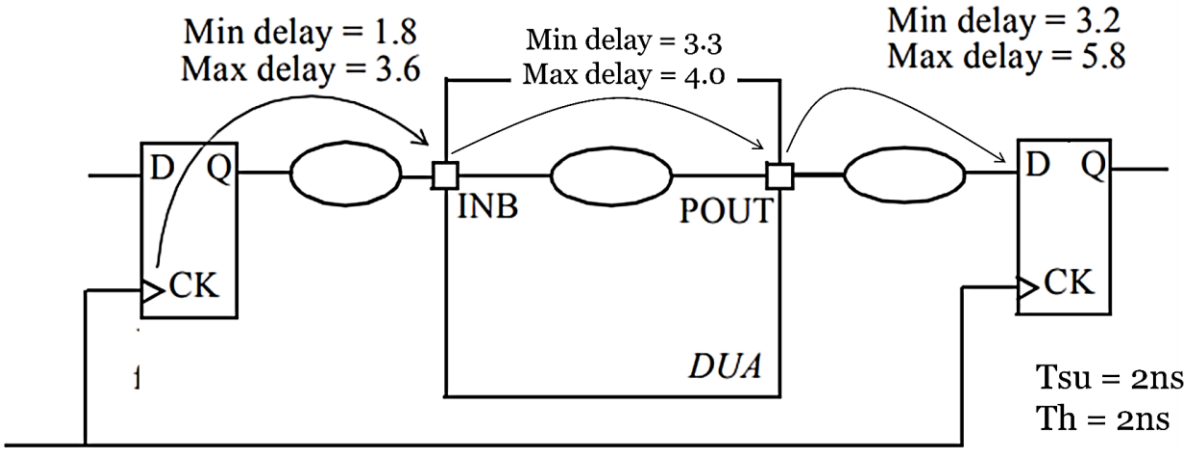
NYU Tandon School of Engineering

Spring 2023, ECE 6443

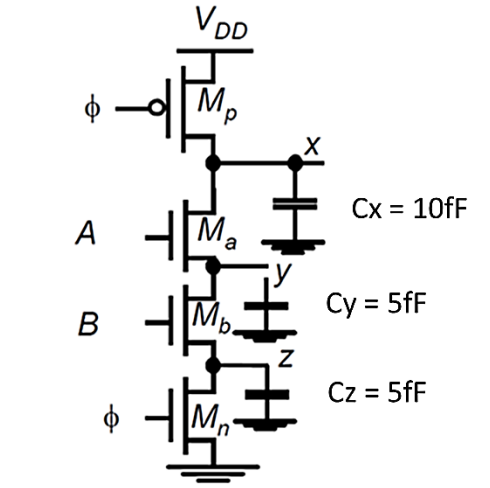
Midterm April 11th 2023

This Test has 3 Problems. Please answer all of them in the Blue Examination Notebook provided. Please capture your notebook pages in a PDF and upload the PDF to Brightspace as you would an assignment. *Please be sure to turn in the Examination Notebook with your netID and name before you leave the Classroom today*.

1. (i) Determine the Minimum Cycle Time required for the Schematic shown below (ii) Identify regions on the timing diagram that INB and POUT cannot change and must be stable. Assume Period of the CLK equals 50ns



2. In this Dynamic N-Tree Gate, the supply voltage equals 0.9V.
   If A, B = 0 during Precharge phase and both transition to '1' during Evaluate phase of the Clock, determine the voltages of X, Y and Z. What is the maximum leakage that can be tolerated assuming a cycle time of 1ns if A, B = 0 during the evaluate phase and the logic threshold of the inverter driven by this gate is 0.7V?



3. Write the Verilog module for a 4b multiplier and write a test bench to verify your 4b multiplier module works