Tianhua Xia

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EDUCATION

University of Illinois at Urbana-Champaign **August 2019~December 2020**
Master of Engineering in Electrical and Computer Engineering 3.74/4.0

Beijing Institute of Technology **September 2015~June 2019**
Bachelor of Science in Electrical Engineering 86/100

University of California, Berkeley Extension **August 2018~May 2019**
Berkeley Global Access Program Visiting Student

WORK EXPERIENCE

Qualcomm Technologies, Inc

Engineer, SoC Low Power Management *04/2022~Present*

- Modeled the behavior of a hardware DVFS algorithm for power and performance analysis.
- Micro architected and developed RTL for SoC level power control system to support chiplet architecture.
- Conducted functional safety analysis and implemented safety mechanisms for automotive SoC.
- Automated RTL code generation and development flows using Python and Bash scripts.

Rotation Engineer, System Cache *10/2021~04/2022*

- Micro architected and developed RTL for cache blocks, provided essential verification and debugging activities.
- Analyzed cache power using Power-Artist and applied clock gating techniques for improvement.

Rotation Engineer, SoC Power *04/2021~10/2021*

- Developed Python and Bash scripts to automate several customized SoC power flow checks.
- Generated and analyzed UPFs of different SoC tiles for power intent check.

RESEARCH EXPERIENCE

Softmax Acceleration with Adaptive Numeric Format for both Training and Inference Advisor: Prof. Sai Qian Zhang
https://arxiv.org/abs/2311.13290 *07/2023~11/2023*

- Proposed an adaptive numeric format architecture which supports floating point Softmax with reduced resource.
- Proposed a reconfigurable division/multiplication unit to enable Softmax training calculation for Transformers.
- Implemented our design in TensorFlow to help model accuracy validation.
- The accelerator reduced 15 times in hardware utilization and 20 times in latency with negligible accuracy impact.

GPU Accelerated Slicing Algorithm for High Resolution 3D Printing Advisor: Prof. Rakesh Kumar
University of Illinois at Urbana-Champaign *10/2020~04/2021*

- Analyzed bottlenecks of existing 3D printing technologies and slicing algorithms for high resolution, large models.
- Implemented the CPU and GPU (CUDA C) version of a Pixelwise Parallel Slicing algorithm as research baseline.
- Accelerated the proposed algorithm in customized hardware using Vivado HLS tools.

Lateral Superior Olive Based Spatial Mapping System Advisor: Prof. Anu Aggarwal
University of Illinois at Urbana-Champaign *06/2020~12/2020*
2021 Conference of the IEEE Engineering in Medicine and Biology Society (EMBC) workshop

- Replicated a circuit to mimic the response of synapse neuron based on conductance incident on it.
- Implemented an electronic lateral superior olive (LSO) column circuit with an array of 32 neurons.
- Architected the mapping between the positions of obstacles and the response of the LSO column circuit.

PROJECT EXPERIENCE

Software Hardware Co-Design of Accelerators *02/2020~05/2020*

- Implemented LeNet in C++ and generated RTL codes using Vivado HLS for hardware acceleration.
- Implemented a stack of communication Ips (ARP, IPv4, UDP, etc.) using HLS.
- Integrated the accelerators with a ZYNQ7 processing system to execute them in FPGA.

Design of a 5 Stage Pipelined RISC-V CPU *09/2019~12/2019*

- Designed a 2-way set-associative cache and decreased the delay of memory execution.
- Increased the CPU to 5-stage pipeline and increased the working frequency.
- Implemented a fast multiplier and divider to extend RISC-V ISA.

OTHER INFORMATION

Programming Language: System Verilog, Verilog, Python, MATLAB, Simulink, C.