Agilent Technologies
Innovating the HP Way

Small Outline, 5 Lead, High CMR, High Speed, Logic Gate Optocouplers

Technical Data

HCPL-M600
HCPL-M601
HCPL-M611

Features

- **Surface Mountable**
- **Very Small, Low Profile JEDEC Registered Package Outline**
- **Compatible with Infrared Vapor Phase Reflow and Wave Soldering Processes**
- **Internal Shield for High Common Mode Rejection (CMR)**
  HCPL-M601: 10,000 V/µs at V_{CM} = 50 V
  HCPL-M611: 15,000 V/µs at V_{CM} = 1000 V
- **High Speed: 10 Mbd**
- **LSTTL/TTL Compatible**
- **Low Input Current Capability: 5 mA**
- **Guaranteed ac and dc Performance over Temperature: -40°C to 85°C**
- **Recognized under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltage of 2500 Vac, 1 Minute**

Description

These small outline high CMR, high speed, logic gate optocouplers are single channel devices in a five lead miniature footprint. They are electrically equivalent to the following Agilent optocouplers (except there is no output enable feature):

SO-5 Package	Standard DIP	SO-8 Package
HCPL-M600	6N137	HCPL-0600
HCPL-M601	HCPL-2601	HCPL-0601
HCPL-M611	HCPL-2611	HCPL-0611

The SO-5 JEDEC registered (MO-155) package outline does not require "through holes" in a PCB. This package occupies approximately one fourth the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

The HCPL-M600/01/11 optically coupled gates combine a GaAsP light emitting diode and an integrated high gain photon detector. The output of the detector I.C. is an Open-collector Schottky-clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 5,000 V/µs for the HCPL-M601, and 10,000 V/µs for the HCPL-M611.

This unique design provides maximum ac and dc circuit isolation while achieving TTL compatibility. The optocoupler ac and dc operational parameters are guaranteed from -40°C to 85°C allowing trouble free system performance.

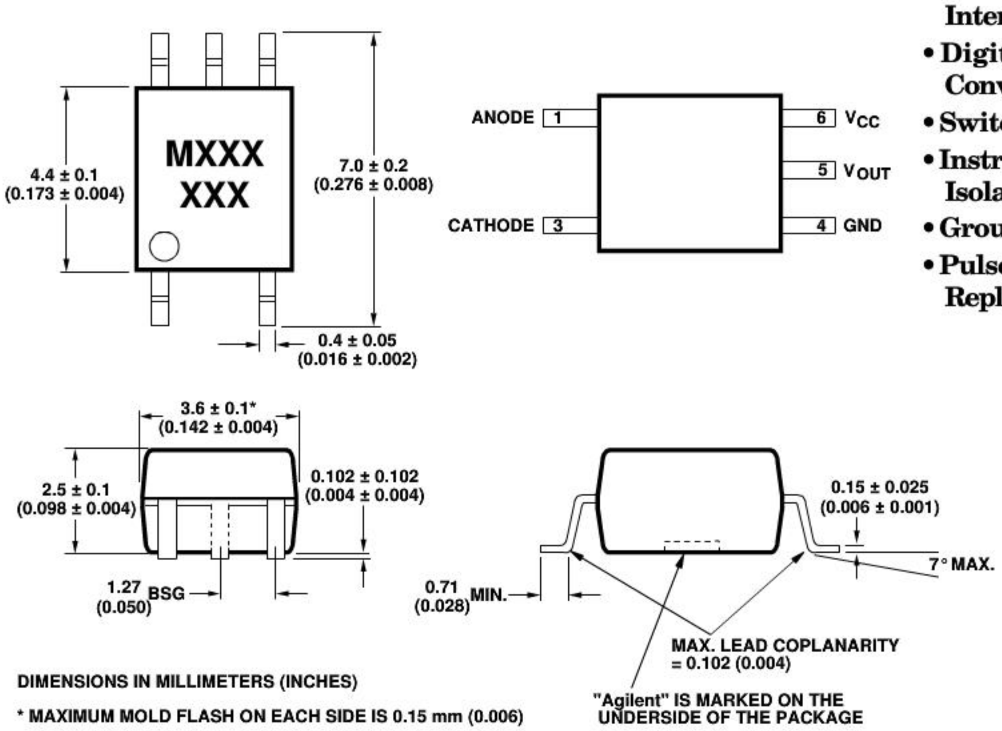
CAUTION: The small device geometries inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and /or degradation which may be induced by ESD.

The HCPL-M600/01/11 are suitable for high speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate, and are recommended for use in extremely high ground or induced noise environments.

Applications

- **Isolated Line Receiver**
- **Simplex/Multiplex Data Transmission**
- **Computer-Peripheral Interface**
- **Microprocessor System Interface**
- **Digital Isolation for A/D, D/A Conversion**
- **Switching Power Supply**
- **Instrument Input/Output Isolation**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**

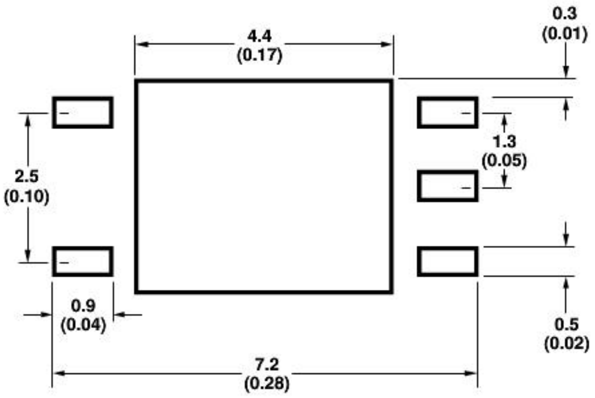
Outline Drawing (JEDEC MO-155)



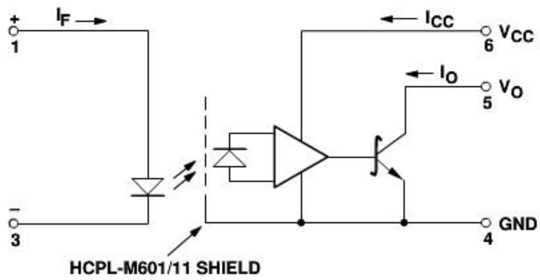
DIMENSIONS IN MILLIMETERS (INCHES)

* MAXIMUM MOLD FLASH ON EACH SIDE IS 0.15 mm (0.006)

Pin Location (for reference only)



Schematic



USE OF A 0.1 µF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 6 AND 4 (SEE NOTE 1).

TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

Recommended Operating Conditions

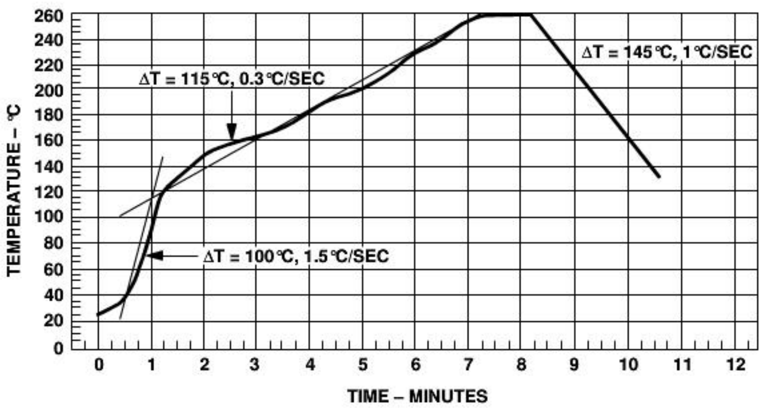
Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}*	0	250	µA
Input Current, High Level	I_{FH}	5	15	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (R_L = 1 kΩ)	N		5	TTL Loads
Output Pull-Up Resistor	R_L	330	4,000	Ω
Operating Temperature	T_A	-40	85	°C

* The off condition can also be guaranteed by ensuring that V_F(off) ≤ 0.8 volts.

Absolute Maximum Ratings

(No Derating Required up to 85°C)

Storage Temperature .... -55°C to +125°C
Operating Temperature .... -40°C to +85°C
Forward Input Current - I_F (see Note 2) .... 20 mA
Reverse Input Voltage - V_R .... 5 V
Supply Voltage - V_{CC} (1 Minute Maximum) .... 7 V
Output Collector Current - I_O .... 50 mA
Output Collector Power Dissipation .... 85 mW
Output Collector Voltage - V_O .... 7 V
(Selection for higher output voltages up to 20 V is available)
Infrared and Vapor Phase Reflow Temperature .... see below



Maximum Solder Reflow Thermal Profile.
(Note: Use of Non-Chlorine Activated Fluxes is Recommended.)

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L(IO1)	≥5	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L(IO2)	≥5	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

Electrical Specifications

Over recommended temperature (T_A = -40°C to 85°C) unless otherwise specified. (See note 1.)

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input Threshold Current	I_{TH}		2	5	mA	V_{CC} = 5.5 V, I_O ≥13 mA, V_O = 0.6 V	13	
High Level Output Current	I_{OH}		5.5	100	µA	V_{CC} = 5.5 V, V_O = 5.5 V I_F = 250 µA	1	
Low Level Output Voltage	V_{OL}		0.4	0.6	V	V_{CC} = 5.5 V, I_F = 5 mA, I_{OL} (Sinking) = 13 mA	2, 4, 5, 13	
High Level Supply Current	I_{CCH}		4	7.5	mA	V_{CC} = 5.5 V, I_F = 0 mA,		
Low Level Supply Current	I_{CCL}		6	10.5		V_{CC} = 5.5 V, I_F = 10 mA,		
Input Forward Voltage	V_F	1.4	1.5	1.75	V	T_A = 25°C	3	
		1.3		1.85		I_F = 10 mA		
Input Reverse Breakdown Voltage	BV_R	5				I_R = 10 µA		
Input Capacitance	C_{IN}		60		pF	V_F = 0V, f = 1 MHz		
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$		-1.6		mV/°C	I_F = 10 mA	12	
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min.		3, 4
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		3
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		3

*All typicals at T_A = 25°C, V_{CC} = 5 V.

Switching Specifications

Over recommended temperature (T_A = -40°C to 85°C), V_{CC} = 5 V, I_F = 7.5 mA unless otherwise specified.

Parameter	Symbol	Device HCPL-	Min.	Typ.*	Max.	Unit	Test Conditions		Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}		20	48	75	ns	T_A = 25°C		6, 7	5
					100				8	
Propagation Delay Time to Low Output Level	t_{PHL}		25	50	75		T_A = 25°C		6, 7	6
					100			R_L = 350 Ω	8	
Propagation Delay Skew	t_{PSK}				40					10, 11
Pulse Width Distortion	$\lvert t_{PHL} - t_{PLH} \rvert$			3.5	35			C_L = 15 pF	9	10
Output Rise Time (10%-90%)	t_{rise}			24					10	
Output Fall Time (10%-90%)	t_{fall}			10					10	
Common Mode Transient Immunity at High Output Level	$\lvert CM_H \rvert$	M600		10,000		V/µs	V_{CM} = 10 V	$V_{O(min)}$ = 2 V	11	7, 9
		M601	5,000	10,000			V_{CM} = 50 V	R_L = 350 Ω I_F = 0 mA		
		M611	10,000	15,000			V_{CM} = 1000 V	T_A = 25°C		
Common Mode Transient Immunity at Low Output Level	$\lvert CM_H \rvert$	M600		10,000			V_{CM} = 10 V	$V_{O(max)}$ = 0.8 V	11	8, 9
		M601	5,000	10,000			V_{CM} = 50 V	R_L = 350 Ω I_F = 7.5 mA		
		M611	10,000	15,000			V_{CM} = 1000 V	T_A = 25°C		

*All typicals at T_A = 25°C, V_{CC} = 5 V.

Notes:

1. Bypassing of the power supply line is required with a 0.1 µF ceramic disc capacitor adjacent to each optocoupler. The total lead length between both ends of the capacitor and the isolator pins should not exceed 10 mm.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
3. Device considered a two terminal device: pins 1 and 3 shorted together, and pins 4, 5 and 6 shorted together.
4. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{RMS} for 1 second (Leakage detection current limit, $I_{I-O} \leq 5$ µA).
5. The t_{PLH} propagation delay is measured from 3.75 mA point on the falling edge of the input pulse to the 1.5 V point on the rising edge of the output pulse.
6. The t_{PHL} propagation delay is measured from 3.75 mA point on the rising edge of the input pulse to the 1.5 V point on the falling edge of the output pulse.
7. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} > 2.0 V).
8. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} > 0.8 V).
9. For sinusoidal voltages, $(\lvert dV_{CM} \rvert / dt)_{max} = \pi f_{CM} V_{CM(p-p)}$.
10. See application section; "Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew" for more information.
11. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the worst case operating condition range.

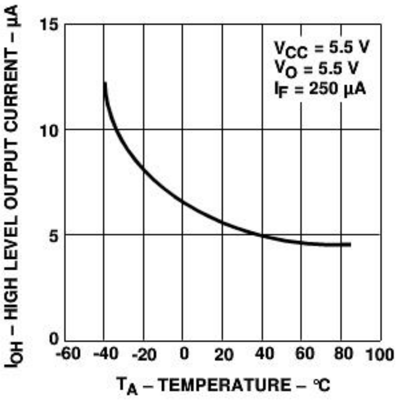


Figure 1. High Level Output Current vs. Temperature.

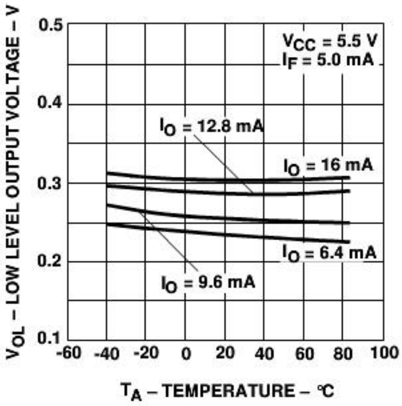


Figure 2. Low Level Output Voltage vs. Temperature.

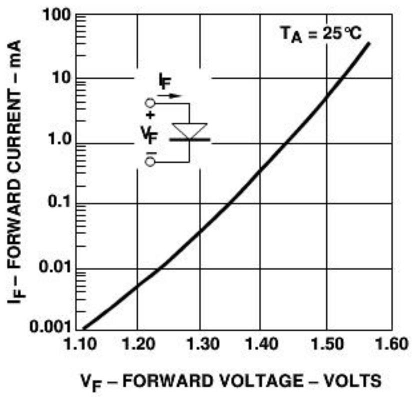


Figure 3. Input Diode Forward Characteristic.

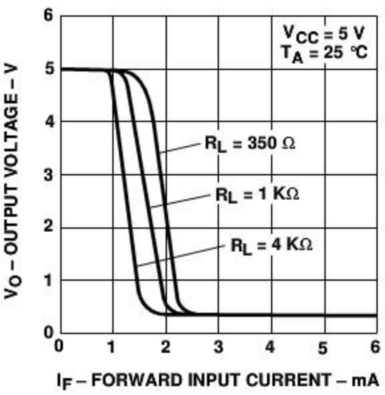


Figure 4. Output Voltage vs. Forward Input current.

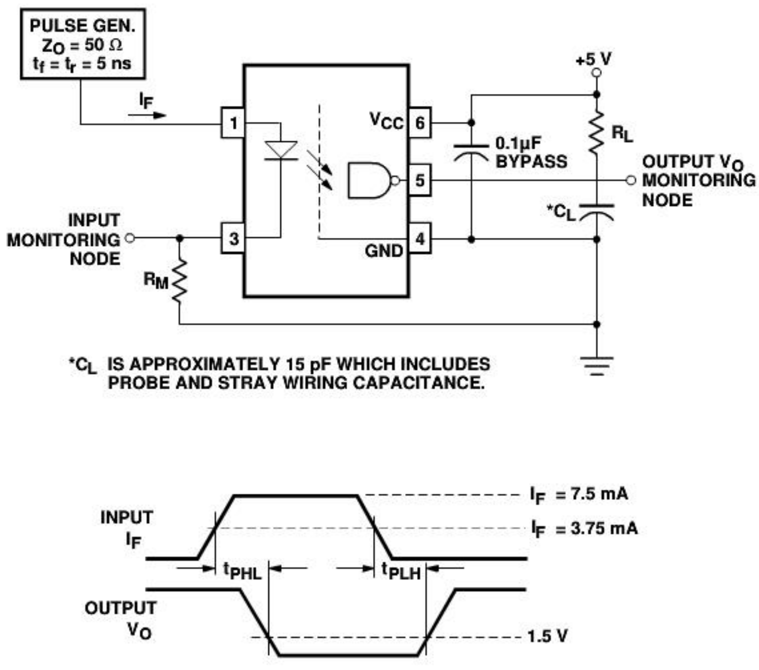


Figure 6. Test Circuit for t_{PHL} and t_{PLH}.

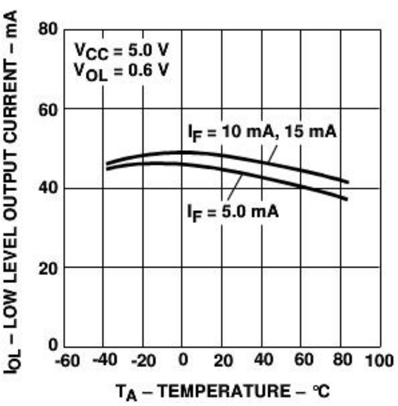


Figure 5. Low Level Output Current vs. Temperature.

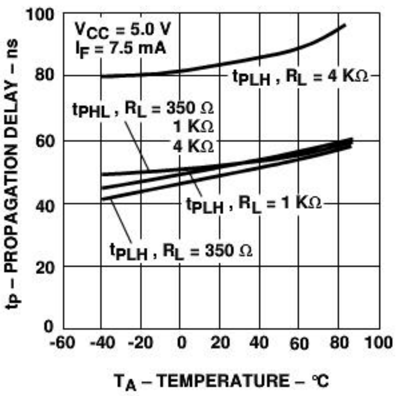


Figure 7. Propagation Delay vs. Temperature.

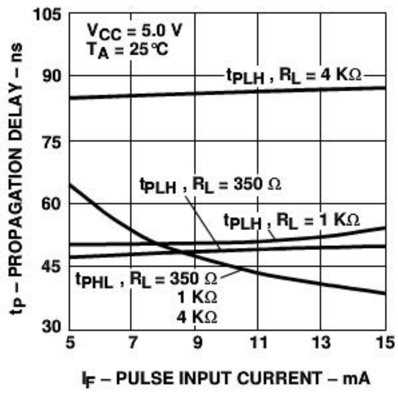


Figure 8. Propagation Delay vs. Pulse Input Current.

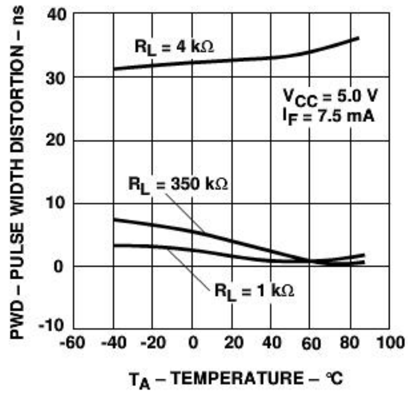


Figure 9. Pulse Width Distortion vs. Temperature.

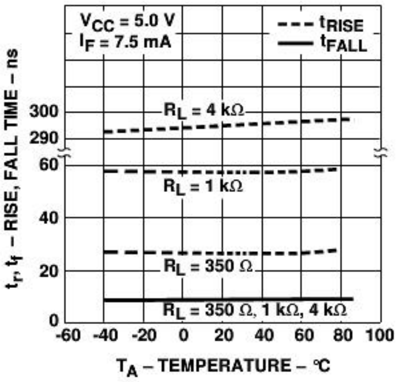


Figure 10. Rise and Fall Time vs. Temperature.

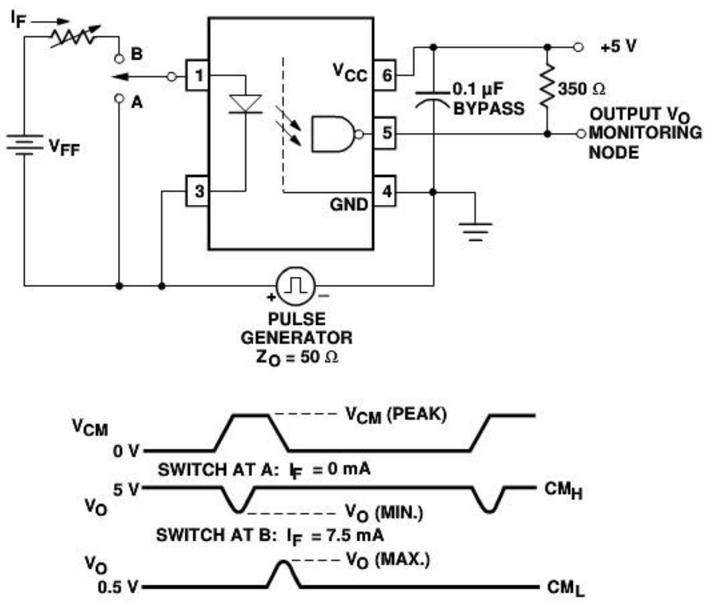


Figure 11. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

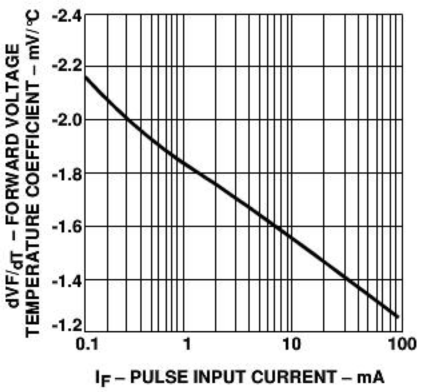


Figure 12. Temperature Coefficient for Forward Voltage vs. Input Current.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 7).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 15, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 11 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 16 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The t_{PSK} specified optocouplers offer the advantages of guaranteed specifications for propagation delays, pulse-width distortion and propagation delay skew over the recommended temperature, and input current, and power supply ranges.

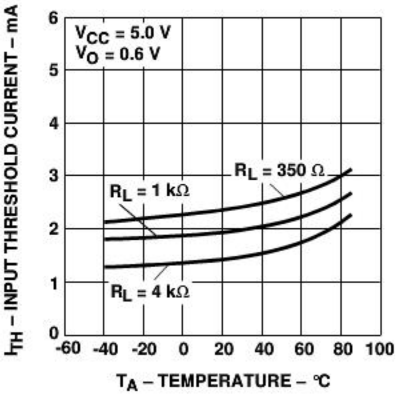


Figure 13. Input Threshold Current vs. Temperature.

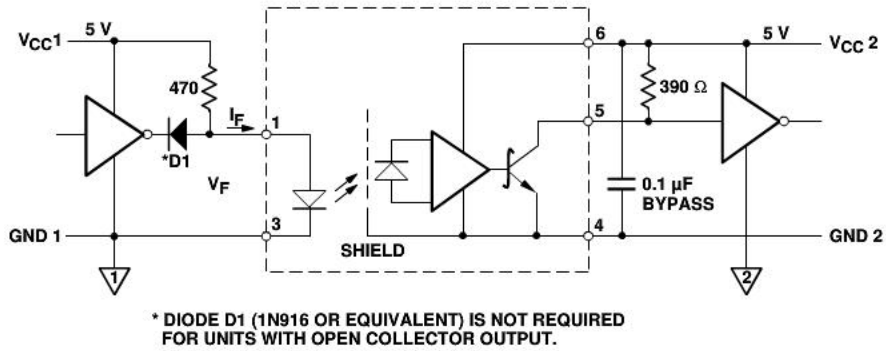


Figure 14. Recommended TTL/LSTTL to TTL/LSTTL Interface Circuit.

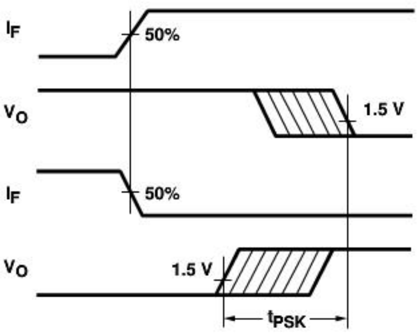


Figure 15. Illustration of Propagation Delay Skew – t_{PSK}.

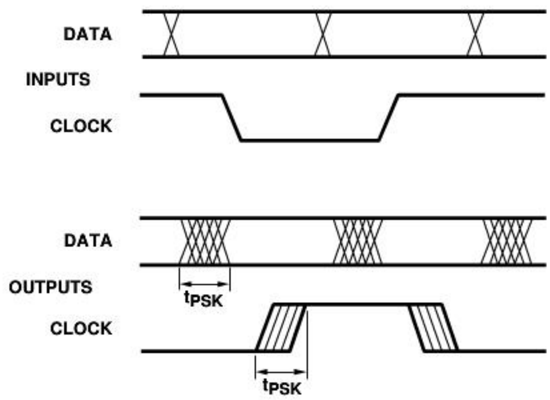


Figure 16. Parallel Data Transmission Example.

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Data subject to change.

Obsoletes 5091-9635E (10/93)
5966-4942E (11/99)