Application Notes: SY6992

Wide Input, High current, Bi-directional Regulator for Single Cell Li-Ion Battery Power Bank Application

Preliminary Specification

General Description

SY6992 is a 4.0-13.5VIN bi-directional regulator for Li-Ion battery power bank application. Advanced bi-directional energy flow control with automatic input power source detection is adopted to achieve battery charging mode and battery power supply mode alternately. If the external power supply is present, SY6992 runs in battery charging mode with fully protection function; if the external power supply is absent, SY6992 runs in battery power supply mode with output current capability up to 2.25A at 12V or 4.5A at 5V.

SY6992 has an integrated reverse blocking switch to prevent current leaking from the system side or battery side to the input side and an integrated linear switch to achieve over voltage/current protection at the system side. A half bridge with quasi-fixed 0.5MHz switching frequency is integrated to achieve power conversion for battery charging mode and battery power supply mode. All of them adopt N-channel MOSFET with 16V rating and extremely low R_{DSON} to optimize operation efficiency and extend battery life-time.
SY6992 is available in QFN4x4 package to minimize the PCB layout size for wide portable applications.

Ordering Information

SY6992 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6992QYC	QFN4x4-20	

Features

- Integrated N-Channel MOSFETs with 16V Voltage Rating and Extremely Low R_{DSON}
- High Switching Frequency to Minimize Peripheral Circuit Design
- Trickle Current / Constant Current / Constant Voltage Charging Mode
- Maximum 5A Battery Charging Current
- Maximum 4.5A/5V or 2.25A/12V System current in Battery power supply mode
- USB Port Identifier for Various Input Current Limit
- Automatic Input Power Source Detection
- I^2C controls
  - Programmable Battery Charge Voltage
  - Programmable Constant Current Charging
  - Programmable Over Current Limit for SYS load
  - Programmable Input Current DPM
  - Programmable Input Voltage DPM
  - Programmable Battery Charging Timeout
- Charging shutdown control
- Charging mode CV tolerance +/-0.5%
- DO+/DO- Divider mode Compliant
- DO+/DO- QC3.0 Compliant
- OUTPUT MTK PE Compliant
- Host Enable Control for Standby Mode in supply mode
- Supplement mode to Supply System by both Adapter and Battery.
- Over Temperature Protection
- Battery UTP/OTP in charging mode and supply mode
- Charge Status Indication
- Light load Status Indication

Applications

- Single cell Li-Ion Power Bank
- Portable device with 1-cell battery pack

Typical Applications

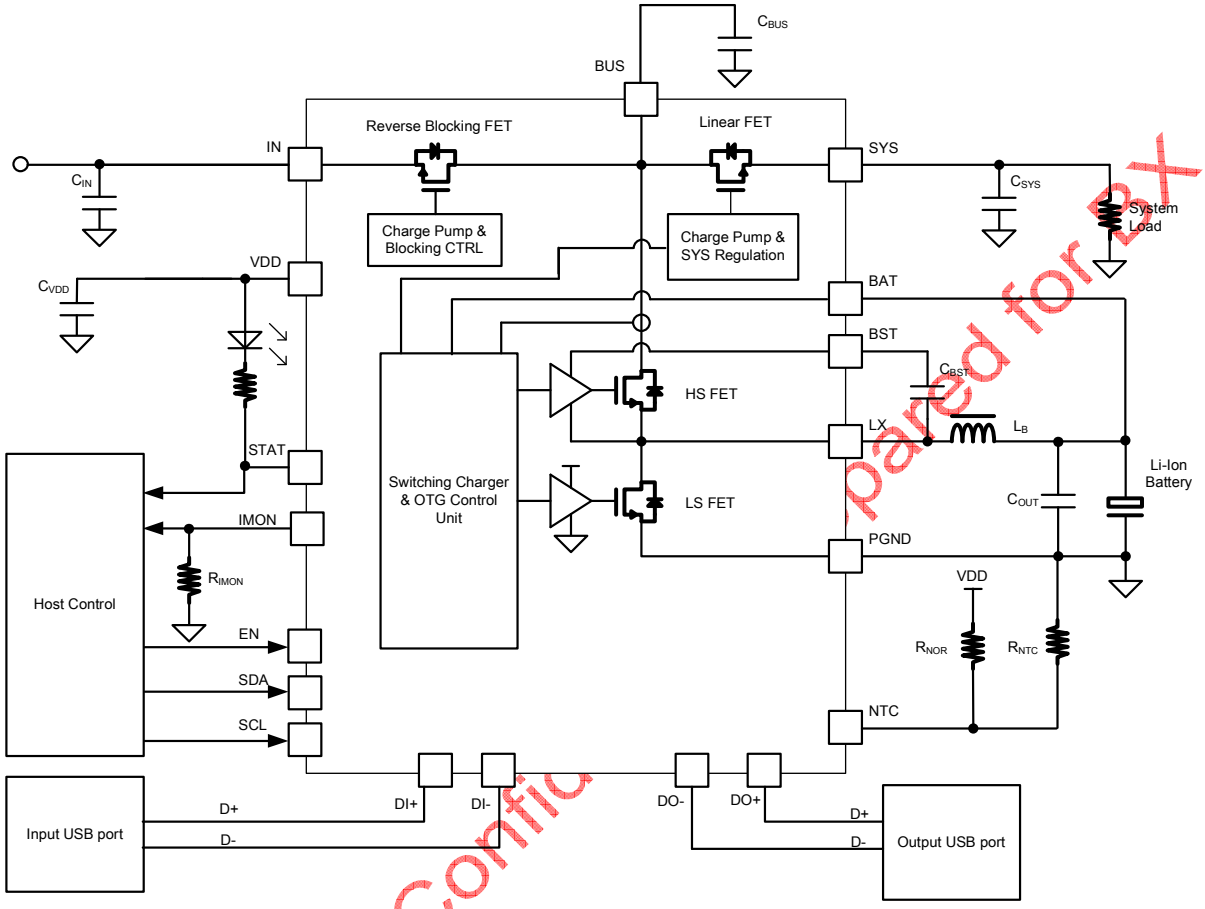
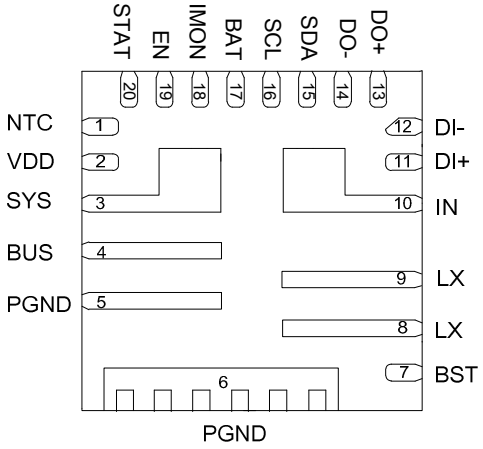


Figure 1. Schematic Diagram

Pinout (Top view)



(QFN4x4-20)

Top Mark: BHO*xyz* (device code: **BHO**, ***x=year code, y=week code, z= lot number code)***

Name	PIN Number	Description
NTC	1	Thermal protection and battery detection pin. In charging mode UTP threshold is about 65% VDD and OTP threshold is about 35% VDD. In discharging mode UTP threshold is about 81% VDD and OTP threshold is about 30% VDD.
VDD	2	Internal Linear regulator output. VDD is the output of 3.3V Linear regulator. Connect a 1uF ceramic capacitor from VDD to GND.
SYS	3	System load pin. Connect a MLCC from this pin to ground to decouple the high frequency noise.
BUS	4	Connection point for reverse blocking FET and bypass linear switch. Connect a MLCC from this pin to ground to decouple the high frequency noise.
PGND	5,6	Power ground pin.
BST	7	Boot strap pin. Connect a MLCC from this pin to LX.
LX	8,9	Switch node pin. Connect an external inductor from this pin to BAT pin.
IN	10	Positive power supply input pin. VIN ranges from 4V to 13.5V for normal operation and up to 16V surge. Connect a MLCC from this pin to ground to decouple high frequency noise.
DI+	11	Host USB D+ connection. For USB input identification
DI-	12	Host USB D- connection. For USB input identification
DO+	13	USB D+ for system connection. Support Divider mode and BC1.2 handshake.
DO-	14	USB D- for system connection. Support Divider mode and BC1.2 handshake.
SDA	15	I2C Interface data.
SCL	16	I2C Interface clock.
BAT	17	Battery positive pin. Also connect to inductor terminal.
IMON	18	Buffered current pin. In buck mode IMON output the input current of Buck converter, in boost mode IMON output the current of LNFET.V_{IMON}=I*R_{IMON}/80k
EN	19	Whole chip enable pin. When VIN is absent, high enable IC, low shutdown IC. When VIN is present, chip is always enabled when EN is low.
STAT	20	Charging status indication pin. It is open drain output pin and can be used to turn on a LED to indicate the charge in process. When the charge is done, LED is off. STAT pin will be pulled low for 200us to generate an INT when DI+, DI-, DO+, DO- pins handshake is done.

Absolute Maximum Ratings (Note 1)

STAT, LX, BUS, BAT, SYS, EN ---------- -0.5- 18V
IN, SCL, SDA, DI+, DI-, DO+, DO- ---------- -0.5- 18V
VDD, NTC, IMON ---------- -0.5- 4V
BST-LX ---------- -0.5-4V
Power Dissipation, PD @ TA = 25°C, ---------- 2.5 W
Package Thermal Resistance (Note 2)
θJA---------- 40 °C/W
θJC ---------- 20 °C/W
Junction Temperature Range ---------- -40°C to +150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 125°C

Recommended Operating Conditions (Note 3)

STAT, LX, BUS, BAT, SYS, EN ---------- less than 16V
IN, SCL, SDA, DI+, DI-, DO+, DO- ---------- less than 16V
VDD, NTC, IMON ----------0-3.6V
BST-LX ----------0-3.6V
Junction Temperature Range ---------- -20°C to 100°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

T_A=25°C, T_A=T_J, V_{IN}=5V, GND=0V, C_{IN}=20uF, L_B=2.2uH, R_{IMON}=20kΩ, C_{OUT}=20uF, C_{BUS}=40uF, C_{SYS}=1uF, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Quiescent Current						
I_{BAT}	Battery leakage current	EN pull down			10	uA
I_{IN}	Input quiescent current	NTC=0V		1.5		mA
I_{BOOST}	Boost null-load battery discharge current	V_{BAT}=4.35V,Vsys=5V, I_{SYS}=0V, Converter switching		2		mA
Input Power Supply						
V_{INUVLO}	Input voltage UVLO threshold			3.9		V
V_{UVHYS}	Input voltage UVLO hysteresis	Falling edge		100		mV
LDO Output						
V_{VDD}	VDD voltage	V_{BUS}=5V		3.3		V
I_{VDD}	VDD source current	V_{VDD}=3V	50			mA
Linear FET						
R_{LNFT}	$R_{DS(ON)}$ of the linear NFET			35		mΩ
I_{SYSMAX}	System current limit tolerance	Reg02[4:2]=100		3		A
V_{SYSMAX}	System clamp voltage tolerance	LV		5.8		V
		HV		13		V
Blocking FET						
R_{BKFT}	$R_{DS(ON)}$ of reverse blocking NFET			35		mΩ
Half-bridge in Buck Mode						
Voltage and Current Bias						
V_{BUS}	BUS Supply voltage for battery charging		4.5		13.5	V
$V_{BOVP\_LV\_BK}$	BUS voltage OVP threshold in LV mode	Rising edge	6			V
$V_{BOVPHYS\_LV\_BK}$	BUS voltage OVP hysteresis in LV mode	Falling edge		0.5		V
$V_{BOVP\_HV\_BK}$	BUS voltage OVP threshold in HV mode	Rising edge	13.5			V
$V_{BOVPHYS\_HV\_BK}$	BUS voltage OVP hysteresis in HV mode	Falling edge		0.5		V
Switching Frequency						
f_{SWBK}	Buck Switching frequency			0.5		MHz
$T_{ONMINHS}$	Min on time for charging mode, HS FET			100		ns
$T_{ONMAXHS}$	Max on time for charging mode, HS FET	In low dropout mode		7		us
Battery Charging						
V_{CV}	Battery CV voltage tolerance	Voltage on BAT pin	-0.5		0.5	%

ΔV_{RCH}	Battery voltage threshold hysteresis for recharge	Falling edge		100		mV
V_{TRK}	Battery trickle charging mode voltage threshold	Rising edge	2.7	2.8	2.9	V
I_{CC}	Charging current accuracy for Constant Current Mode	Reg03[2:0]=011		2		A
	Charging current accuracy for Trickle Current Mode	Reg03[2:0]=011		0.2		A
I_{TERM}	Termination current tolerance	Reg03[2:0]=011.		100		mA
V_{BTOVP}	Battery voltage OVP threshold		105%	110%	115%	V_{CV}
Battery Short Circuit Protection						
$V_{SHORTBT}$	Battery short circuit protection threshold			2		V
Dynamic Input Power Management						
I_{DPM}	Input current limit tolerance	Reg02[7:5]=011		1.5		
V_{DPM}	Input Voltage regulation during input voltage dynamic power management		-2		2	%
USB Port Identification and Current Limit Reference (Proposal 1)						
I_{SDP}	SDP input current limit			500		mA
I_{DCP}	DCP input current limit			1500		mA
Half-bridge in Boost Mode						
Voltage and Current Bias						
V_{BATDEP}	Battery depletion voltage tolerance	Falling edge		2.6		V
$V_{BATDEPHYS}$	Battery depletion voltage	Rising edge		0.28		V
$V_{BOVPHYS\_LV\_BT}$	BUS voltage OVP threshold in LV mode	Rising edge	6			V
$V_{BOVPHYS\_LV\_BT}$	BUS voltage OVP hysteresis in LV mode	Falling edge		0.5		V
$V_{BOVP\_HV\_BT}$	BUS voltage OVP threshold in HV mode	Rising edge	13.5			V
$V_{BOVPHYS\_HV\_BT}$	BUS voltage OVP hysteresis in HV mode	Falling edge		0.5		V
V_{SYS}	SYS voltage tolerance					V_{SYS}
I_{SYS_LOW}	OTG light load threshold	REG01[4]=1,I_{SYS_LOW}=50mA,falling edge		50		mA
		REG01[4]=0,I_{SYS_LOW}=100mA,falling edge		100		mA
$I_{PEAK\_MAX\_BT}$	Boost mode max peak current tolerance	REG02[1:0]=00, $I_{PEAK\_MAX\_BT}$=5A				%
		REG02[1:0]=01, $I_{PEAK\_MAX\_BT}$=7A				%
		REG02[1:0]=10, $I_{PEAK\_MAX\_BT}$=9A				%
		REG02[1:0]=11,$I_{PEAK\_MAX\_BT}$=11A				%
Switching Frequency						
f_{SWBST}	Boost Switching			0.5		MHz

	frequency					
T_{ONMINL}	Min on time for discharging mode, LS FET			200		ns
Other General Parameters						
Battery Thermal Protection NTC						
Battery Detection	Battery removed	Rising edge	88%			
UTP_CHG	Under temperature protection	Rising edge, charging mode	63%	65%	67%	
	Under temperature protection hysteresis	Falling edge, charging mode		5%		
OTP_CHG	Over temperature protection	Falling edge, charging mode	33%	35%	37%	
	Over temperature protection hysteresis	Rising edge, charging mode		2%		
UTP_DCHG	Under temperature protection	Rising edge, Discharging mode	79%	81%	83%	
	Under temperature protection hysteresis	Falling edge, Discharging mode		5%		
OTP_DCHG	Over temperature protection	Falling edge, Discharging mode	28%	30%	32%	
	Over temperature protection hysteresis	Rising edge, Discharging mode		2%		
Power MOSFET						
R_{HSFT}	$R_{DS(ON)}$ of High-Side NFET			10		mΩ
R_{LSFT}	$R_{DS(ON)}$ of Low-Side NFET			5		mΩ
Logic Level and Timing						
V_{LOW}	EN,SCL,SDA low level threshold				0.4	V
V_{HIGH}	EN,SCL,SDA low level threshold		1.3			V

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

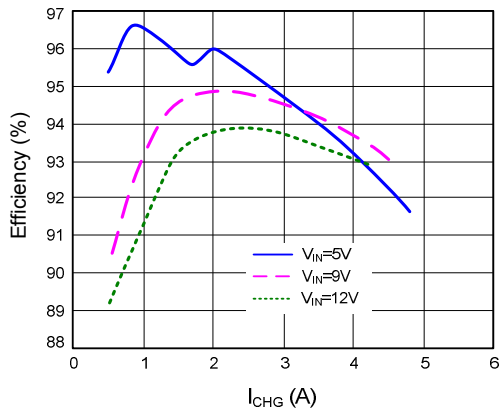
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions

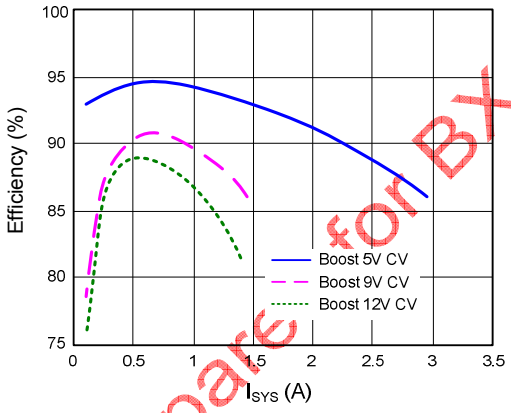
Typical Performance Characteristics

(T_A=25°C, V_{IN}=5V, unless otherwise specified.)

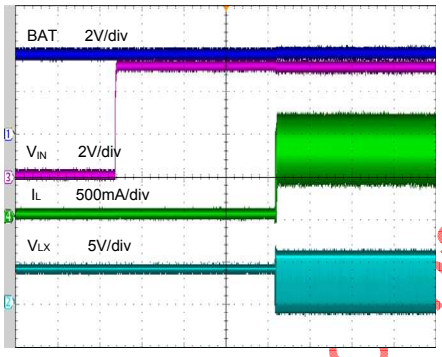
Efficiency vs. Charging current (CV mode)



Efficiency vs. I_{SYS} (Boost mode, BAT=2.8V)

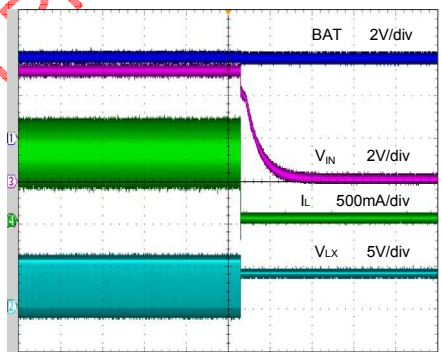


5V VIN Power ON(Adapter)



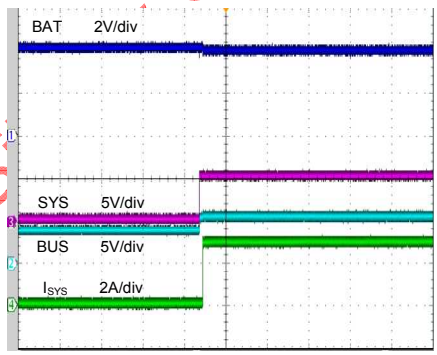
Time (200ms/div)

5V VIN Power OFF(Adapter)



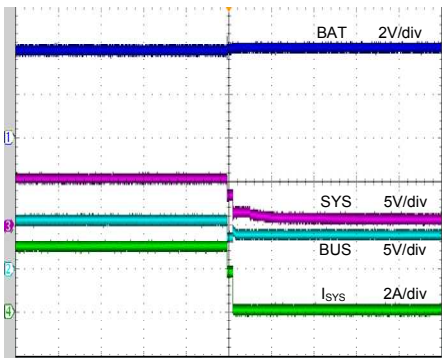
Time (200ms/div)

5V Boost mode OTG ON by I2C



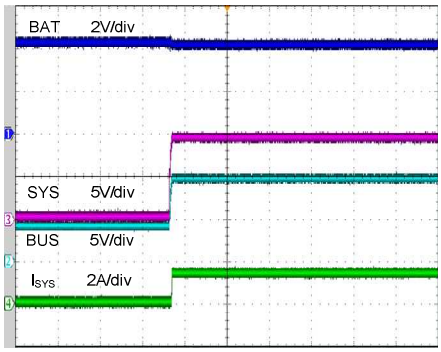
Time (200ms/div)

5V Boost mode OTG OFF by I2C



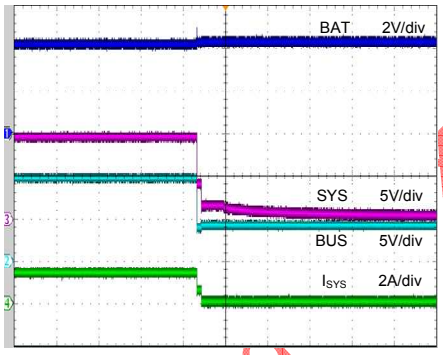
Time (200ms/div)

9V Boost mode OTG ON by I2C



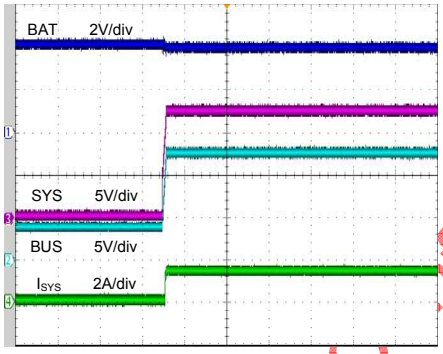
Time (200ms/div)

9V Boost mode OTG OFF by I2C



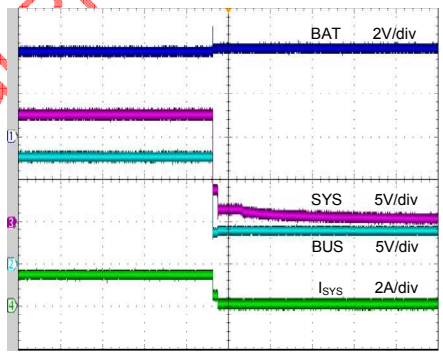
Time (200ms/div)

12V Boost mode OTG ON by I2C



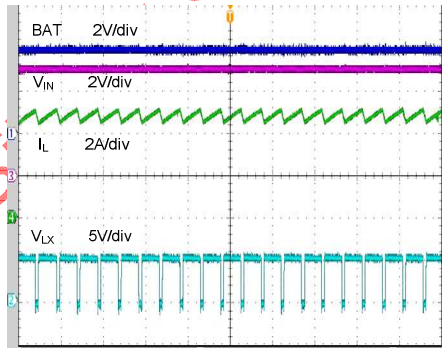
Time (200ms/div)

12V Boost mode OTG OFF by I2C



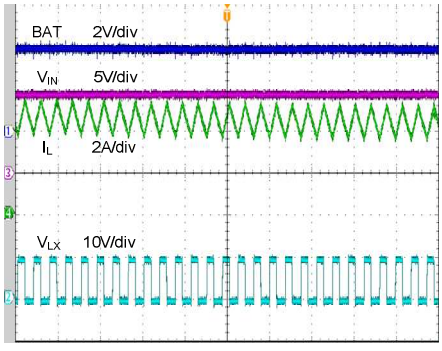
Time (200ms/div)

5V Buck Steady State



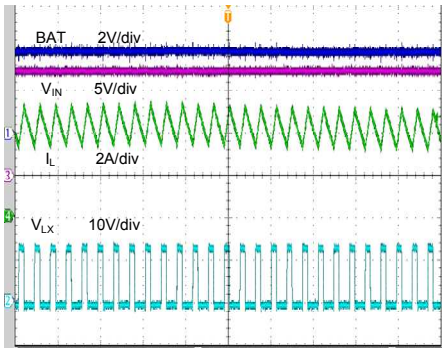
Time (4μs/div)

9V Buck Steady State



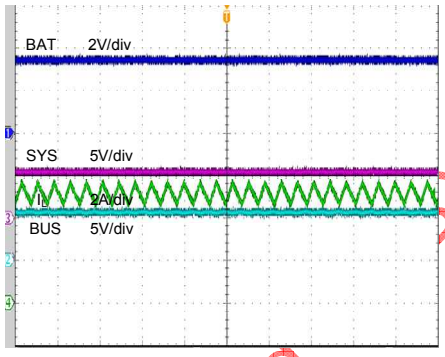
Time (4μs/div)

12V Buck Steady State



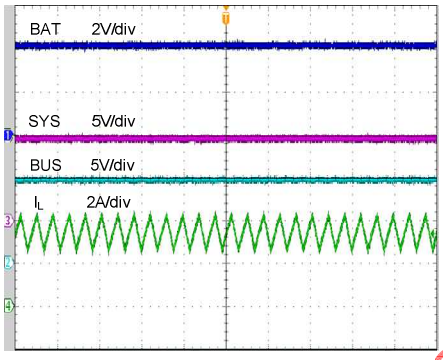
Time (4μs/div)

5V Boost Steady State



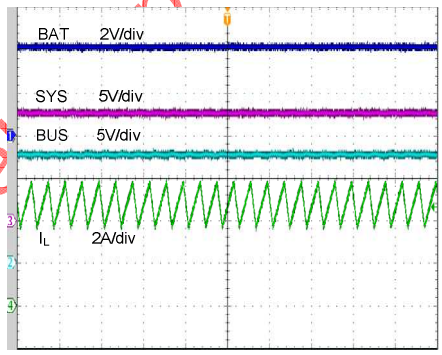
Time (4μs/div)

9V Boost Steady State



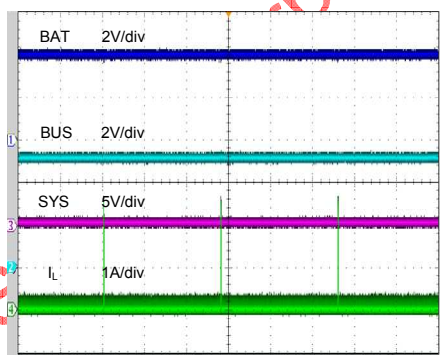
Time (4μs/div)

12V Boost Steady State



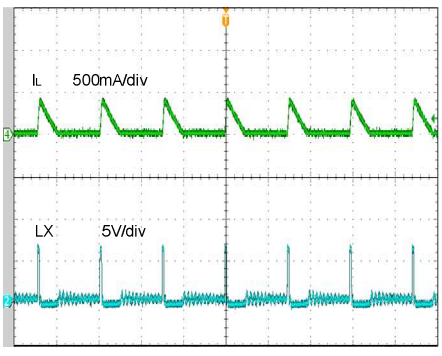
Time (4μs/div)

Boost SYS Short



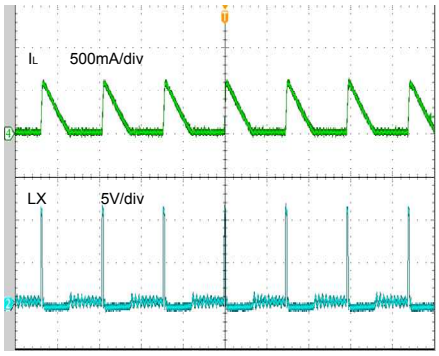
Time (200ms/div)

Battery Short In 5V Charging Mode



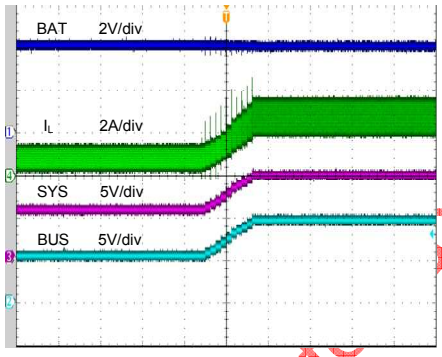
Time (4μs/div)

Battery Short In 12V Charging Mode



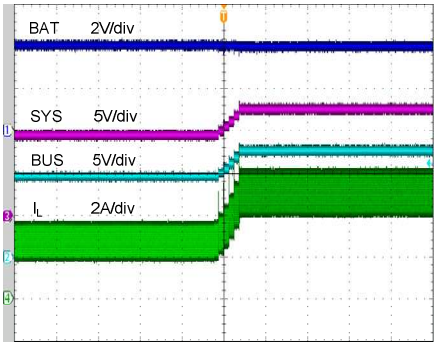
Time (4μs/div)

Boost 5V to 9V



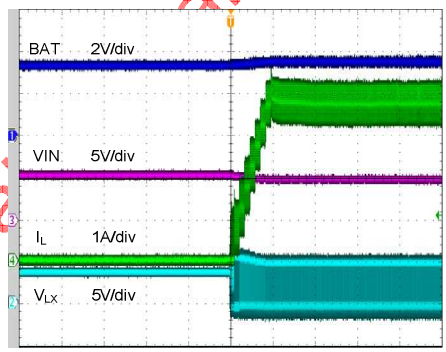
Time (10ms/div)

Boost 9V to 12V



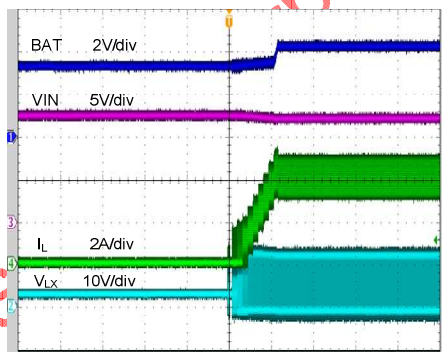
Time (10ms/div)

Inductor current soft start in 5V charging mode



Time (10ms/div)

Inductor current soft start in 12V charging mode



Time (10ms/div)

General Function Description

Working mode description

Charging mode. When input is present, SY6992 works in charging mode to charge the battery. The half bridge works in buck mode with the control of I_{DPM}/V_{DPM}/CV/CC loop.

Bypass mode. When input is present, OTG is enabled, SY6992 works in charging mode and supply the power from input to SYS at the same time.

Supplement mode In bypass mode, the increase of SYS load may make SY6992 work in I_{DPM} loop and make charging current decreases. When the PWM duty cycle of buck converter decrease to zero and the system current goes on increasing, SY6992 will enter into supplement mode. In supplement mode the half bridge of SY6992 switches from Buck mode to Boost mode and delivers the power from both the input and the battery to SYS.
The supplement mode is enabled by REG01[6].

Supply mode/Boost mode When input is absent, V_{BAT} is higher than V_{BATDEP}, the half bridge of SY6992 works in boost mode to supply power to SYS load.

Automatic Input Power Supply Detection

SY6992 adopts an internal current source with 10mA maximum capability to discharge the IN pins for 100ms once V_{IN} exceeds input UVLO threshold. When a good adapter is present, V_{IN} should keep being higher than the input UVLO even after 100ms discharging. While V_{IN} is present REG00[0] will be set to 1.

Input Power Up

After Automatic Input Power Supply Detection is done and V_{IN} is present, SY6992 will generate an INT and enable BC1.2 detection automatically, after BC1.2 detection the input USB type is recorded in REG07[5:4]. The MCU can monitor the USB type by I2C to set the appropriate Charging current\Input current limit\Input V_{DPM}. After BC1.2 detection is done SY6992 will start charging.

SY6992 can set the DI+\DI- output voltage by REG06[3:0] and monitor the DI+\DI- input voltage by REG06[7:4].

After Input power up, the input voltage range should be 4.2V-6V to ensure SY6992 works normally. In order to work in higher input voltage, REG07[7:6] should be set to 7V/9V or 12V to change the OVP and V_{DPM} of SY6992.

Charging mode Enable control

When V_{IN} is present, charger can be enabled by I2C REG01[7].

Programmable Input Current Dynamic Power Management

The input current limit is programmed by I2C REG02[7:5]. Once input current reaches I_{DMP}, the input current will be limited to I_{DPM} by regulating the duty of Buck convertor.

Programmable Input Voltage Dynamic Power Management

The input voltage limit is programmed by REG03[7:5]. Once input voltage drops to V_{DPM}, the input voltage will be limited to V_{DPM} by regulating the duty of Buck convertor.

REG00[1] will be set to 1 while SY6992 in VDPM state.

SYS Current Limit

SYS current limit is programmed by REG02[4:2].
In boost mode, once SYS current exceeds I_{SYS_Limit}, SYS current is limited to I_{SYS_Limit} by regulating the duty of Boost converter.

Programmable charging current

Charging current is programmed by REG03[2:0].

Termination current can be set to 5%Icc.

Programmable charging voltage

Charging voltage is programmed by REG03[4:3].

The monitor of current

In buck mode IMON output the input current of Buck converter, in boost mode IMON output the current of LNFET.

$V_{IMON}=I*R_{IMON}/80k$

Interrupt to Host (INT)

An INT is generated by pulling STAT low for 200us. In some applications, the host does not always monitor the charger operation. The INT notifies the system on the device operation. The following events will generate 200us INT pulse.

- 130ms delay time after VIN power on
- Downstream QC detection done
- The request voltage of Downstream changed

After INT is inserted, the MCU must read I2C to clear the INT, otherwise an INT will be sent every 800ms.

OTG Function

When VIN is present, REG01[5] is active, OTG function is enabled to turn on LNFET. When VIN is absent, REG01[5] is active, OTG function is enabled to turn on the Boost converter and LNFET.

Downstream output voltage control

REG05[4:2] can set the SYS output voltage in boost mode and record the request voltage of downstream .

OTG RESET condition

REG01[5] will be reset to 0 (OTG is disabled) while following protections happens:

- BAT depletion

Charging Status Indication Description

1. **Charging-In-Process** – Pull and keep STAT pin to Low;
2. **Charging Done** – Pull and keep STAT pin to High;
3. **Fault Mode** – Output high and low voltage alternatively with 10Hz frequency. Fault mode includes VIN OVP, BAT OVP, BAT SCP, BAT UTP/OTP, charging time out.

Connect a LED from VDD to STAT pin, **LED ON** indicates **Charging-in-Process**, **LED OFF** indicates **Charging Done**, **LED Flash** indicates **Fault Mode**. Charging status is recorded in REG00[5:4]

Protection Description

Thermal Protection-Thermal protection for battery is achieved through NTC pin in charging and discharging mode. The basic scheme is shown in application information. Thermal shutdown is active for the device itself. IC recovers to normal work when the temperature returns into normal range again. Charging timer stops and maintains the result during thermal protection.

Short Circuit Protection- There are BAT short circuit protection and SYS short circuit protection in SY6992. When V_{SYS} is lower than $V_{SHORTSYS}$, the linear FET modulates the current to be saw tooth shape from 0A to 1.7A for short circuit protection recovery. SY6992 tries recovery for 5ms per 0.7s. In charging mode once V_{BAT} is lower than $V_{SHORTBT}$, the switching frequency is fold back to 20% of the default value.

Over Voltage Protection- When V_{BUS} or V_{BAT} is higher than the over voltage protection threshold, the half bridge stops boost operation or buck operation immediately. It recovers to normal work when the monitored voltage backs to normal level. Input voltage has UVLO and OVP, which would make the device shutdown, SY6992 will recover to normal work when the V_{IN} backs to normal range.

Battery Over discharge protection

IN Supply mode, once battery voltage is lower than V_{BATDIS}, SY6992 will turn off boost and LNFET. REG01[5] will be reset to 0 at the same time.

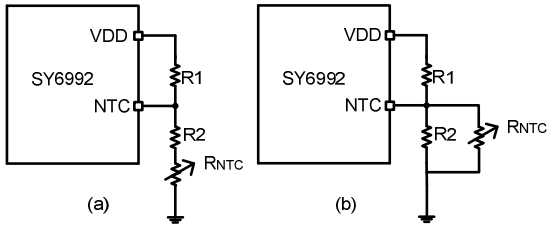
Timeout Protection-Programmable timeout protection for the Trickle Current Charge Mode and the Constant Current and CV Charge Mode both. Time out time is set by REG01[2:1].Once timeout, the device stops the charge operation and latch-off. Only re-plug in power source can reset the latch logic and restart the normal charging.

Applications Information

Because of the high integration of SY6992, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, BUS capacitor C_{BUS}, battery capacitor C_{BAT}, inductor L, NTC resistors R1, R2, need to be selected for the targeted applications specifications.

NTC resistor:

SY6992 monitors battery temperature by measuring the VDD voltage and NTC voltage. The controller triggers the UTP or OTP when the rate K (K= V_{NTC}/V_{VDD}) reaches the threshold of UTP (K_{UT}) or OTP (K_{OT}). The temperature sensing network is showed as below.
Choose R1 and R2 to program the proper UTP and OTP points.



The calculation steps of Figure (a) are:

1. Define K_{UT}, K_{UT} =65%
2. Define K_{OT}, K_{OT} =35%
3. Assume the resistance of the battery NTC thermistor is R_{UT} at UTP threshold and R_{OT} at OTP threshold.
4. Calculate R2

$$R2 = \frac{K_{OT}(1-K_{UT})R_{UT} - K_{UT}(1-K_{OT})R_{OT}}{K_{UT} - K_{OT}}$$

5. Calculate R1

$$R1 = (1/K_{OT} - 1)(R2 + R_{OT})$$

If choose the typical values K_{UT} =65% and K_{OT}=35%, then

$$R2 = 0.408R_{UT} - 1.408R_{OT}$$
$$R1 = 1.857(R2 + R_{OT})$$

Input capacitor C_{IN}:
Input capacitor reduces the surge current drawn from the input and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high-frequency-switching current from passing to the input.

To minimize the potential noise problem, place a typical X7R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. At least 20uF ceramic capacitor are suggested.

Bus capacitor C_{BUS}:
1. Buck mode
The capacitor acts as the input capacitor of the buck converter. The input current ripple rms value is larger than:

$$I_{CIN\_MIN} = I_{CHG}\sqrt{D(1-D)}$$

While I_{CHG} is the charge current.

2. Boost mode
C_{BUS} is the output capacitor of boost converter. C_{BUS} reduces the bus voltage ripple and ensures the stability of boost. The output current ripple rms value is :

$$I_{CBUS\_RMS} = \frac{\Delta I}{2\sqrt{3}}$$

While ΔI is the current ripple of inductor.
At least 20uF ceramic capacitor are suggested.

Battery capacitor C_{BAT}:
1. Buck mode
Battery capacitor acts as the output capacitor of Buck converter. C_{BAT} is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X7R or better grade ceramic capacitor. The output voltage ripple is calculated as below:

$$V_{Ripple\_BAT\_Buck} = \frac{(1-D)\times V_{BAT}}{8C_{BAT}F_{SW}^{2}L}$$

Where F_{SW} is the switching frequency.
2. Boost mode
C_{BAT} acts as the input capacitor of Boost converter. The input voltage ripple is calculated as below:

$$V_{Ripple\_BAT\_Boost} = \frac{D\times V_{BAT}}{8C_{BAT}F_{SW}^{2}L}$$

Where F_{SW} is the switching frequency.
At least 20uF ceramic capacitor are suggested.

Inductor L:
Inductor selection trades off between cost, size, and efficiency. A lower inductance value corresponds with smaller size, but results in higher ripple currents, higher magnetic hysteretic losses, and higher output capacitances. However, a higher inductance value benefits from lower ripple current and smaller output

filter capacitors, but results in higher inductor DC resistance (DCR) loss. An inductor must not saturate under the worst-case condition.

1.Buck mode

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:

$$L = \frac{V_{BAT}(1 - V_{BAT}/V_{IN,\,MAX})}{F_{SW} \times I_{CHG,\,MAX} \times 40\%}$$

Where F_{SW} is the switching frequency and $I_{CHG,MAX}$ is the maximum charge current.

SY6992 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,\,MIN} > I_{CHG,\,MAX} + \frac{V_{BAT}(1 - V_{BAT}/V_{IN\ MAX})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement.

2. Boost mode

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:

$$L = \frac{V_{BAT}(1 - V_{BAT}/V_{BUS\_MAX})}{F_{SW} \times I_{DIS,\,MAX} \times 40\%}$$

Where F_{SW} is the switching frequency and $I_{DIS,MAX}$ is the maximum discharge current.

SY6992 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,\,MIN} > I_{DIS,\,MAX} + \frac{V_{BAT}(1 - V_{BAT}/V_{BUS\_MAX})}{2 \times F_{SW} \times L}$$

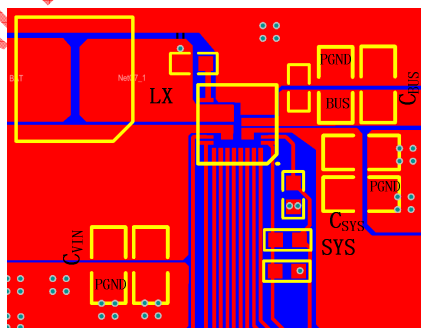
3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement.

Layout Design:

The layout design of SY6992 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN}, C_{BUS}, C_{SYS}, L.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to Pins IN and GND, C_{BUS} must get close to Pins BUS and GND. The loop area formed by C_{IN} and GND, C_{BUS} and GND must be minimized. Following figure is the recommended layout design.



3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) In high current applications, a RC snubber circuit should be placed between LX and GND for better EMI.

Register Description

Battery Charger Registers

The SY6992 supports 7 battery-charger registers that use either Write-Word or Read-Word protocols, as summarized in Table 1. 04H are “read only” registers and can be used to identify the SY6992.

Table 1. Battery Charger Register Summary

Register Address	Register Name	Read/Write	Default
00H	Status/Control Register	Read or Write	XXH
01H	Control Register	Read or Write	84H
02H	Current Register	Read or Write	XXH
03H	Charge Register	Read or Write	89H
04H	Vendor/PN/Rev Register	Read	XXH
05H	Quick Charge Register1	Read or Write	XXH
06H	Quick Charge Register2	Read or Write	XXH
07H	Quick Charge Register3	Read or Write	XXH

Table 2. Status/Control Register (00H)

Bit	Bit Name	R/W	Description
7	Reset	R/W	Write 1 to reset all the parameters, auto clear
6	Boost	R	1: In boost mode 0: Not in boost mode
5:4	Status	R	00: Ready 01: Charge in progress 10: Charge done 11: Fault
3	BST_LLOAD	R	0:I_{SYS}> I_{SYS_L} 1:I_{SYS}< I_{SYS_L} ,Boost mode light load
2	BAT_DPL	R	0: V_{BAT}> V_{BATDEP} 1: V_{BAT}< V_{BATDEP}
1	VDPM_STATE	R	1: In VDPM state; 0: Not in VDPM state.
0	VIN_PRES	R	1: Vin present; 0: Vin absent.

Table 3. Control Register (01H)

Bit	Bit Name	R/W	Description
7	Charge_Enable	R/W	0: Disable charger 1: Enable charger (default)
6	Supplement_Enable	R/W	0: Disable charge Supplement mode (default) 1: Enable charge Supplement mode

5	OTG_Enable	R/W	0: Disable OTG mode(default) 1: Enable OTG mode Both OTG and the register are available can enable OTG function.
4	OTG_Lightload	R/W	SYS light load threshold set. 0: 100mA (default) 1: 50mA
3	Vsys comp	R/W	System output voltage compensation in 5V mode. 1: 5.25V; 0: 5V(default).
2:1	Timer	R/W	Charge timeout protection. 00: 5h 01: 10h 10: 20h (default) 11: Disable timer
0	Freq	R/W	Buck and Boost converter frequency set. 0: 500kHz (default) 1: 300kHz

Table 4. Current Register (02H)

Bit	Bit Name	R/W	Description
7:5	IDPM	R/W	Input current limit for 5/8.4V source. 001: 0.5A 010: 1A 011: 1.5A 100: 2A 101: 2.5A 110: 3A 111: Disable input current limit
4:2	ISYS_Limit	R/W	SYS current limit for 5/8.4V SYS voltage. 000: 1/0.5A 001: 1.5/0.75A 010: 2/1A 011: 2.5/1.25A 100: 3/1.5A 101: 3.5/1.75A 110: 4/2A (default) 111: 4.5/2.25A
1:0	IPKBST	R/W	Boost peak current set. 00: 5A 01: 7A 10: 9A 11: 11A (default)

Table 5. Voltage Register (03H)

Bit	Bit Name	R/W	Description
7:5	VDPM	R/W	Input voltage dynamic control. For 5V/7V/9V/12V input voltage set, V_{DPM}=Vin_set x(1-bit[7:5]). The VDPM need be clamped upon UVLO threshold. 000: 0 001: -2%

			010: -4% 011: -6% 100: -8% (default) 101: -10% 110: -12% 111: Disable VDPM
4:3	Charge_Voltage	R/W	Max charge voltage. 00: 4.10V 01: 4.20V (default) 10: 4.35V 11: 4.4V
2:0	Charge_Current	R/W	Max charge current 000: 0.5A 001: 1A (default) 010: 1.5A 011: 2A 100: 2.5A 101: 3A 110: 4A 111: 5A

Table 7. Vendor/PN/Rev Register (04H)

Bit	Bit Name	R/W	Description
7:5	Vendor_Code	R	101: Identify the supplied
4:3	PN	R	11: SY6992
2:0	Revision	R	001: Revision 1.0 010: Revision 1.1 011: Revision 1.2 ……

Table 8. Quick Charge Register1 (05H)

Bit	Bit Name	R/W	Description
7:5	Downstream_Voltage_Request	R	Record the voltage of downstream request. 111:12V(PE) 110:9V(PE) 101:7V(PE) 100:5V(PE) 011:12V(QC) 010:9V(QC) 001:continuous mode (QC) 000:5V(QC)
4:2	Downstream_Voltage_Set	R/W	Set the output voltage of SYS. 111:12V(PE) 110:9V(PE) 101:7V(PE) 100:5V(PE) 011:12V(QC) 010:9V(QC)

Bit	Bit Name	R/W	Description
			001:continuous mode (QC) 000:5V(default)
1:0	Continuous_mode_UP_DOWN	R/W	QC3.0 continuous mode control. In continuous mode, in order to increase the SYS voltage by 200mV these 2 bits must be set to 01 and then to 00; in order to decrease the SYS voltage by 200mV these bits must be set to 10 and then to 00. 10:DOWN 01:UP 00:HOLD (defalut) 11:HOLD

Table 9. Quick Charge Register2 (06H)

Bit	Bit Name	R/W	Description
7:6	DI-_Input_Voltage	R	11:> 2.7V 10:2.0-2.7V 01:0.35V-2.0V 00:0-0.35V
5:4	DI+_Input_Voltage	R	11:> 2.7V 10:2.0-2.7V 01:0.35V-2.0V 00:0-0.35V
3:2	DI+_Output_Voltage	R/W	11:Floating(default) 10:3.3V 01:0.6V 00:0V
1:0	DI-_Output_Voltage	R/W	11:Floating(default) 10:3.3V 01:0.6V 00:0V

Table 9. Quick Charge Register3 (07H)

Bit	Bit Name	R/W	Description
7:6	Input_Voltage_Set	R/W	Set the input voltage to change VDPM and VIN OVP. 11:12V 10:9V 01:7V 00: 5V(Default)
5:4	Upstream_USB_type	R	After BC1.2 detection, the USB type is recorded. 11: nonstandard adapter 10: DCP 01: CDP 00: SDP
3	BC1.2_DET_DONE	R	Indicate the BC1.2 detection status. 1: done 0: not done
2	Downstream_device_QC_support	R	Indicate whether downstream device supports QC. 1: support 0: not support
1	Downstream_QC_EN	R/W	1:Enable QC2.0 and QC3.0 Detect 0:Disable QC2.0 and QC3.0 Detect(default)

0	Downstream_OUT_SEL	R/W	SYS output voltage control. 1:Set by REG05[4:2] 0:SY6992 set according DO+/DO- (default)

I2C Interface

SY6992 uses I2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address d4H, receiving control inputs from the master device like micro controller or a digital signal processor. The I2C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits).

Both SDA and SCL are bi-directional lines, connecting to the positive supply voltage via a current source or pull- up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

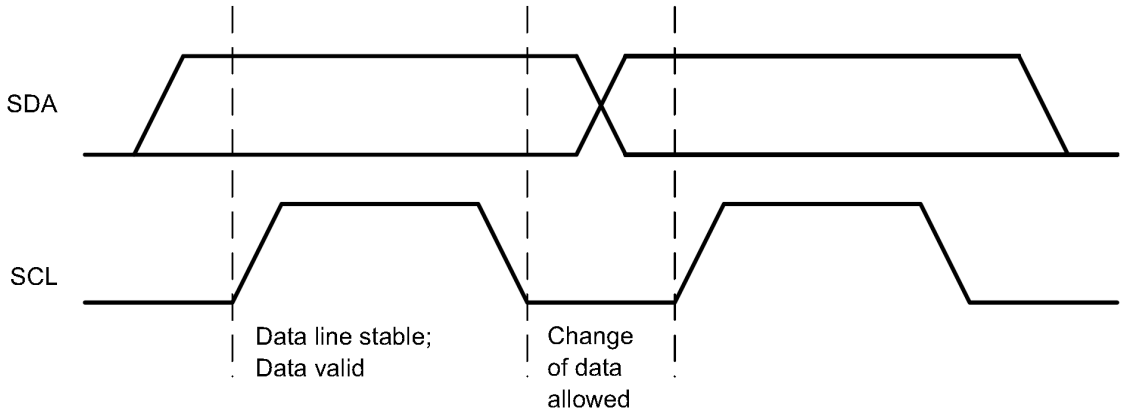


Figure 2. Bit Transfer on the I2C Bus

START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCl is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

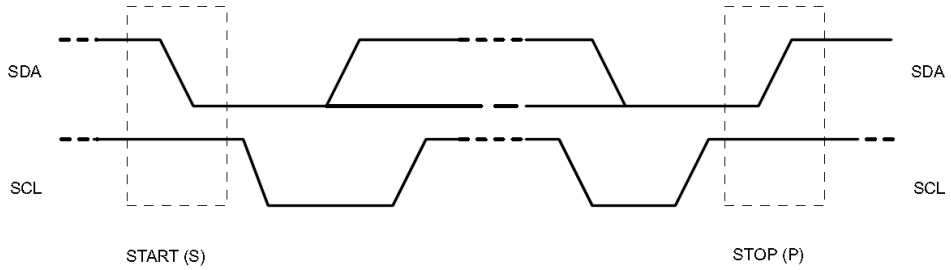


Figure 3. START and STOP conditions

Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

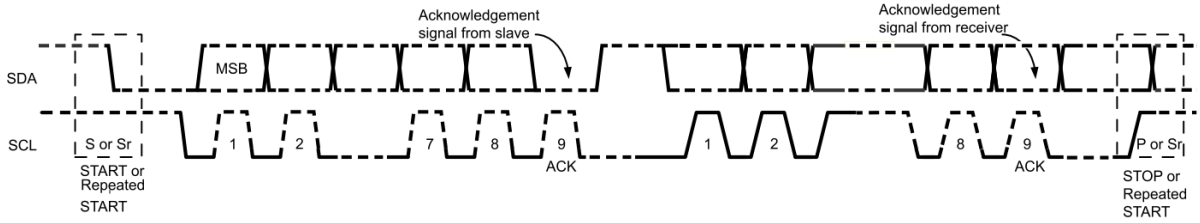


Figure 4. Data Transfer on the I2C Bus

Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

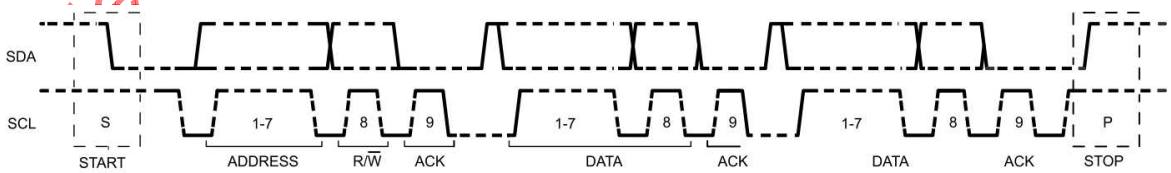


Figure 5. Complete Data Transfer

Single Read and Write

Figure 6. Single Write

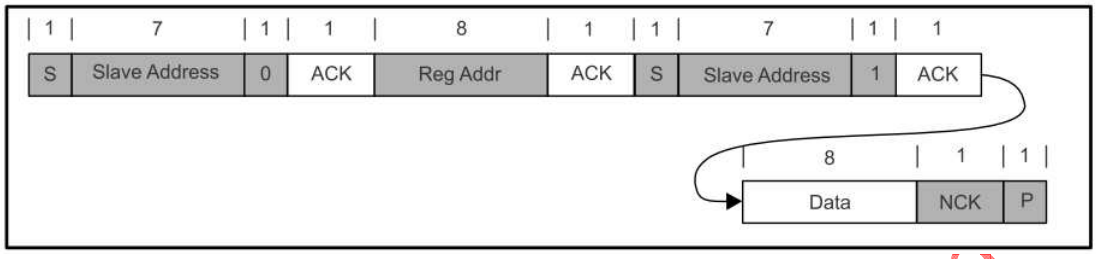
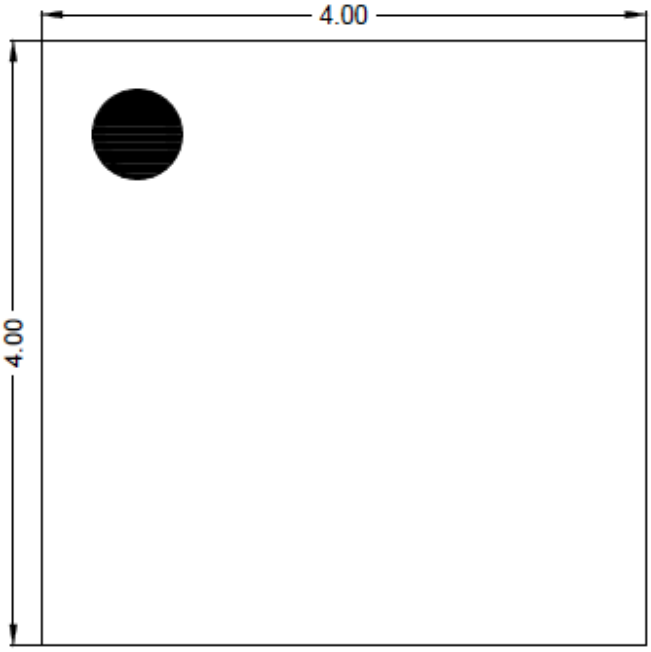


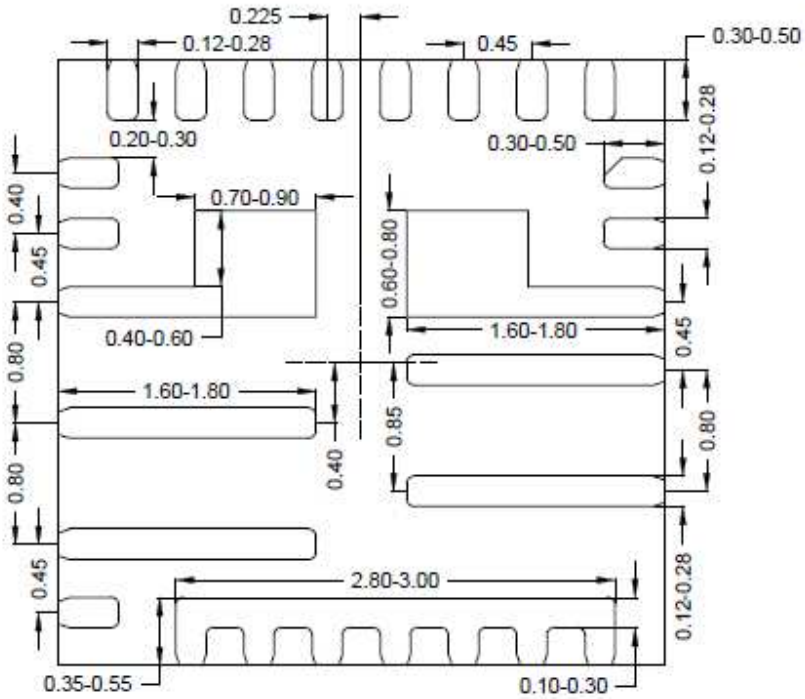
Figure 7. Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

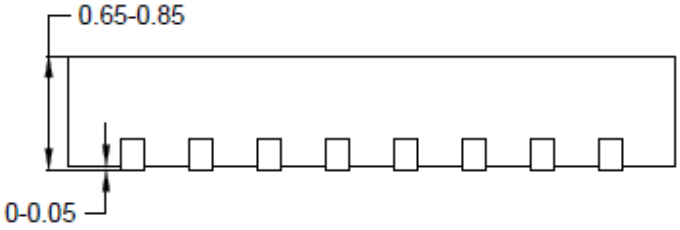
QFN4x4-20 Package Outline Drawing



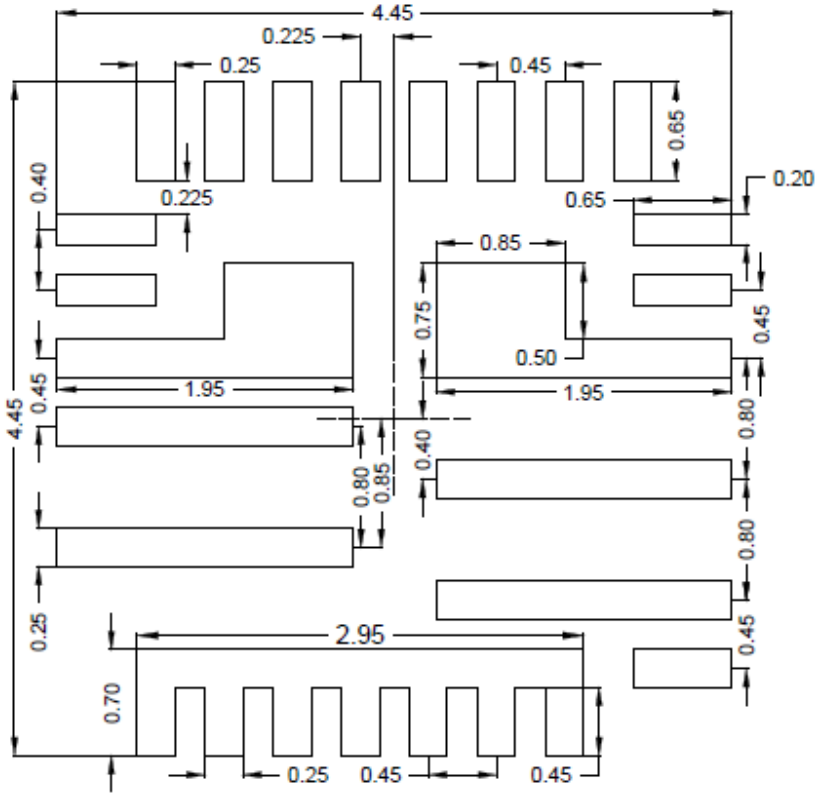
Top View



Bottom View



Side View

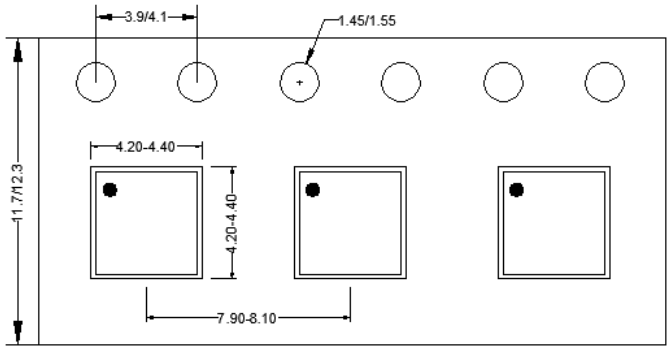


Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

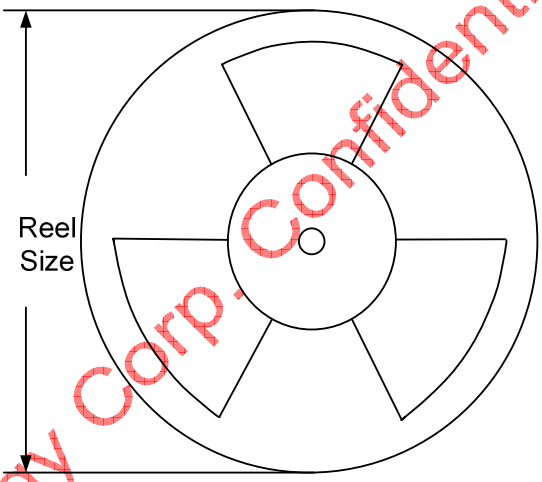
Taping & Reel Specification

1. QFN4x4 taping orientation



Feeding direction

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
QFN4x4	12	8	13"	400	400	5000

3. Others: NA