An EKG Instrumentation Amplifier Design Employing Common-Mode Feedback

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I. Introduction

With the rapid advancement in integrated circuit technology, wearable devices are also becoming drastically more capable and energy efficient. The ability to measure human-body related parameters has always been a strong focus of wearable devices. Among the many possible measurements, EKG stands out as one of the most well known and useful. EKG measures the electrical signal generated by the heart, using electrodes placed on human skin. The importance of portable and continuous EKG measurement is apparent, as it can help detect and, in some cases, prevent, many heart related health problems.

The human body is electrically noisy, therefore an instrumentation amplifier used for portable EKG measurements must exhibit a series of properties in order to achieve proper amplification. These include high differential mode gain, high CMRR, high input impedance, low noise, and from a practicality perspective, low power. In this report, we present an instrumentation amplifier design that meets all of the above requirements, with 39.7 dB $A_{v,dm}$, 123 dB CMRR at 60 Hz, 2.98 uV integrated input referred noise, and 2.7 uW power consumption.

II. Amplifier Design

The overall amplifier design adopted in this project uses the classic 3 op-amp structure with an additional op-amp for common-mode feedback (fig.1a). In this chapter, we will explain the general working principle of the amplifier, then go over the challenges encountered during the design process and the modifications and design choices that were made to overcome them.

The amplifier consists of two stages, the fully differential first stage has ideally infinite input impedance, provides some amount of differential mode gain, while keeping a unity common mode gain. The second stage provides some differential to single ended gain, while having some amount of common mode rejection. The CMFB circuit (also referred to as DRL circuit) reduces common mode interference seen at the amplifier input, and biases the human body to the correct DC voltage for the OTAs in the first stage. It utilizes the fully differential output of the first stage, acquiring the common mode signal by averaging the voltages on the two output rails. The common mode signal is then amplified by an auxiliary op-amp and fed back onto the body. This creates a negative feedback loop to suppress the common mode interference on the body. The open loop gain of both the forward path and the CMFB circuit are set by the ratio of feedback capacitors around the OTAs, the design decisions of setting these gains will be discussed later.

A. CMRR

While the two stages of amplifier themself have some common mode rejection, a preliminary simulation using ideal op-amps revealed that the intrinsic CMRR of the amplifier is far from enough to overcome the 60 Hz interference that the human body can pick up. The component mismatch in the feedback network can alone degrade the CMRR to around 55 dB. Therefore, the implementation of CMFB is necessary to boost the effective CMRR of the amplifier. Before implementing the design, we made the decision of using a capacitive feedback network to set the gain of the amplifier. Compared to using resistive feedback, this design has less common mode gain resulting from component mismatch, as capacitors in modern CMOS processes tend to have better matching than resistors. The use of capacitors also has the extra advantage of not introducing noise, which is the topic of discussion in the next section. One problem that came with using capacitive feedback is the lack of DC biasing for the OTAs. We added pseudo-resistors to achieve proper DC biasing level, as represented by the A blocks in the circuit diagram (fig. 1b).

The common-mode feedback network uses an auxiliary op-amp to amplify the common mode signal. Here, an op-amp, instead of OTA, is required, because the op-amp output must drive the electrode impedance in series with the body capacitance. The amplification device must have low output impedance to order to drive the body's voltage effectively. Therefore, we added a super source follower (SSF) to buffer the output of the CMFB OTA. The SSF has near unity gain and very low output impedance. Another challenge with the CMFB circuit is that a significant amount of current is required to cancel out the 1uA interference current. This current must come from the bias current of the SSF, it was experimentally determined that the SSF requires at least 1 uA of bias current to function correctly, this ended up accounting for the majority of the amplifier's power consumption.

Theoretically, higher open loop gain of the CMFB amplifier provides more common mode signal attenuation, and is therefore desirable. However, an open loop gain too high can lead to stability issues in close loop. We performed Cadence stb analysis to find the loop gain and gain & phase margin. The CMFB open loop gain is chosen to be as large as possible while maintaining a reasonable amount of gain and phase margin (fig. 3).

B. Noise

The biggest challenge we faced in designing the amplifier is minimizing noise. Noise can come from resistors and amplifying components, such as the input MOSFET stacks in the OTAs. Many design choices are made to minimize input referred noise, apart from using capacitive feedback. The OTAs are designed with the simple 5 transistor structure in order to reduce possible noise sources. The per stage gain of the amplifier is chosen to be 28 dB + 12 dB. Since the first stage's output noise is amplified by the second stage, a lower second stage gain helps to reduce total output noise. The first stage OTAs received special attention, as they are the main noise contributors. The MOSFETs in them are sized very large to reduce flicker noise (fig. 1c). Their bias current is also increased compared to the other OTAs to reduce channel noise component when referred to input. Another effective way to reduce integrated output noise is by limiting bandwidth. The extra capacitors at the output of each stage are used to add extra poles to the transfer function so that the gain falls off faster past 250 Hz. With the combined effect of all the above measures, we are able to meet the noise spec while keeping our power consumption significantly lower than spec (fig 4).

III. Performance

The amplifier runs on 1.8 V supply voltage, uses a 100nA ideal current source and no other ideal sources. The power consumption is 2.7 uW, exact current allocation can be seen in fig. 1d. The midband gain is measured to be 39.7 dB, with a bandwidth of 74 mHz to 273 Hz. At 60 Hz, the CMRR of the forward path is 51.5 dB, the DRL circuit provides an extra 71.6 dB of input common mode signal attenuation, the effective CMRR of the amplifier is therefore 123 dB (fig. 2). The integrated input referred noise is 2.98 uV. The gain & phase margins of the CMFB circuit are measured to be 3.35 dB and 18.1° respectively.

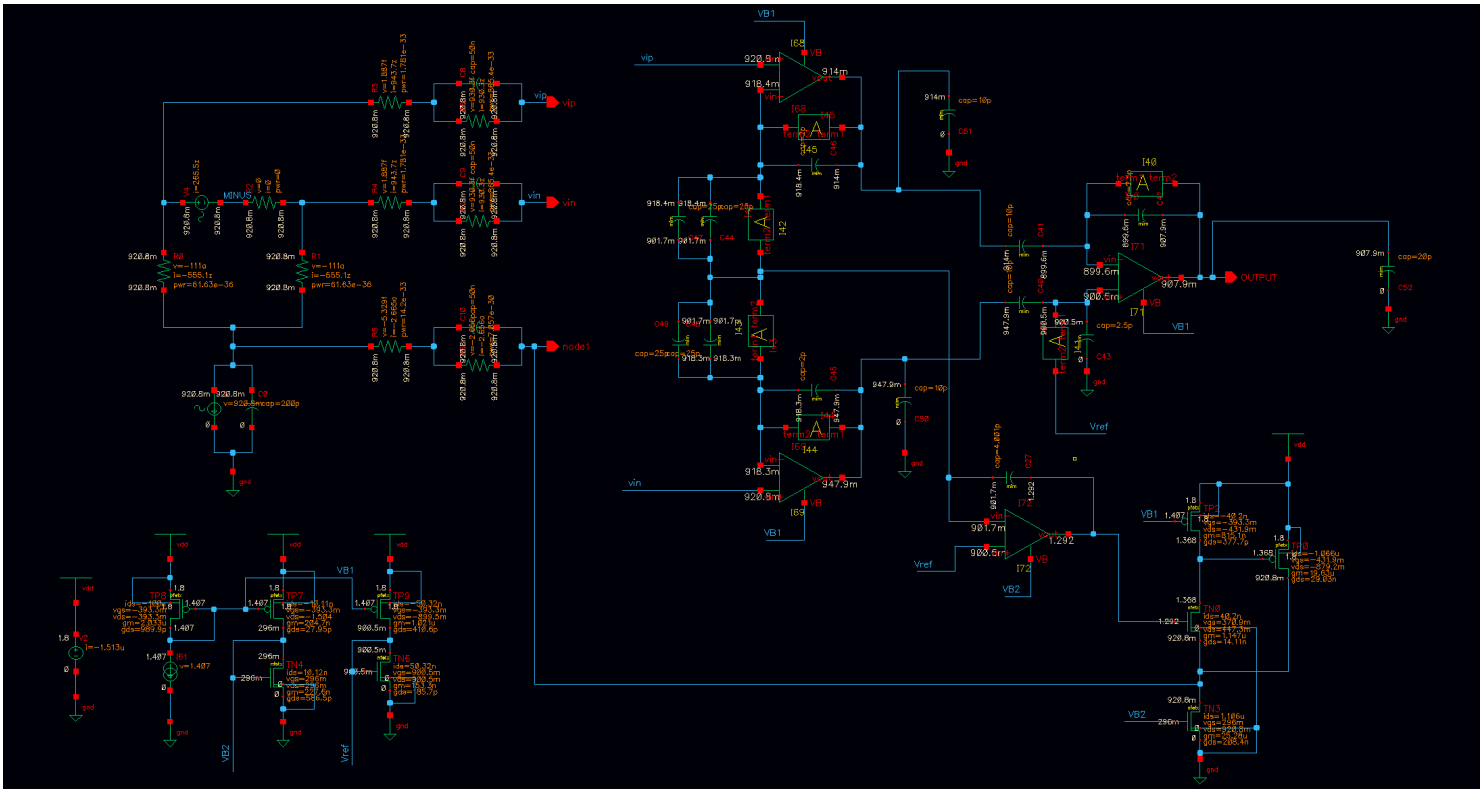
A robust design must be tolerant to process variation and mismatch. For example, we want the CMFB loop to always be stable, this requires designing for enough gain and phase margin to account for variation. We tested many performance specs using monte carlo analysis, as summarized in fig. 5 and Table 1. These mismatch simulations showed that even in the worst cases, our design still meets almost all specifications, and even exceeds specification in many aspect s.

IIII. Conclusion

Overall, this project is successful. The highlights of our design include very high CMRR and low power consumption. The high CMRR is the result of using capacitive feedback and the CMFB circuit. We are able to achieve low power consumption thanks to the various techniques employed to minimize noise, as described in the noise section. Without them, we would have to burn a lot more current through the first stage OTAs to meet the noise specification. In hindsight, we could have experimented with using lower V_{DD}, which may further lower power consumption.

IIII. Acknowledgements

We would like to thank Professor Mercier and Vineel for providing us with guidance throughout the entire course of the project.



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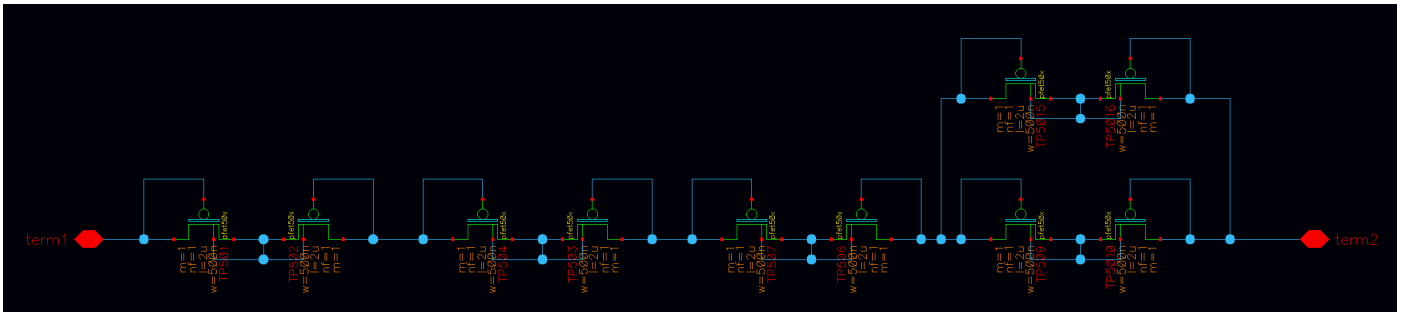

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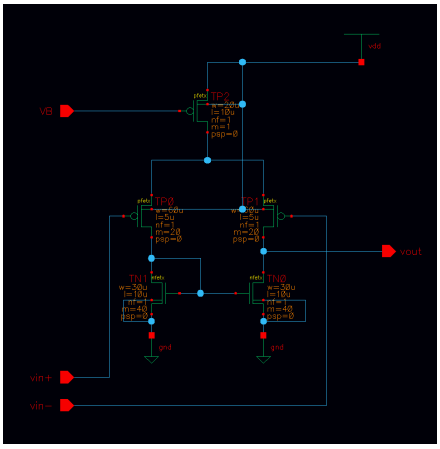
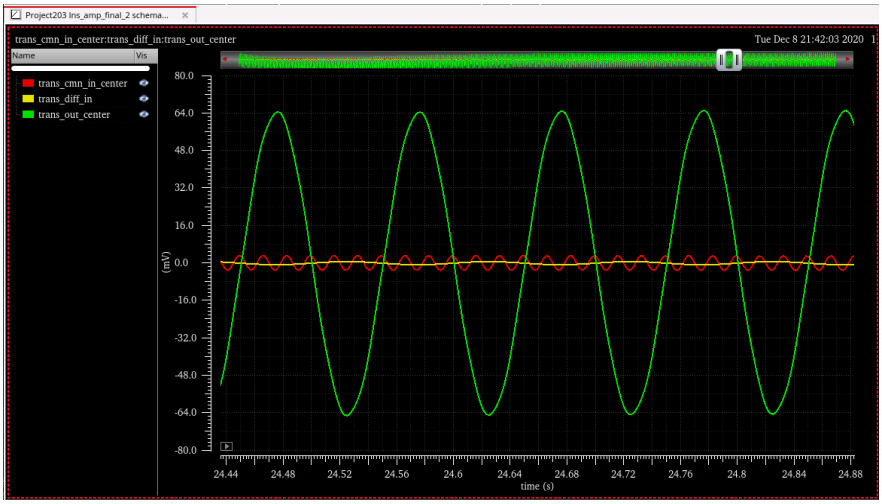


(c)

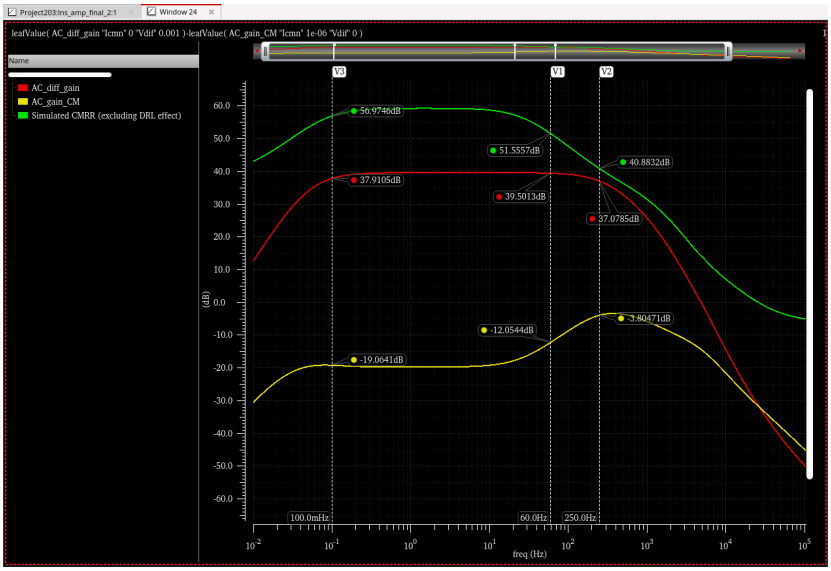
V_{DD} = 1.8V	Current	Power
Forward path OTAs	225 nA	0.405 uW
CMFB OTA+SSF	1127 nA	2.023 uW
Biasing network	160 nA	0.288 uW
Total	1512 nA	2.72 uW

(d)

Figure 1. (a) Circuit schematic with DC operating point. Bottom left corner shows total current (1.513 uA) and supply voltage (1.8 V). **(b)** Pseudo resistor schematic. **(c)** First stage OTA schematic. **(d)** Current and power allocation table.



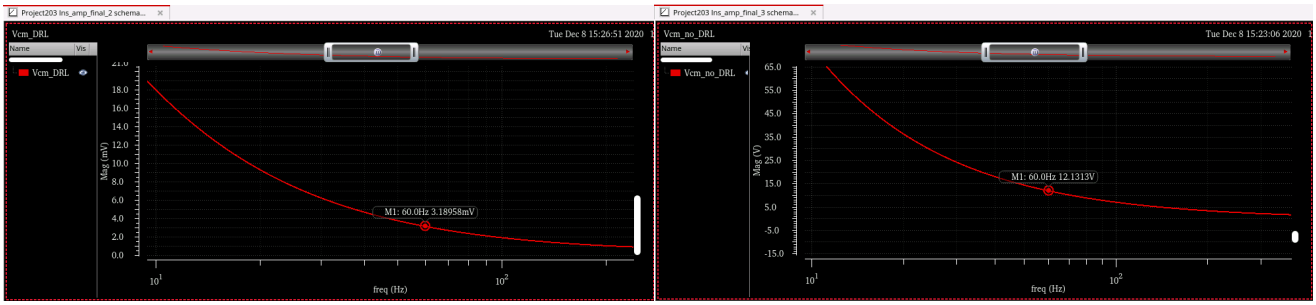
(a)



Outputs

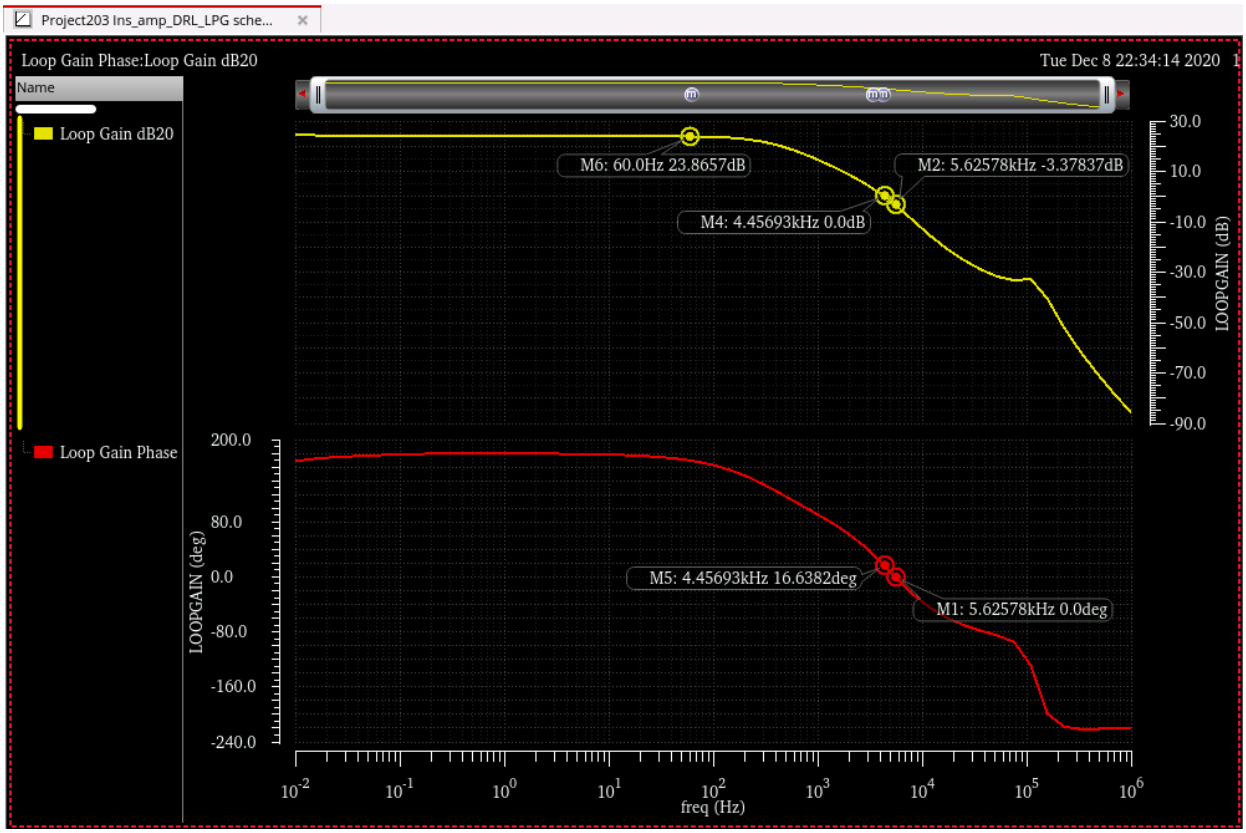
	Name/Signal/Expr	Value	Plot	Save				
14	BW_L	74.28m	☑	☐	Project203:I...	BW_L	expr	cross(AC_diff_gain (ymax(AC_diff_gain) - 3) 1 "rising" nil nil nil)
15	BW_H	273.2	☑	☐	Project203:I...	BW_H	expr	cross(AC_diff_gain (ymax(AC_diff_gain) - 3) 1 "falling" nil nil nil)

(b)



(c)

Figure 2. (a) Transient response minus DC offset. **(b)** AC differential mode gain (and BW), common mode gain, and CMRR of forward path (without DRL's effect). Forward CMRR is calculated by CMRR [dB] = $A_{v,dm}$ [dB] - $A_{v,cm}$ [dB]. **(c)** Input common mode magnitude at 60 Hz with and without DRL. Common mode attenuation from DRL in dB is calculated by $20\log_{10}(V_{CM,DRL}/V_{CM,noDRL})$ = -71.6 dB. The input common mode without DRL is measured by disconnecting the DRL from the right leg electrode, leaving the body voltage "floating". The input voltage is therefore only determined by the 60 Hz current source.



(a)

Outputs

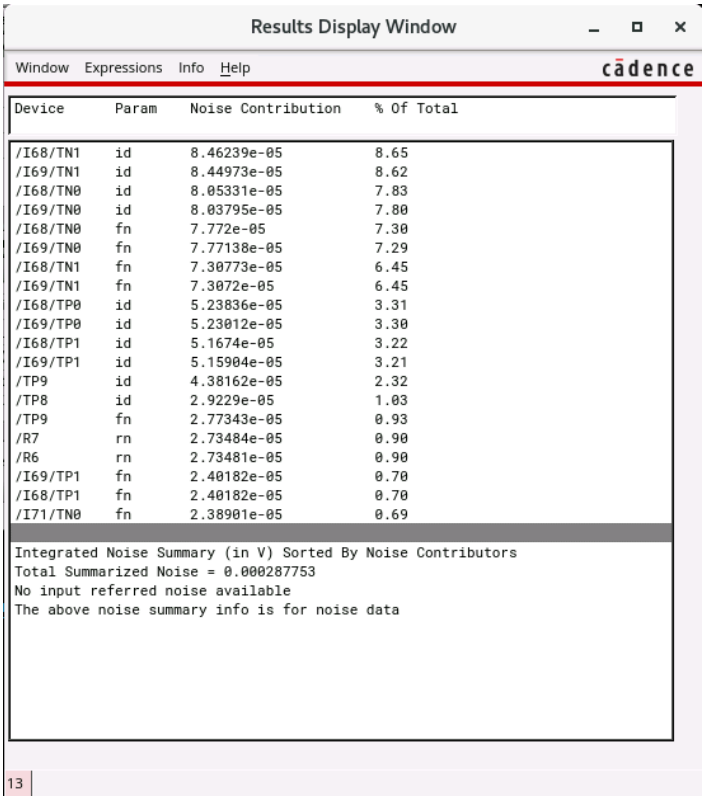
	Name/Signal/Expr	Value	Plot	Save	Save Options
1	Loop Gain dB20		☑	☐	
2	Loop Gain Phase		☑	☐	
3	PM	18.11	☑	☐	
4	GM	3.349	☑	☐	

(b)

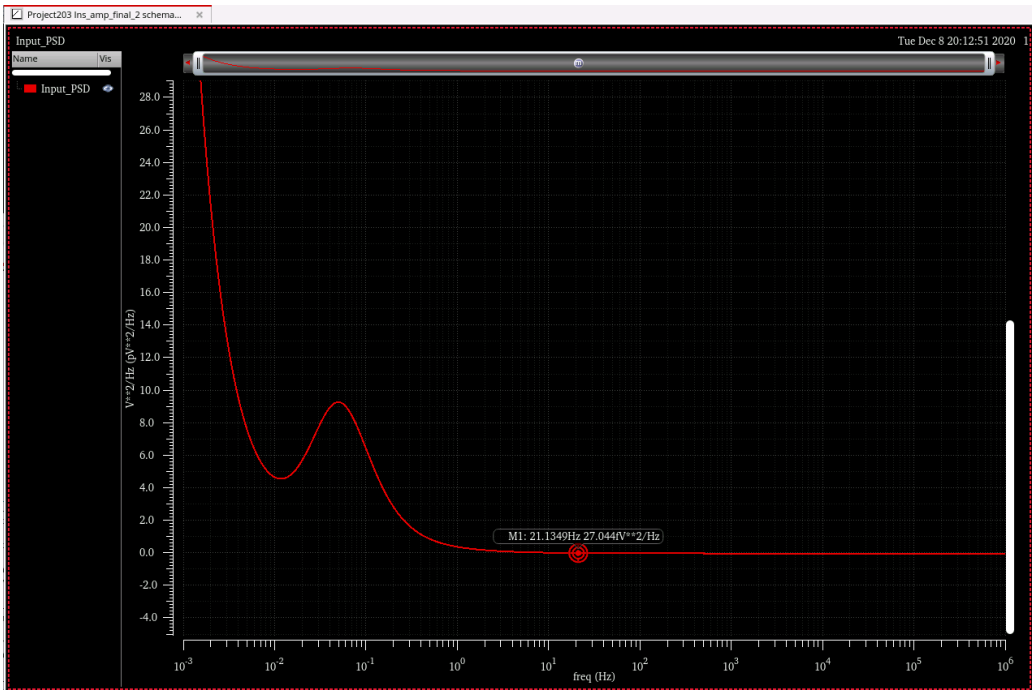
Project203:Ins_amp_DRL_LPG:1	GM	expr	(- gainMargin((- getData("loopGain" ?result "stb"))))	point
Project203:Ins_amp_DRL_LPG:1	PM	expr	phaseMargin((- getData("loopGain" ?result "stb")))	point

(c)

Figure 3. (a) magnitude and phase of CMFB loop gain using stb analysis. Cadence's stb analysis seems to give -1*loop gain, so the phase is 180 degree off from the convention we use. The open loop gain (equal to loop gain) is set to 24 dB. **(b)** Phase and gain margin of the CMFB loop, calculated using Cadence calculator's built in functions. The result seems to be slightly different from reading directly from the plot, for unknown reasons. **(c)** The calculator expressions used to find phase and gain margin.

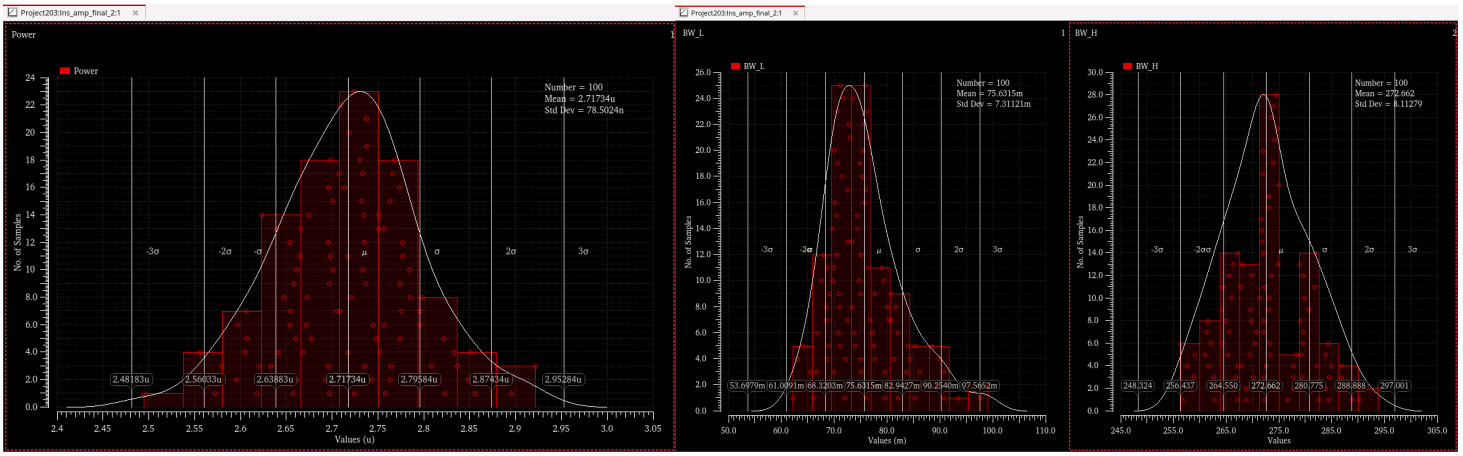


(a)

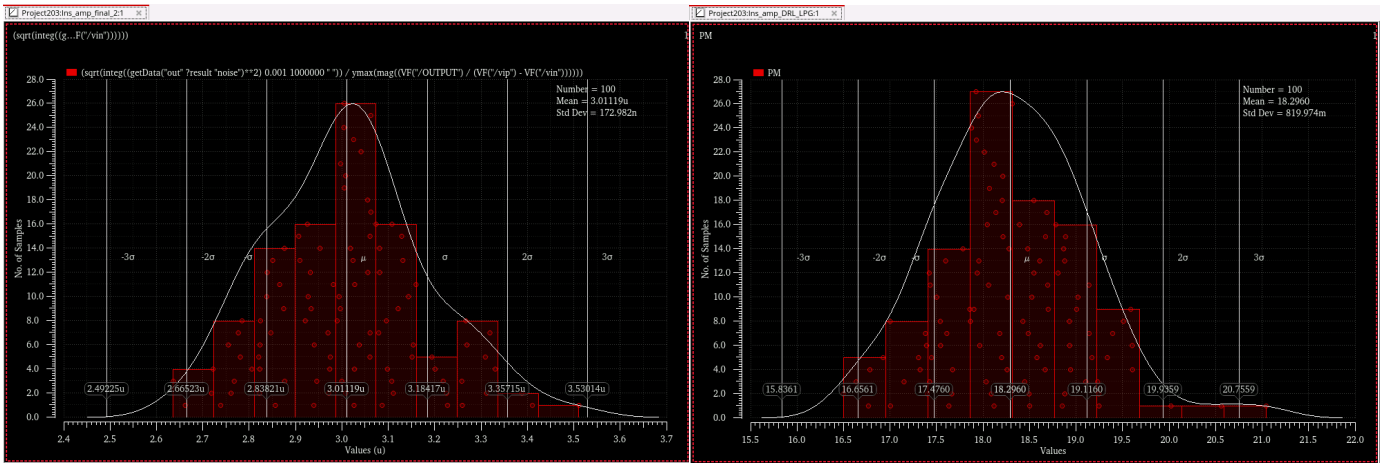


(b)

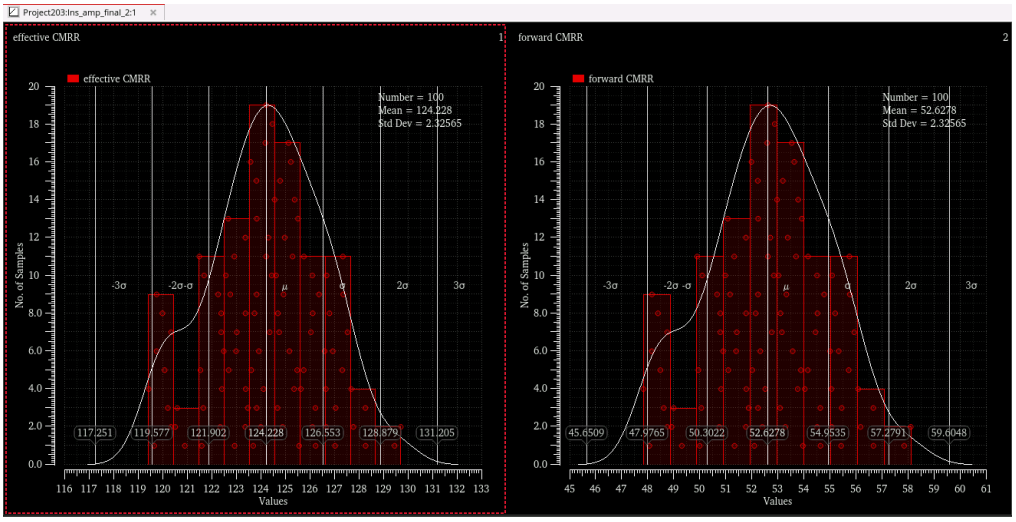
Figure 4. (a) Summary for total output noise, from 1mHz to 1MHz. The total input referred noise can be calculated by dividing the output noise by $A_{v,dm}$=39.7 dB. Therefore, $V_{n,in,rms}$ = 287.7 uV/96.6 = 2.978 uV. **(b)** Input PSD from 1mHz to 1MHz, it's hard to identify the white noise component as the transfer function cut off is rather early, and the flicker noise is masking the white noise at lower frequencies.



(a) (b)



(c) (d)



(e)

Figure 5. N = 100 Monte Carlo simulation showing **(a)** Power. **(b)** Bandwidth. **(c)** Total input referred noise. **(d)** Phase margin. **(e)** Forward CMRR and effective CMRR. The CMRR expression used for Monte Carlo assumes that the differential gain and DRL common mode suppression are constant, in other words, only the variation in common mode gain is simulated. It was tested that the differential gain at 60 Hz only varys by 0.5 dB (3 sigma). The amount of common mode suppression is dependent mainly on the open loop gain of the CMFB circuit, which should also stay relatively constant with mismatch. Therefore, the assumptions made in the CMRR mismatch simulation should be reasonably accurate.

	Ideal performance	Worst case mismatch performance	Best case mismatch performance
Power	2.7 uW	2.9 uW	2.5 uW
Bandwidth	74 mHz - 273 Hz	97 mHz and 256Hz *	61 mHz and 295 Hz *
Gain	39.7 dB	39.5 dB	40 dB
CMRR, without DRL	51.5 dB	48 dB	58 dB
CMRR, with DRL	123.1 dB	119 dB	130 dB
Total input referred noise	2.978 uV	3.5 uV	2.6 uV
DRL phase margin	18.1 degrees	15.8 degrees	21 degrees
DRL gain margin	3.35 dB	3 dB	3.9 dB
NEF	3.435	4.04	3
Voltage sources used	One 1.8V voltage source	-	-
Total value of capacitance	173 pF	-	-

*The best and worst case low-end and high-end BW are taken from a N = 100 Monte Carlo simulation, however, the recorded low and high BW values may not come from a single sub-simulation.

Table 1. Performance summary including mismatch performance