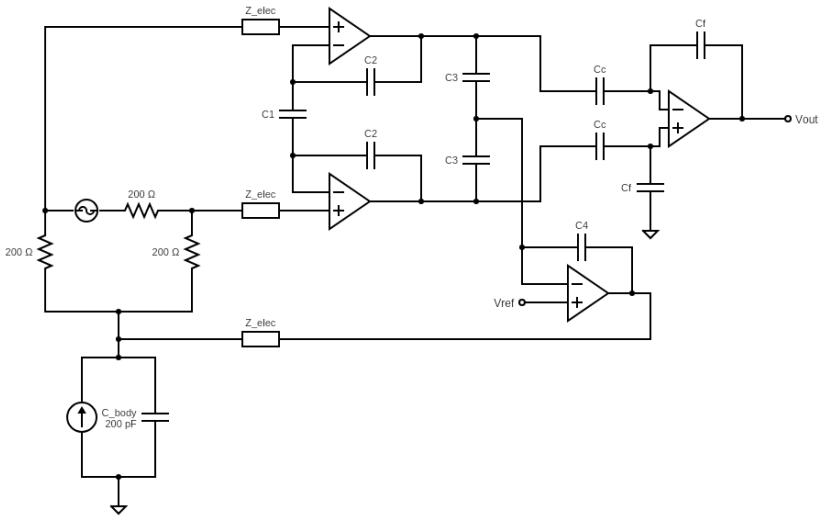
ECE 203 Project Progress Report

So far, we have built and simulated the entire instrumentation amplifier with DRL using ideal op-amp models. The measured performance include gain, CMRR, and mismatch.

The circuit design we adopted is very similar to the 3 op-amp + DRL structure from lecture, except the feedback resistors are replaced with capacitors in order to reduce component mismatch.




For now, we chose the first stage gain to be 40 dB and second stage gain to be 0 dB, this is to minimize the effect of common mode gain due to mismatch. In practice, we may need to lower the first stage gain due to second stage's input linear range concern.

The differential mode gain formula is given by

First stage: $H_1 = \frac{C_2+2C_1}{C_2}$, Second stage: $H_2 = -\frac{C_C}{C_f}$

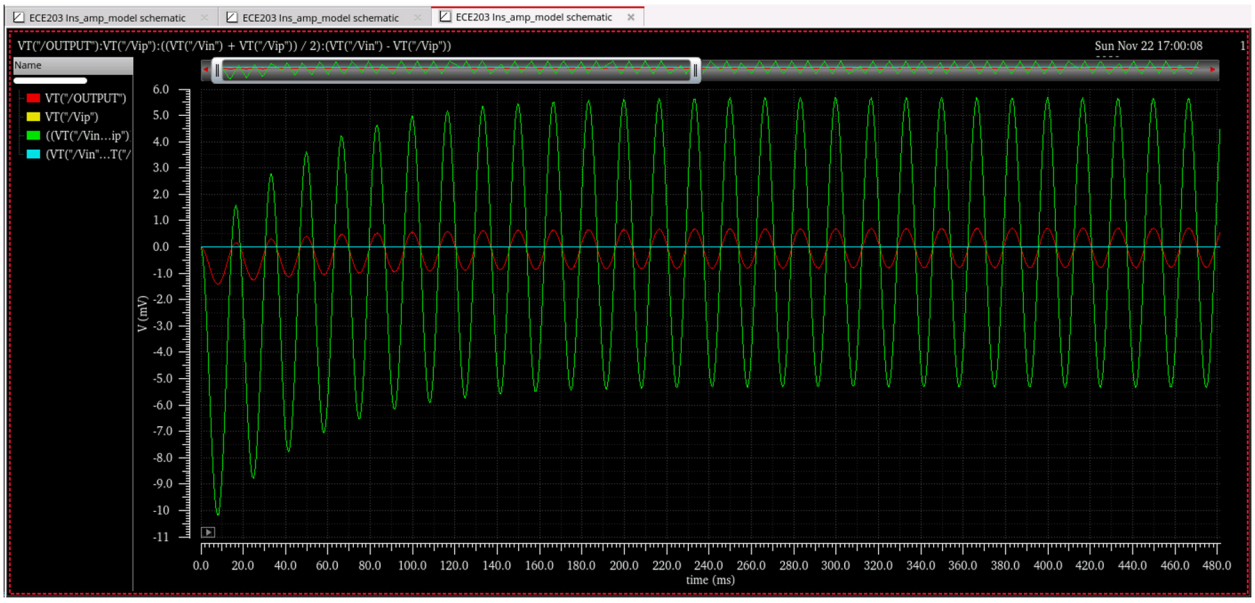
With the DRL circuit, we can calculate the $V_{CM}$ voltage in terms of $I_{in}$, $C_4$, $C_3$, $C_{body}$ and $Z_{elec}$

$$V_{CM} = I_{in}\frac{1}{sC_{body} + \frac{A+1}{Z_{elec}}}, \qquad where\ A = 2\frac{C_3}{C_4}$$

Without DRL, $V_{CM}$ becomes

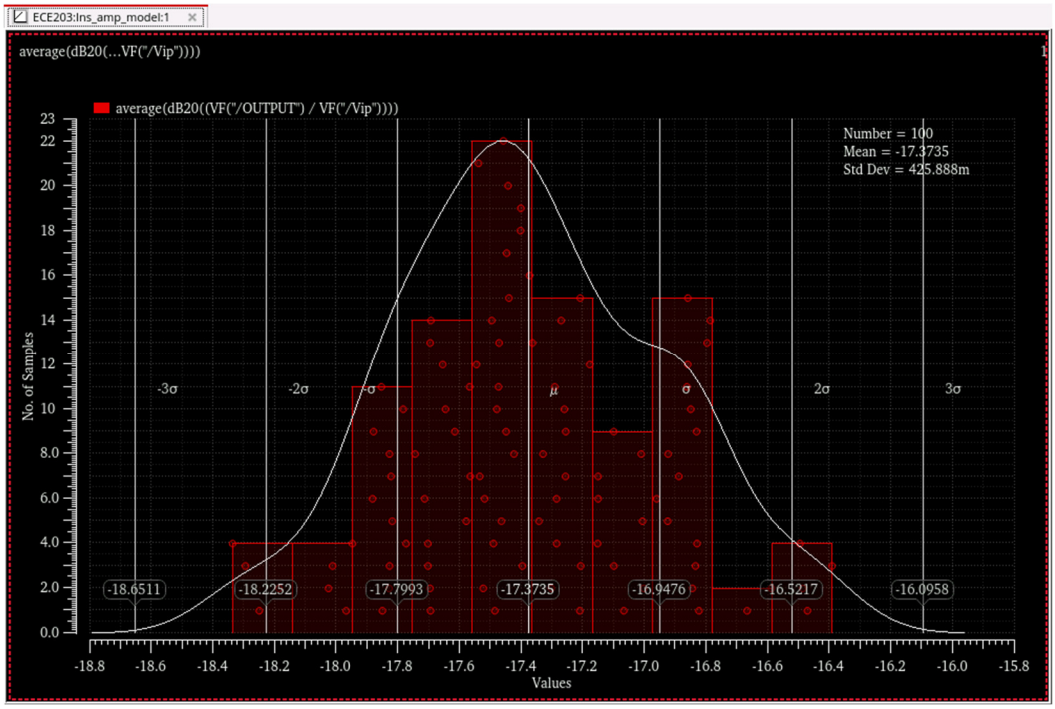
$$V_{CM} = I_{in}\frac{1}{sC_{body}}$$

The DRL feedback circuit offers a huge reduction in $V_{CM}$ voltage. In our preliminary simulations, we used A = 8. Hand analysis suggests that at 60 Hz, $V_{CM}$ is 13.3 V without DRL feedback, and only 5.9 mV with DRL. This result is confirmed by simulation. Larger values of A should be able to achieve much lower $V_{CM}$ still.




$V_{CM}$ (green) at input, and output (red) when $V_{DM} = 0$

All capacitors in our circuit are mim capacitors, which is affected by mismatch. We ran a N = 100 Monte Carlo simulation to figure out the common mode gain with capacitor mismatch. Interestingly, the results are centered tightly around -17.4 dB, even the best case only achieved a -18.3 dB $A_{V,CM}$.




With the differential mode gain being 40 dB, this means the CMRR is 40+17.4 = 57.4 dB, which is not enough. Thankfully, DRL feedback comes to the rescue, driving the input $V_{CM}$ to a very low level. In our simulations, the DRL circuit drives $V_{CM}$ from 13.1V to 5.6 mV, this is a -67 dB

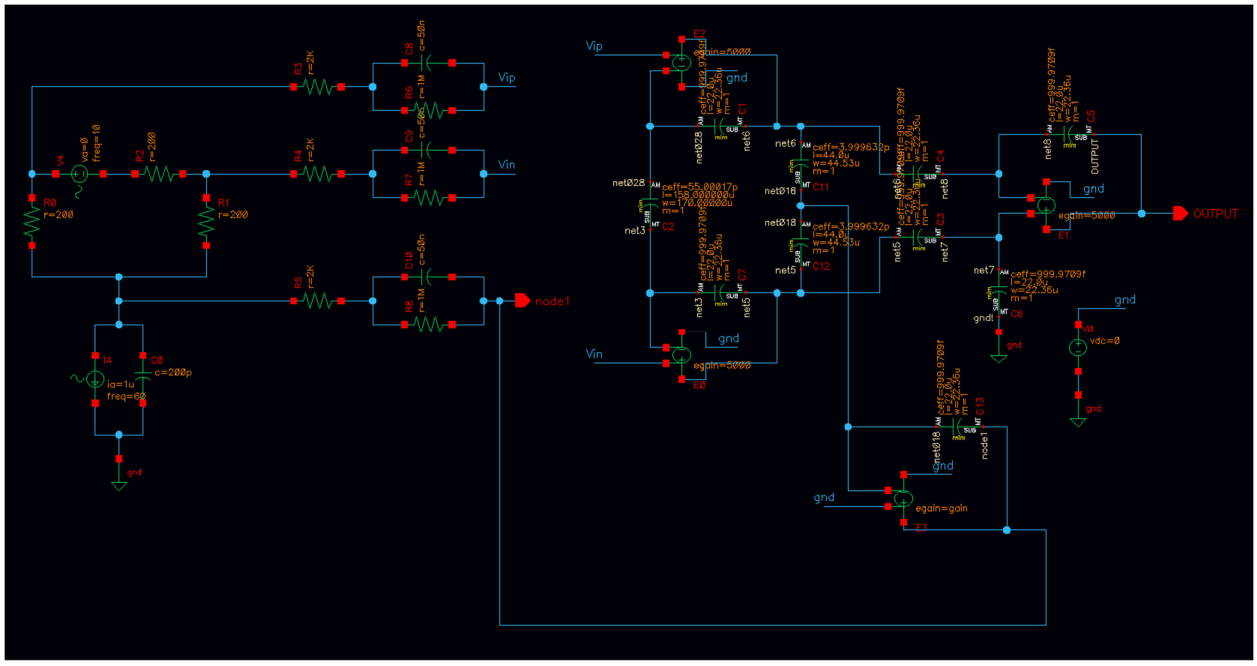
reduction in $V_{CM}$ magnitude. Add the effect of DRL circuit to CMRR, and we have an effective CMRR of ~124 dB! Though we do have to consider that in reality, the effective CMRR may be significantly lower because of op-amp nonidealities.

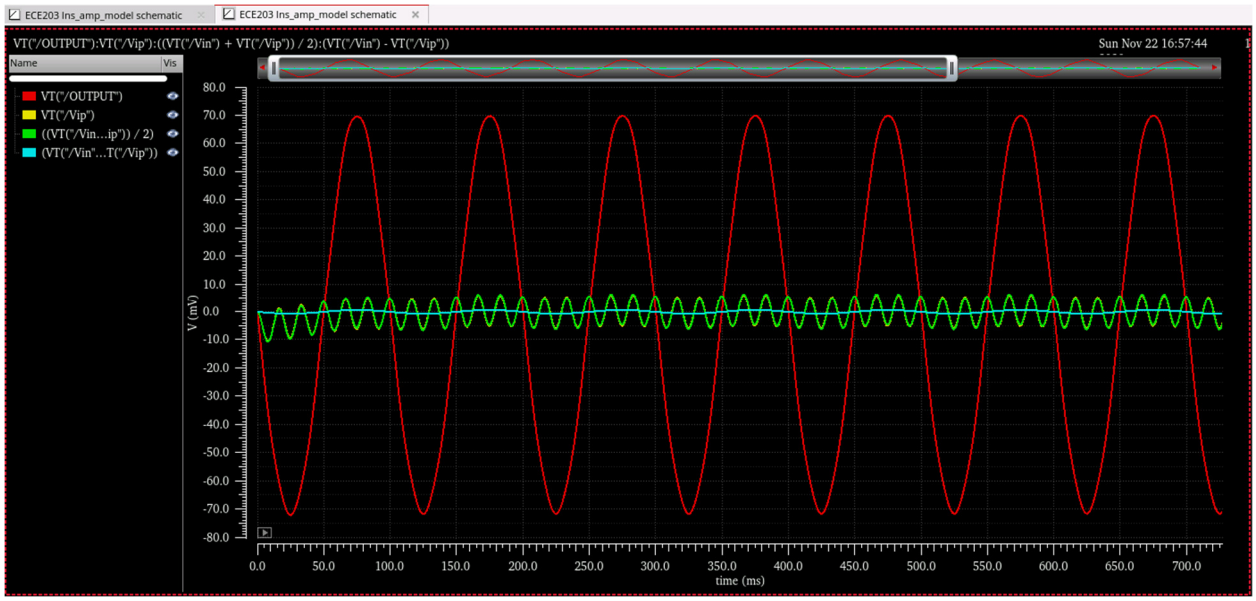
Here is a summary of what we have measured so far:

| | |
|---|---|
| Differential mode gain | 40 dB |
| Common mode gain | -17.4 dB |
| CMRR without DRL | 57.4 dB |
| Effective CMRR with DRL | 124.8 dB |

There are a few things we couldn't measure, such as common mode feedback stability, amplifier bandwidth, noise and power consumption. These require knowledge of op-amp performance. Therefore, our next step is to design the op-amp and biasing network, then incorporating them into our circuit model.

Finally, here is the screenshot of our circuit schematic and a transient simulation with both common and differential mode input.






Input differential mode (cyan), input common mode (green), output (red)