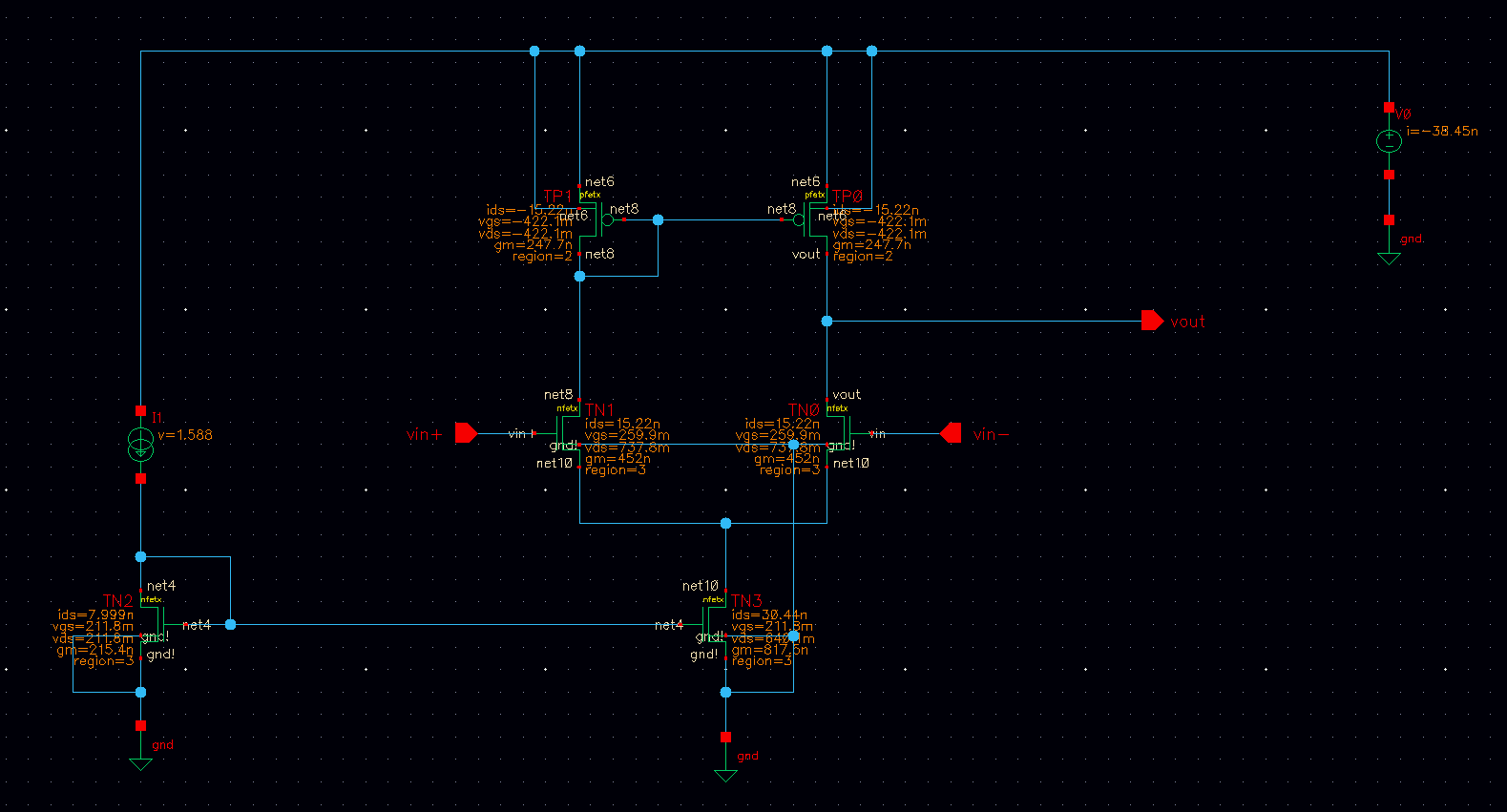
Problem 2.

In the past week we designed the OTAs, a super source follower to use for the DRL circuit, and finished the DC biasing of the entire amplifier. The amplifier can now operate correctly in fully differential mode, however, the DRL circuit seems to cause some stability problem once common mode interference is added.

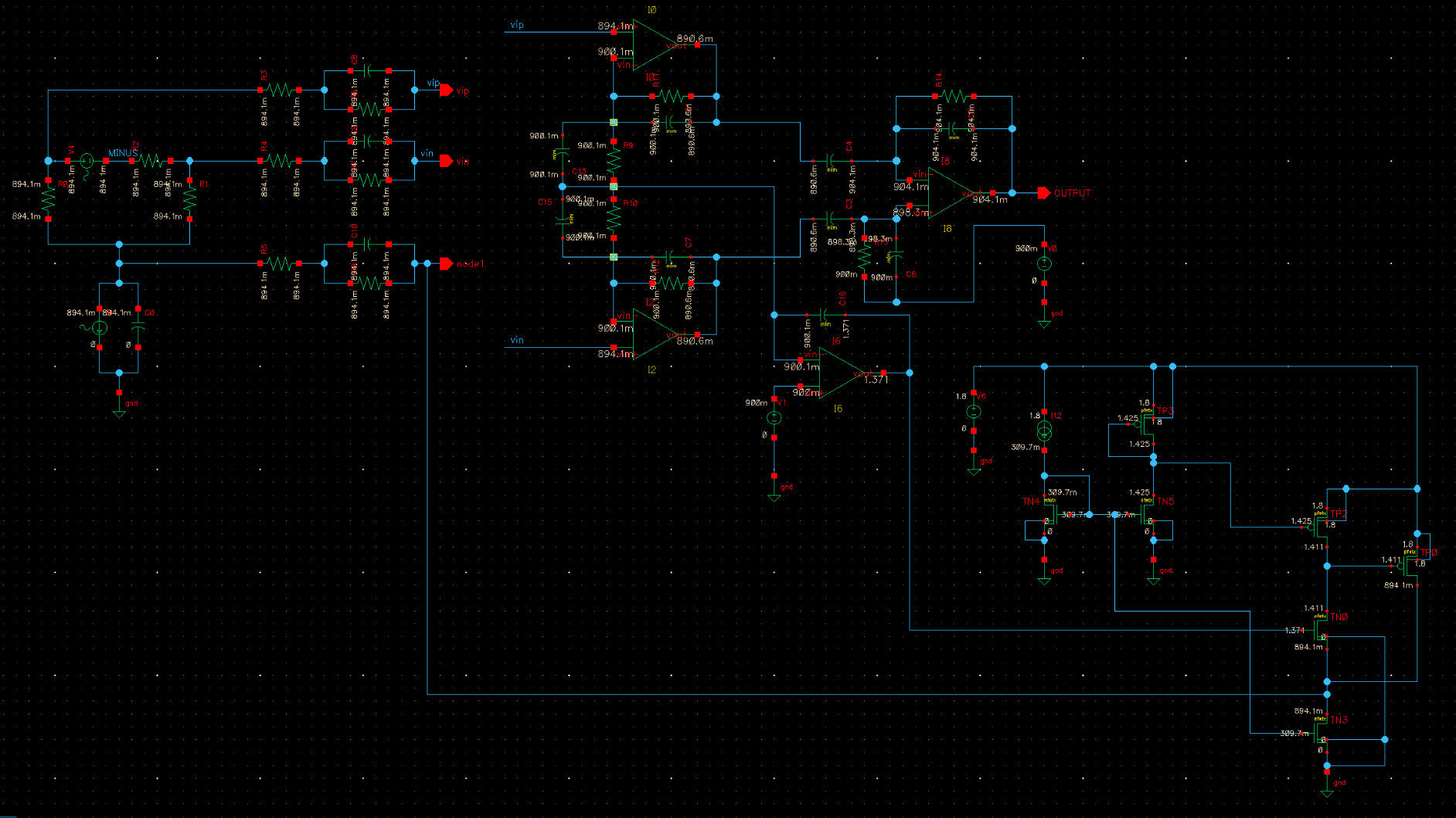
The OTA is a classic 5 transistor structure with NMOS inputs. For noise considerations, the PMOS are biased in Saturation region, while the other transistors are biased in sub-threshold region. The differential mode gain is 39 dB, BW = 46 Khz.



Because the OTA’s gain is 39 dB, the amplifier’s single stage gain (achieved using feedback) will need to be much lower. We redesigned the amplifier to have 20 dB gain each stage, instead of the 40 dB + 0 dB design before.

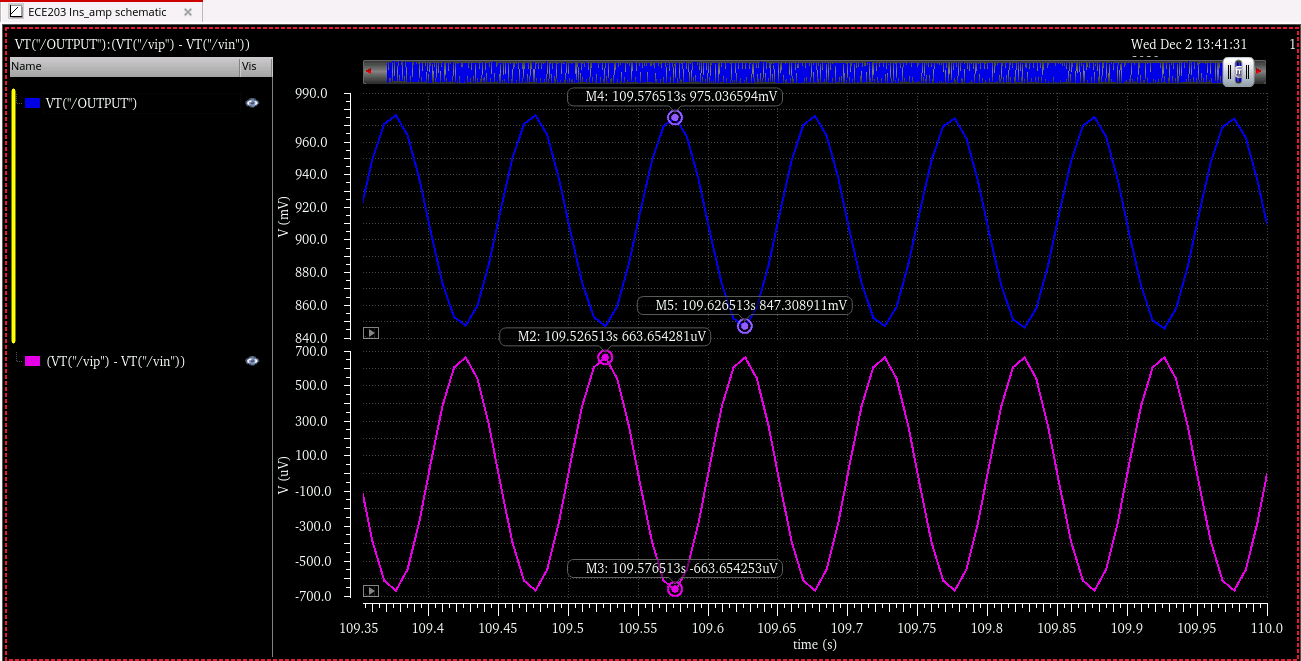
The DRL circuit is driving a relatively small impedance. The OTA has a high output impedance and therefore require a buffer stage to avoid reducing gain. We designed the super source follower circuit to buffer the OTA output (same circuit as in the midterm). This circuit has close to 1 gain, and only ~10 kohm of output resistance.

We put together the entire circuit and achieved the correct DC biasing level. For now, we used ideal resistors for DC biasing, but plan to later change to MOS pseudo-resistors.



We also used multiple ideal current and voltage sources for biasing, but later plan to combine all the OTAs and Super SF to use a single biasing network.

Finally, here is the transient simulation showing the differential mode gain, with common mode interference disabled. The DRL still have some stability issues that needs to be resolved.



The next step would be to fix the DRL circuit, measure the CMRR, noise and power performances, and doing further optimizations.