The very first step our team took was to divide the entire circuit into a few subparts. After careful analysis, the circuit was split into three major parts: The bias circuit, the folded cascode stage, and the common source stage. The gain was entirely determined by the folded cascode and the CS stages. And the bias circuit acted like a voltage and current source that was used to bias the folded cascode stage and the common source stage.

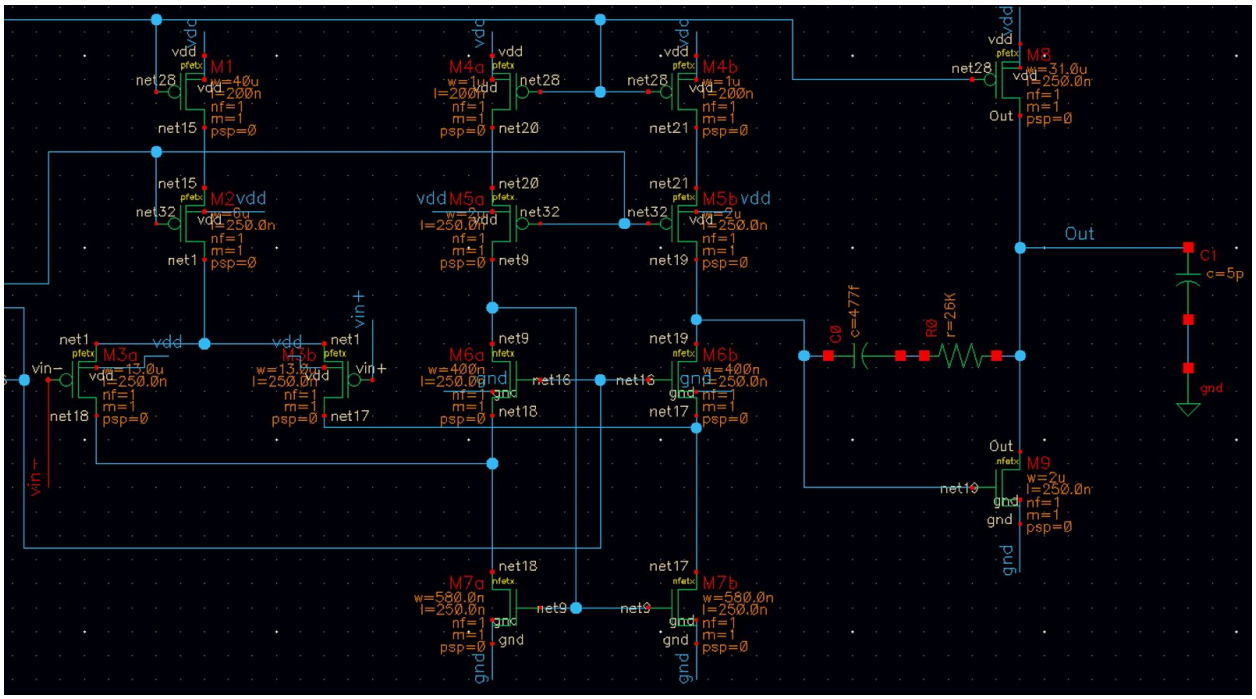
Our team put our focus on the folded cascode and common source stages first. The role of the bias circuits was replaced by a bunch of ideal voltage sources first. We first calculated some node voltages that required the bias voltage sources such as the nodes between M4a and M4b, the node between M5a and M5b, and the node between M6a and M6b. We assumed some appropriate overdrive voltages for the transistors and calculated some other key node voltages with the knowns. We also picked a value in the input common mode range to run the nominal test. We did not expect a large gain as the large gain would mess up the unity bandwidth. Since the folded cascode tended to provide more gain, our team split the gain to 50dB for the folded cascode stage and 20 dB for the CS stage to reach the requirement of 70dB.

Next we tried to locate the positions of the dominant pole and non-dominant pole to meet the constraints of the phase margin, gain margin, and unity gain bandwidth. We tried to push the dominant pole as close as to the imaginary axis and we also know that the frequency of the non-dominant pole is much larger than the dominant pole. Another insight was that Cc will give a rise to the zero so that a means to mitigate the zero's effect is necessary. We can either push the zero further away to the infinity or we can cancel out the zero with the non-dominant pole, the one who has a major effect on phase margin, by determining the value of the Rc.

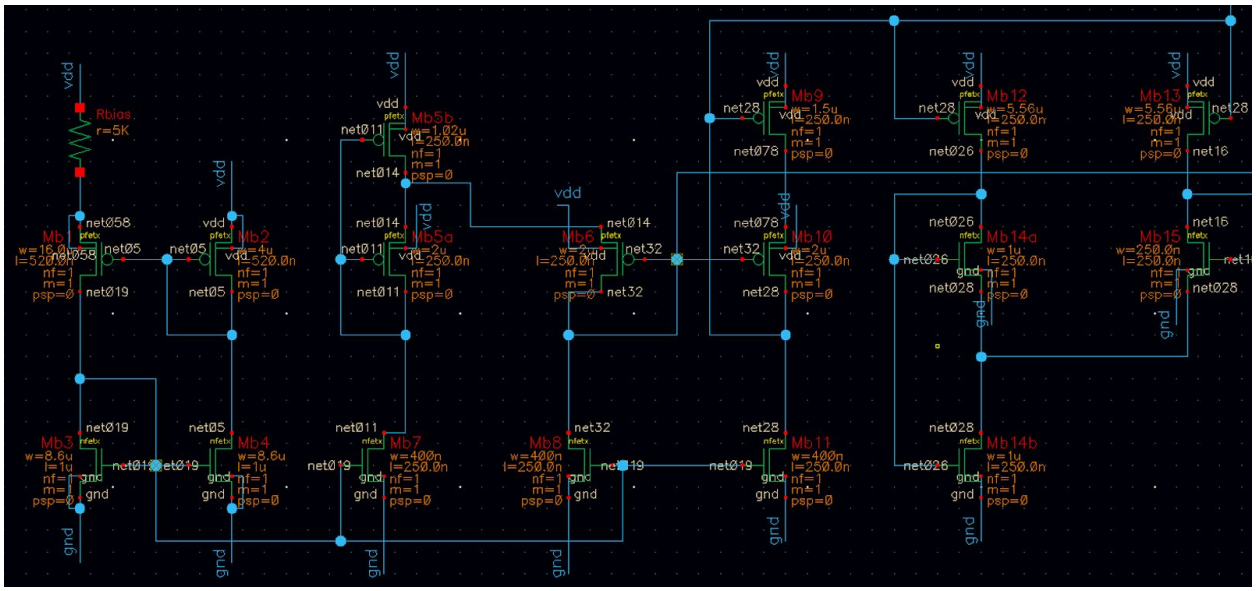
For the design of the bias circuit, our team decides to construct the circuit from right to left towards the constant gm part. We set the current quite small in order to meet the power constraint. The key parts in the bias circuit were the nodes that led to bias the folded cascode and CS circuits. Our main goal here was to set those nodes to the voltages that we were used to bias the folded cascode and CS circuit so that those stages could function properly just as we used the ideal voltage sources to bias them. We also noticed that since most of the transistors in the bias circuit were either current mirrors and diodes connected, they should all be in saturation except for Mb5b and Mb14b. Also we kept m<20 in the constant gm circuit. Another crucial step was to first estimate the gate voltage between Mb8 and Mb11 and bias that node to fulfill the desired node voltages at Mb6 and Mb15 which biased the two stages. So what we needed to do was to construct a constant gm circuit that can provide a voltage at the gate Mb3 that led to the node between Mb8 and Mb11 so that the same results could be obtained.

Schematic of our final design with component values

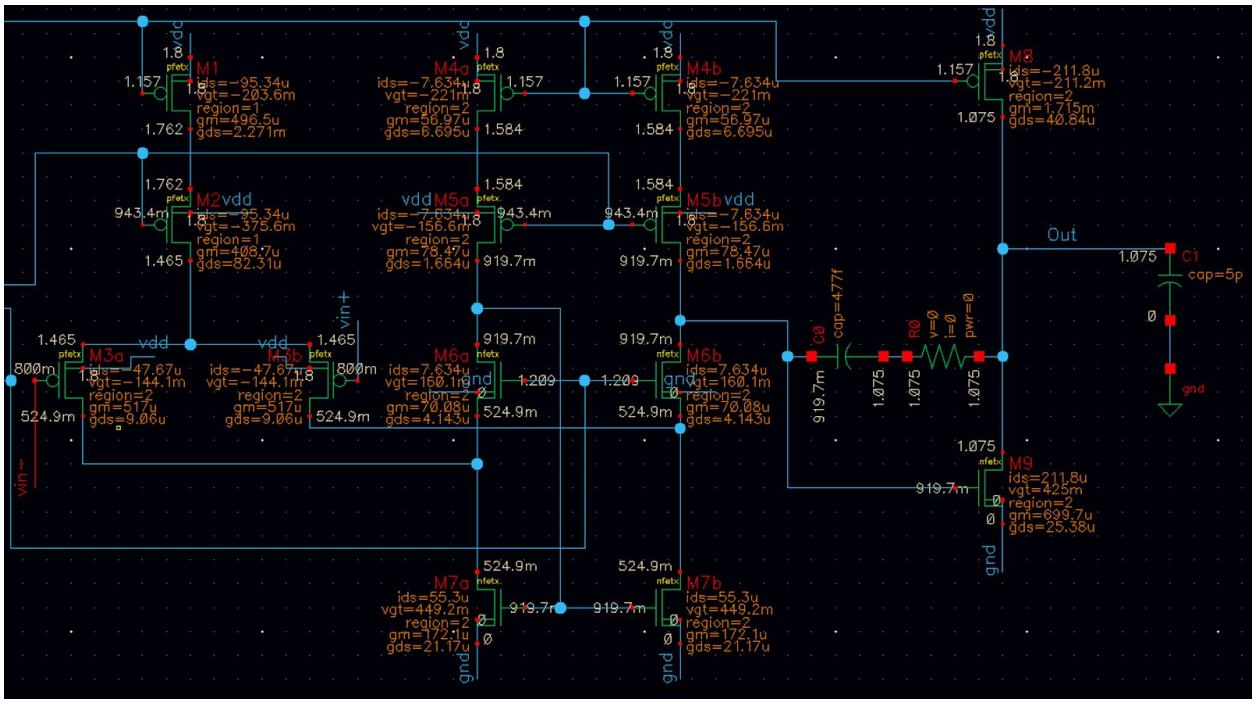
Size of two stages amplifier



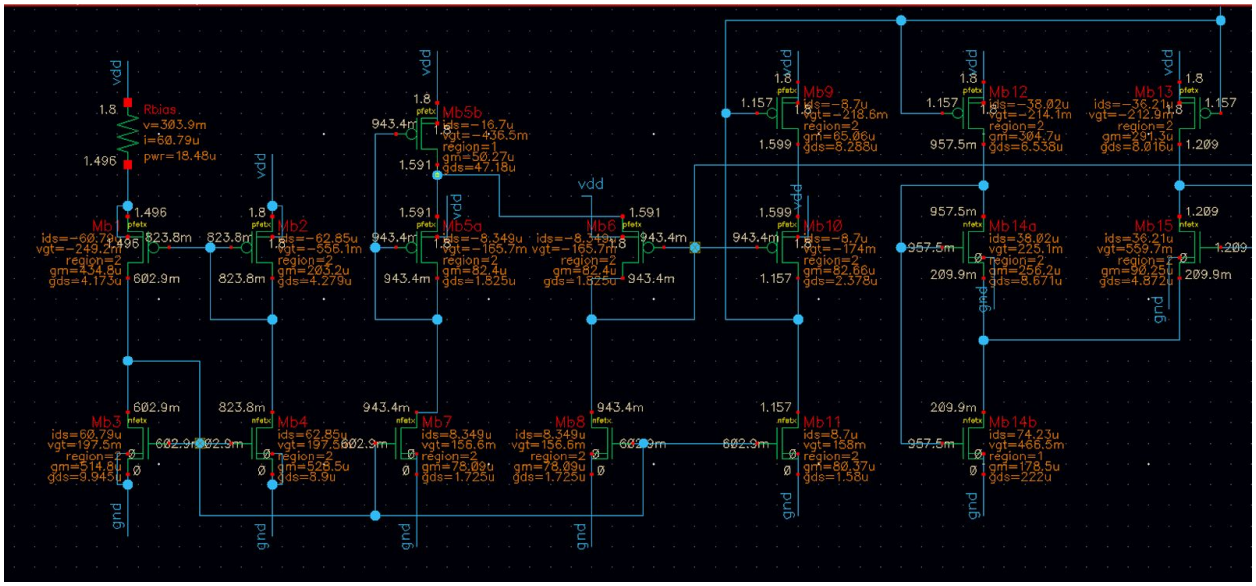
Size of bias circuit



Operation point of two stages amplifier



Operation point of bias circuit



Calculation part

Some technology parameters:

$K_n' = 260\mu$ $V_{tn} = 325m$ $\lambda = 0.1$

$K_p' = 50\mu$ $|V_{tp}| = 383m$

if we consider back gate effect, V_{tn} and V_{tp} will increase, so we assume:

$V_{tn} = 400m$, $V_{tp} = 450m$.

The gain of folded cascode:

$R_{out} = r_{o5b}(1+g_{m5b}r_{o4b}) \,//\, r_{o6b}(1+g_{m6b}(r_{o7b} // r_{o3b}))$ if $g_m r_o >> 1$

We have: $R_{out} = g_{m5b} r_{o5b} r_{o4b} // g_{m6b} r_{o6b} (r_{o7b} // r_{o3b}))$

$A_v = g_{m3} R_{out}$

The gain of CS:

$A_v = g_{m9}(r_{o8} // r_{o9})$

First, we analyzed the folded cascode and determine the bias voltages where we put the ideal voltage sources at.

For $M_{3a,b}$ in saturation, we first set $V_{g3} = V_{sr} = 0.8V$ and $V_{ov3} = 0.15V$ to make M1, M2 easier in saturation.

$V_{ov3} = V_{s3} - 0.8 - V_{tp}$

$V_{s3} = V_{ov3} + 1.25 = 1.4V = V_{D2}$

For M_2, set $V_{ov2} = 0.2V$, $V_{SD2} = 0.2V$.

$V_{S2} = 0.2 + V_{D2} = 1.6V = V_{D1}$

$V_{G2} = V_{S2} - V_{ov2} - V_{tp} = 1.6 - 0.2 - 0.45 = 0.95V$

For M_1: assume $V_{ov1} = 0.2V$, $V_{SD1} = 0.2V$.

$V_{S1} = 0.2 + V_{D1} = 1.8V$.

$V_{G1} = 1.8 - 0.2 - 0.45 = 1.15V$

I then chose these three voltages to bias the folded cascode and CS.

For M_5: $V_{g5} = 0.95V$. assume $V_{ov5} = 0.2V$.

set $V_{DS5} = 0.95V$ this is also the gate voltage of M_4 also the gate of M_7 $V_{ov7} = 0.95 - 0.4 = 0.55V$.

$\therefore V_{DS7} > V_{ov7}$, $V_{DS7} = V_{S6} \geq V_{ov} = 0.55V$

I choose $V_{S6} = 0.6V$.

For M6: $V_{ov6} = 0.2V$

$V_{g6} - V_{s6} - V_{tn} = 0.2$

$V_{g6} - V_S = 0.6V$.

$V_{g6} = 1.2V$

Frequency analysis.

For M_9: $V_{ov} = V_{gs} - V_t = 0.55 - 0.4 = 0.55\,V$

The total gain of this circuit is 70dB = 3162

To achieve the unity GBW ≥ 100MHz we have:

$$\omega_c = \omega_{p1} A_v$$

$$f_{p1} = \frac{\omega_c}{A_v} = \frac{2\pi \cdot 10^8}{3162} \simeq 2\times10^5\ Hz$$

we know f_{p2} is much larger than f_{p1} so lets assume it to be $10^8 Hz$

C_c: $GBW = \omega_c = \frac{gm_3}{C_c}$

$10^8 \cdot 2\pi = \frac{300\mu}{C_c}$

$C_c = 477fF$.

R_c: Using pole-zero cancellation:

$$R_c = \frac{C_c + C_L}{C_c \cdot gm_9} = 22964\,\Omega \approx 23k\,\Omega$$

We also have:

$$f_{p2} = \frac{gm_9}{C_L} \Rightarrow 10^8 = \frac{gm_9}{5\times10^{-12}} \Rightarrow gm_9 = 5\times10^{-4}S$$

$$I_8 = I_9 = \frac{gm_9 V_{ov9}}{2} = 1.375\times10^{-4}A = 137.5mA.$$

$$\left(\frac{W}{L}\right)_9 = \frac{137.5\times2}{260\times0.55^2} \approx 3.5.$$

assume $V_{ovp} = 0.2V$ $\left(\frac{W}{L}\right)_8 = \frac{137.5\times2}{50\times0.2^2} = 137.5$

For folded cascode.

$$A_v = gm_3 R_{eq}$$

$$R_{eq} = gm_{5b} r_{o5b} r_{o4b} \,//\, gm_{6b} r_{o6b} (r_{o7b} // r_{o3b})$$

$$= \frac{2I_5}{V_{ov5}} \cdot \frac{1}{\lambda I_5} \cdot \frac{1}{\lambda I_5} \,//\, \frac{2I_5}{V_{ov6}} \frac{1}{\lambda I_5} \left(\frac{1}{\lambda I_7} // \frac{1}{\lambda I_3}\right)$$

assuming $V_{ov5} = V_{ov6} = 0.2V$.

$$= \frac{2}{V_{ov5}\lambda^2(2I_5 + 2I_3)}$$

$$A_v = \frac{2I_3}{V_{ov3}} \cdot \frac{2}{V_{ov5}\lambda^2(2I_5+2I_3)}$$

where $V_{ov3} = 0.15V$, $V_{ov5} = 0.2V$, $\lambda = 0.4$ (nmos λ is larger than 0.1)

$I_3 \simeq 3I_5$

Assume $I_{4,5,6} = 10M$, $I_3 = 30M$, $I_7 = 10+30 = 40M$, $I_{1,2} = 80M$.

$gm_{4,5,6} = \frac{2I}{V_{ov}} = 100M$.

$gm_7 = \frac{2I}{V_{ov}} = 145M$.

$gm_3 = \frac{2I}{V_{ov}} = 300M$

$gm_{1,2} = \frac{2I}{V_{ov}} = 200M$.

$gm_8 = \frac{2I}{V_{ov}} = 1.375m$.

$gm_9 = \frac{2I}{V_{ov}} = 500M$.

$\left(\frac{W}{L}\right)_{4,5} = 10 = \frac{2.5M}{250n}$

$\left(\frac{W}{L}\right)_6 = 2 = \frac{500n}{250n}$

$\left(\frac{W}{L}\right)_7 = 1 = \frac{250n}{250n}$

$\left(\frac{W}{L}\right)_3 = 30 = \frac{7.5M}{250n}$

$\left(\frac{W}{L}\right)_{2,1} = 60 = \frac{15M}{250n}$.

the actual values are adjusted to meet the constraints such as $V_{ov2} \geq 150mV$, gain ≥ 70dB, etc.

Bias circuit:

We decided to the bias circuit from right to left.

Notice that the current through M_2 / M_{4} / M_1 are all mirrored from the current through M_{69} with different m factors. So I set the current through M_{b12}, M_{b13} to ba 40mA in order to keep the power Small.

The final $I_{9,8}$ I got from my CS stage is 144mA, So for $I = 40mA$ for M_{b12}, I should make $\frac{W}{L}$ Smaller assuming V_{ov} is the same with the value of 0.2V.

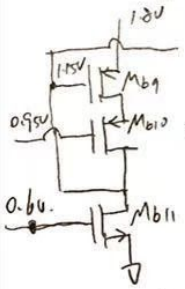
$\therefore$ $\frac{W}{L}$ M_{b3}, M_{b5} is $\frac{40}{144} \cdot (\frac{W}{L})_8 = \frac{5.56u}{250n}$ and for M_{b14a}, and M_{b5}, since they are nmos with larger k_n', I set their $(\frac{W}{L})$ to be $\frac{1u}{250n}$ for convenience reason.

I also keep $(\frac{W}{L})_{b4b}$ as $\frac{1u}{250n}$. notice it is in triode.

for $M_{b9, b10, b11}$ Initially I set the current the same as 40mA. So. I get $(\frac{W}{L})_{b9/10} = \frac{5.56u}{250n}$ and $(\frac{W}{L})_{b11} = \frac{1u}{250n}$. The key part here is to calculate a bias voltage between gate of M_{b8} and M_{b11}.

$(\frac{W}{L})_{b6,b5b} = \frac{5.56u}{250n}$ $(\frac{W}{L})_{b8,7} = \frac{1u}{250n}$.

$(\frac{W}{L})_{b5a,b6} = \frac{2.7u}{250n}$



For M_{b11}:

$V_g - 0 - 0.4 = 0.2$

$V_g = 0.6V$.

So I bias this gate with 0.6V for now., Here I triod to make the node between M_{b6}, M_{b10} to be 0.95V and the gate of M_{b15} = 1.2V. with only one bias source at gate of $M_{b13,12,9}$ = 1.15V.

Next step is to construct Constant gm. which achieve the node voltage between $M_{b3,4}$ = 0.6V.

Initially I assume current is 40mA. I chose $m = 4$

$I_d = \frac{V_{ovb_2}(1 - \frac{1}{\sqrt{4}})}{R_2}$ where $V_{ov_2} = 0.2$

$I_d = \frac{1}{2} k_n' \frac{W}{L} V_{ov}^2$

$\frac{W}{L} = \frac{100}{13}$.

$R_2 = 5k\Omega$.

I use $(\frac{W}{L})_{b_2} = \frac{4u}{520n}$ So that $(\frac{W}{L})_{b1} = \frac{16u}{520n}$. Then I did dc sweep at that node to select a $(\frac{W}{L})_{b3,4}$ to provide a 0.6V voltage at gate of $M_{b3,4}$. $(\frac{W}{L})_{b3,4} = \frac{8.6u}{1u}$

After everything was set, I put all parts together and discard the 1.15V ideal voltage source and tweak around the $(\frac{W}{L})$ of all transistors to achieve the requirement of all $V_{ov} \geq 150mV$ and achieve the gate of $M_{b9,12,13}$ to have 1.15V, gate of M_{b10} to have 0.95V, and gate of M_{b15} to have 1.2V.

Power dissipation:

$P = I \cdot V = (137.5 + 10\times2 + 60 + 40\times5 + 80)\times10^{-6}\times1.8 = 895\,\mu W. << 2.5mW$

Some key parameter comparison:

parameters:	Hand Calculations	SPICE values:
$I_{8,9}$	137.5μ	121.8μ
$I_{4,5,6}$	10μ	7.634μ
I_7	40μ	55.3μ
I_3	30μ	47.67μ
$I_{1,2}$	60μ	95.34μ.
g_{m9}	500μ	699.7μ
g_{m8}	1.375m	1.715m
g_{m7}	145μ	172μ
$g_{mA,5,6}$	100μ	56.9μ, 78.47μ, 70.08μ
g_{m3}	300μ	517μ
$g_{m1,2}$	200μ	496μ, 408μ
C_c	477fF	477fF
R_c	23kΩ	26kΩ
Power Dissipation	895μW.	982.2μW

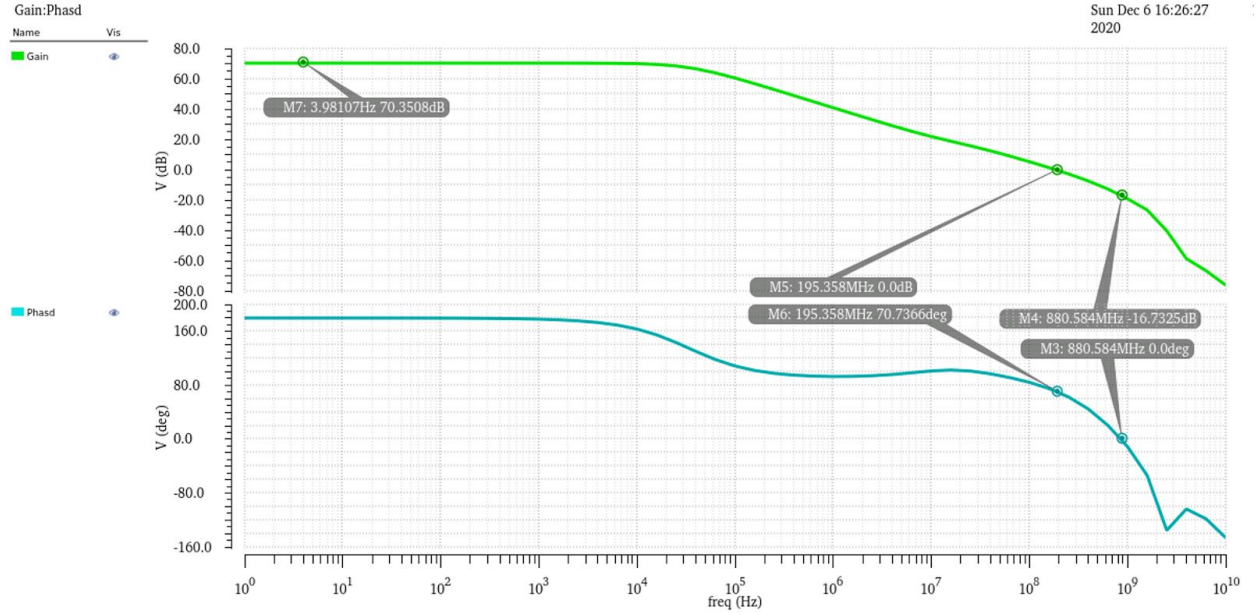
Reasons of Discrepancies:

For currents, the discrepancies were actually quite small. The reason that these discrepancies exist might be in reality, Id are actually experiencing CLM while when I first estimated the values, I did not take that into account for convenience. And gm values are little off because first Is are different and second, vov are not the ones we assumed.

Rc, Cc are adjusted to meet phase margin / gain margin requirements but overall are constant. Power is little bit more because the actual currents amount is larger because of CLM.

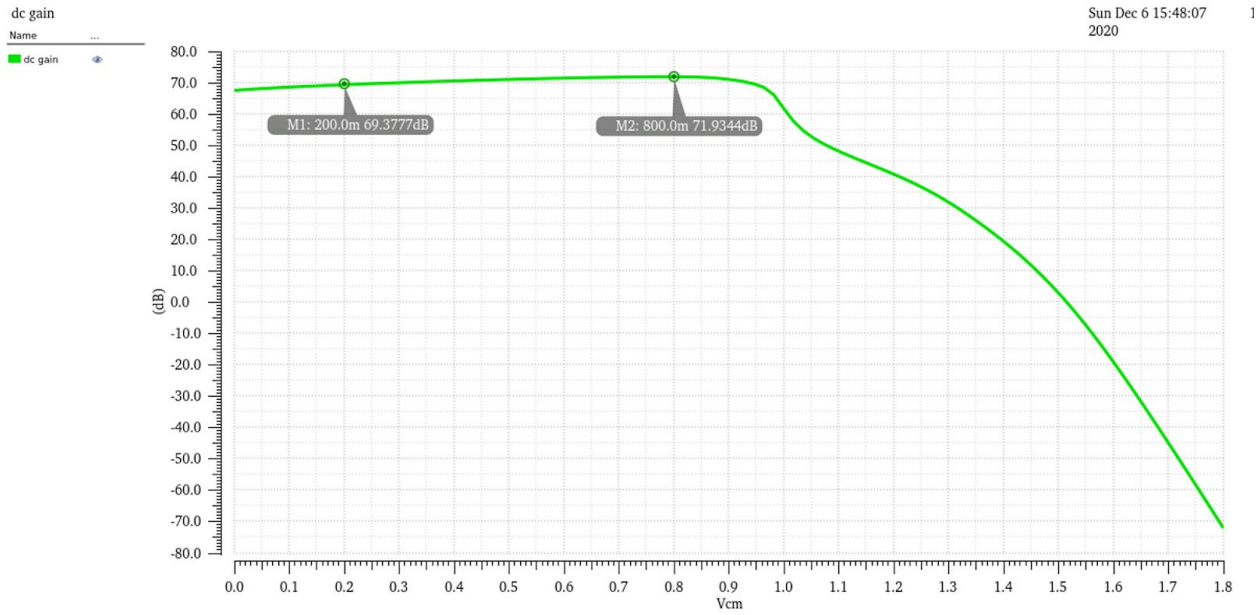
Bode plot simulation results

Gain and Phase Margin

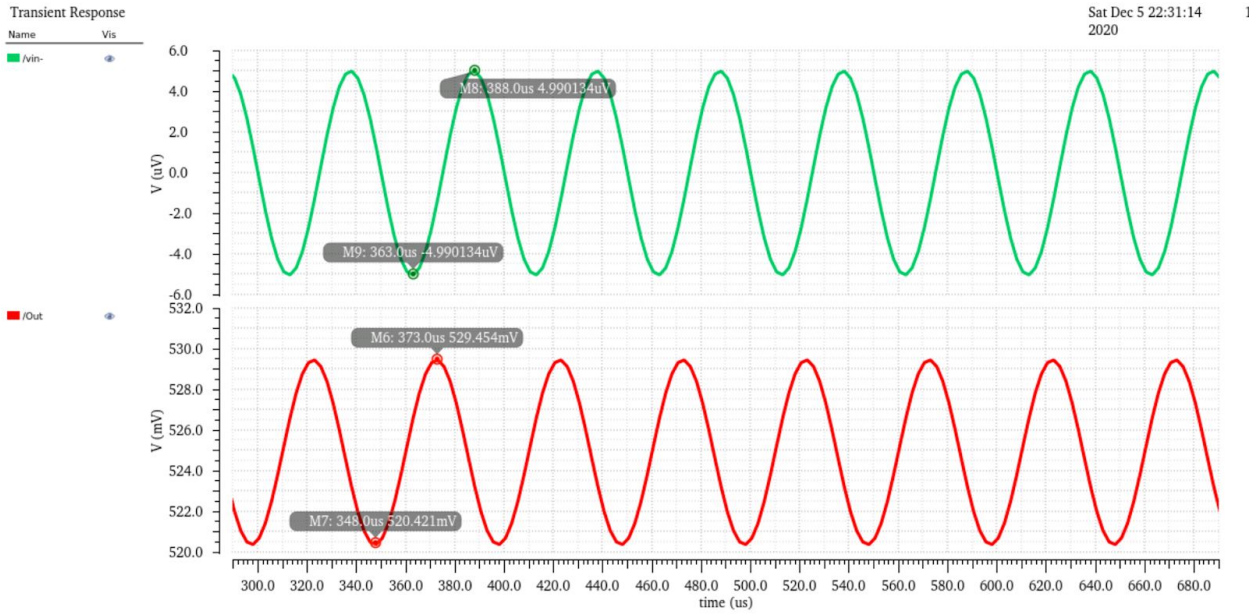


Phase Margin by calculation: 73.4 degree(approximately the same)

DC gain



Transient simulation results for a 10 µVpp sinusoid at 20 kHz.



Result of Test Bench showing Unity Gain Bandwidth and Power.

Outputs

	Name/Signal/Expr	Value	Plot	Save
2	Gain Margin	-16.51	☑	☐
3	Phase Margin	71.45	☑	☐
4	Unit gain BW	200.7M	☑	☐
5	Phasd	wave	☑	☐
6	dc gain	70.35	☑	☐
7	power	982.2u	☑	☑

Conclusion:

This is definitely a challenging project for us but also a valuable experience especially for those who later would go into the industry.

We have learned tons of useful information and steps that are required for solving such a practical problem. First of all, we have learned that before starting to solve a problem, we should first divide the problem into small blocks and decide which parts should be our priority and most critical. On the top of that, we have learned how to integrate the knowledge we learned from the lectures and homework into solving this project. We now know how to make proper and educated estimations to give us a starting point to solve an intricate circuit. The most challenging part came when we tried to determine the current ratio between I3 and I5. We kept getting the wrong results until we found out that lambda actually made a huge impact on the results. From this experience, we learned that any small seemingly trivial values can make a huge difference. We basically need to take anything into consideration. We also gain a deeper understanding on poles and zeros and how they impact the design.