



UEFI & EDK II TRAINING

EDK II Open Board Platform Design for Intel
Architecture (IA)

tianocore.org

LESSON OBJECTIVE

- ★ Introduce Minimum Platform Architecture (MPA)
- ★ Explain the EDK II Open board platforms infrastructure & focus areas
- ★ Describe Intel® FSP with the EDK II open board platforms

Reference: [Minimum Platform Architecture Specification](#)

DESIRED USE CASES

– Open Source EDK II Platforms

Developers need a way to turn on and off of a feature.

Developers need a way to get platform configuration data.

Developers need to do porting work from an existing board to a new board.

Developers might need to work on a different board.

INTRODUCING

Minimum Platform Architecture

Minimum Platform Architecture (MPA)

Structured

Enable developers to consistently navigate code, boot flow, and the functional results

Approachable

Enable developers to quickly produce a baseline that is extensible with minimal UEFI or EDK II knowledge

Portable

Minimize coupling between common, silicon, platform, board, and feature packages

Reusable

Enable large granularity binary reuse (FV binaries)

Testable

Enable validating the correctness of a port

Design open source EDK II Intel Architecture firmware

Code Convergence & Consistency



System firmware (BIOS) is the largest payload in the IFWI binary image

Platform implementation is ~2-3 million lines+ of “C” code

Technology complexity increasing, strains firmware implementation solutions

Limited firmware engineering resources

Copy + Paste + Modify = Human Errors

Why Move to Open Source?

Goal:

- Enable improvements in quality and security for Intel products
- Enable vertically integrated open solutions

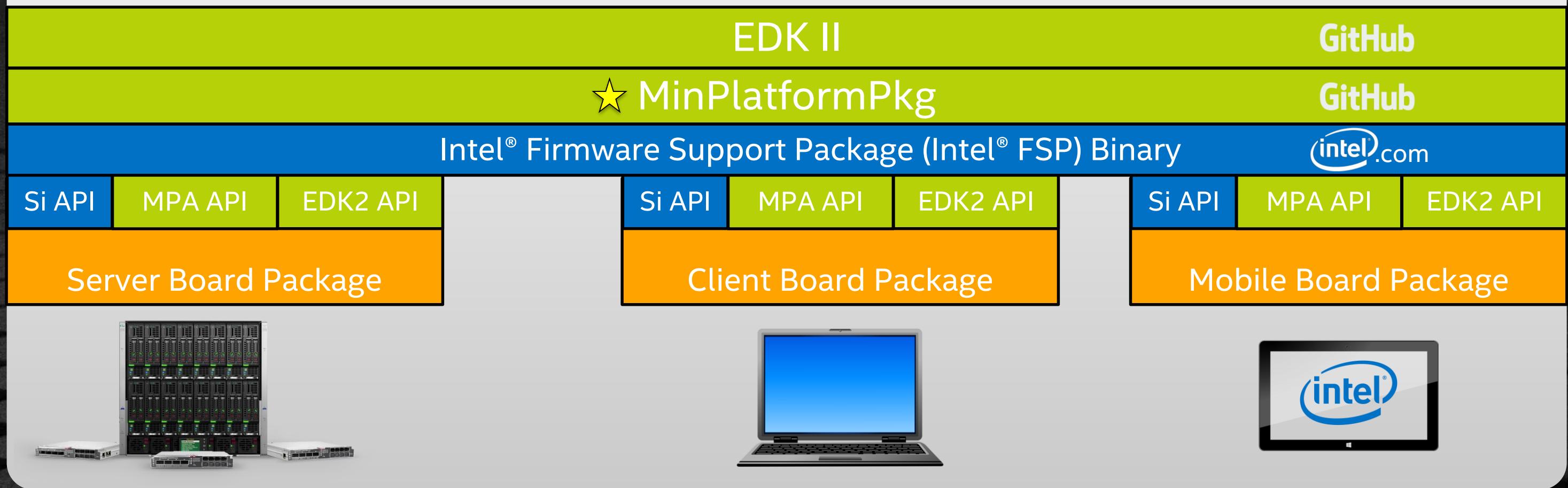
Benefits:

- Allow improved customer engagements
- Builds transparency and trust
- Reduce overhead to transition from internal to external
- Deploy fixes across the ecosystem more rapidly

Easier to access, understand, fix & optimize means improved product quality

MinPlatform + Intel® Firmware Support Package (Intel® FSP)

Open source Closed source Implementation Choice



Intel Open Platform Firmware Stack - Minimum Platform

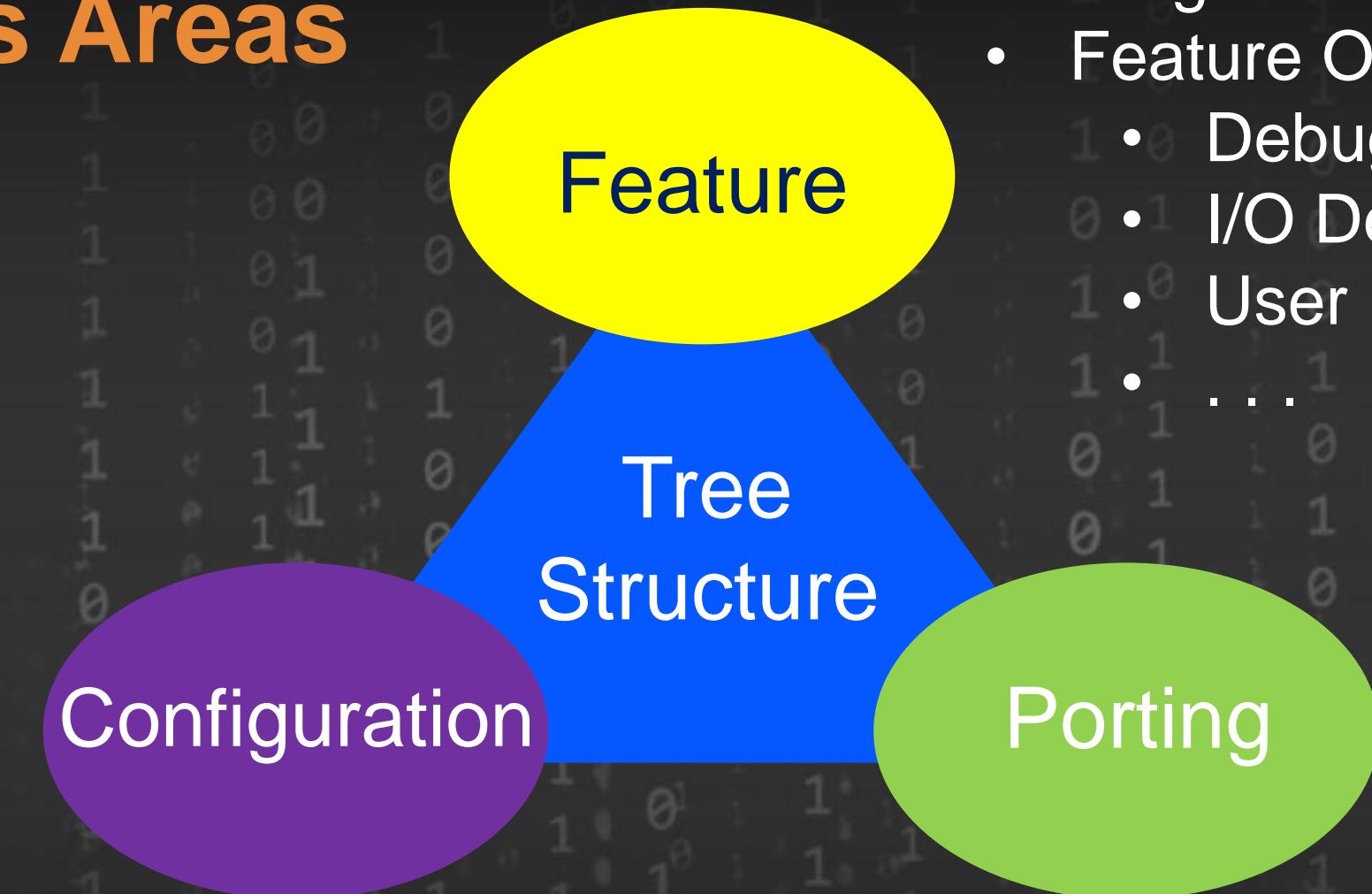
Consistent boot flows and interfaces
Approachable across the ecosystem
Scalable from pre-silicon to derivatives

What are Minimum Platform Stages?



Stages reflect firmware development lifecycle
and how a system bootstraps itself

Four Focus Areas

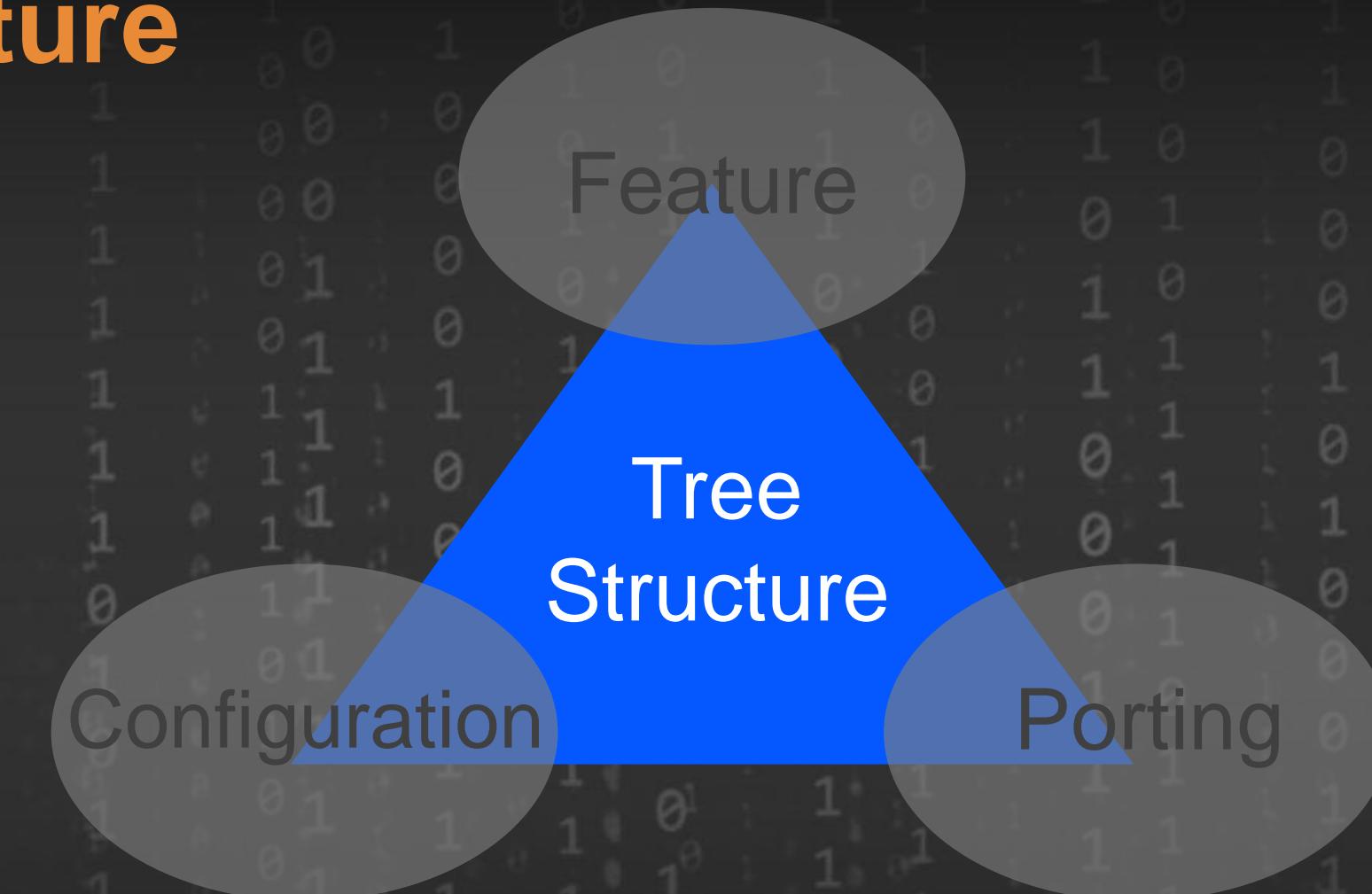


- Staged
- Defined PCD
- Policy Hob/PPI/Protocol

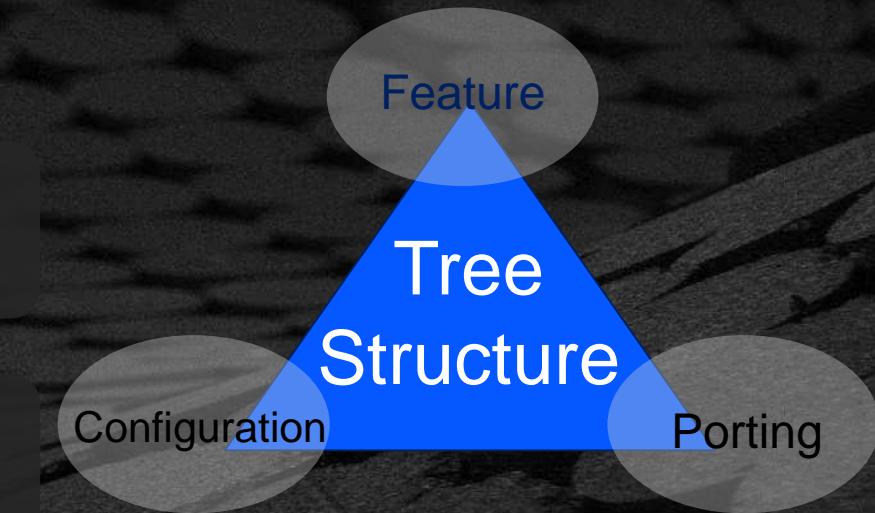
- Staged Minimal Baseline
- Feature ON/OFF
 - Debug
 - I/O Devices
 - User Interface
 - ...

- Staged
- GPIO
- SIO
- ACPI

Tree Structure



Organization



Common

- No direct HW requirements

Platform

- Enable a specific platform's capabilities.

Board

- Board specific code

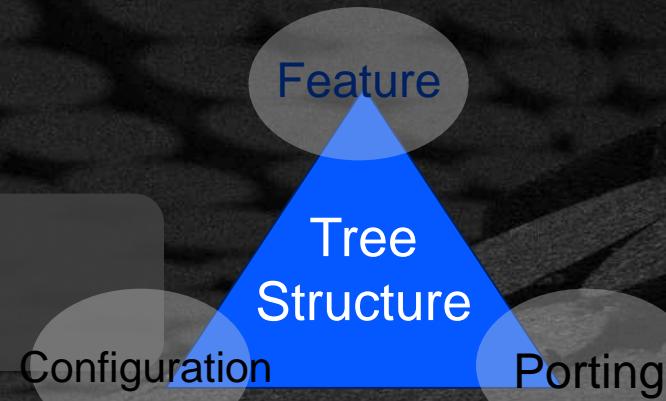
Silicon

- Hardware specific code

Features

- Advanced features of platform functionality that is non-essential for "basic OS boot"

Package Organization Example



MinPlatformPkg

- Common - Boot flow, well defined interfaces

BoardModulePkg

- Board - Generic board functionality (e.g. CMOS access code) – staging to EDK II

XxxOpenBoardPkg

- Platform Xxx* - board-specific details: GPIOs, memory config, audio verb tables, etc.

XxxSiliconPkg

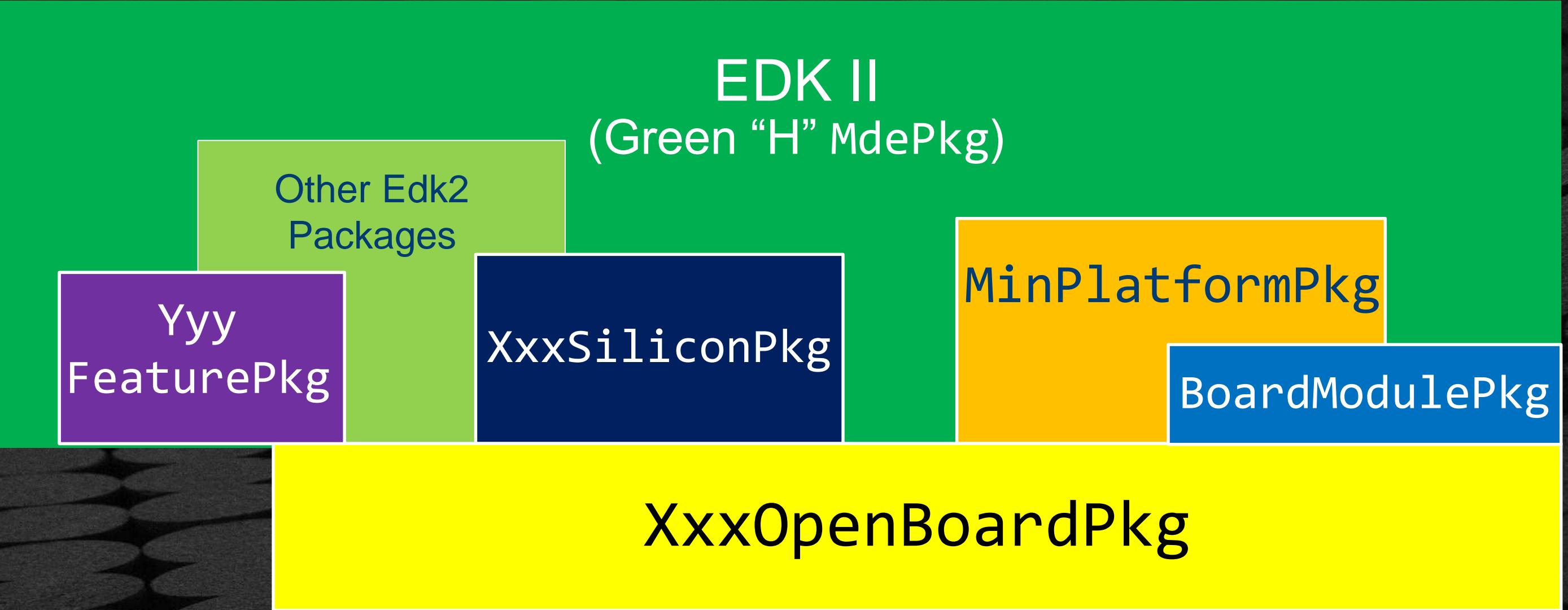
- Silicon - Hardware specific code for Xxx

YyyFeaturePkg

- Features – Advanced functional features

*Where Xxx would be an open platform: KabyLakeOpenBoardPkg, WhiskeyLakeOpenBoardPkg, etc.

MPA Dependency Rules

**Key**

Bottom shapes can only depend on shapes above them

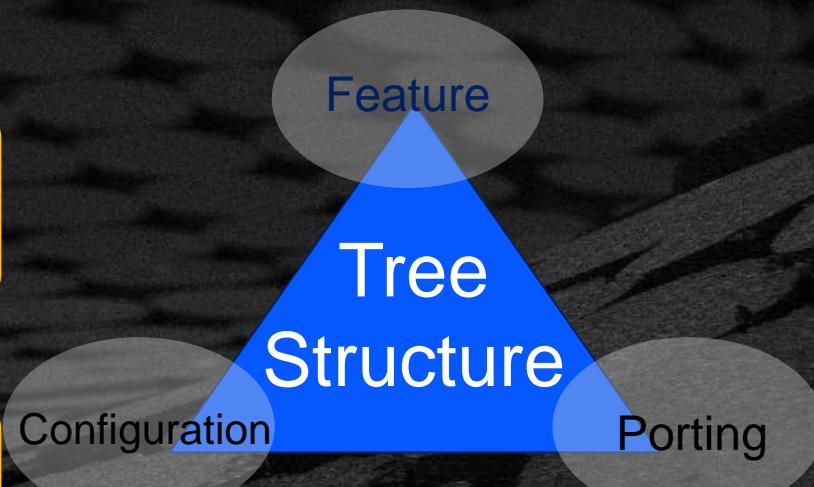
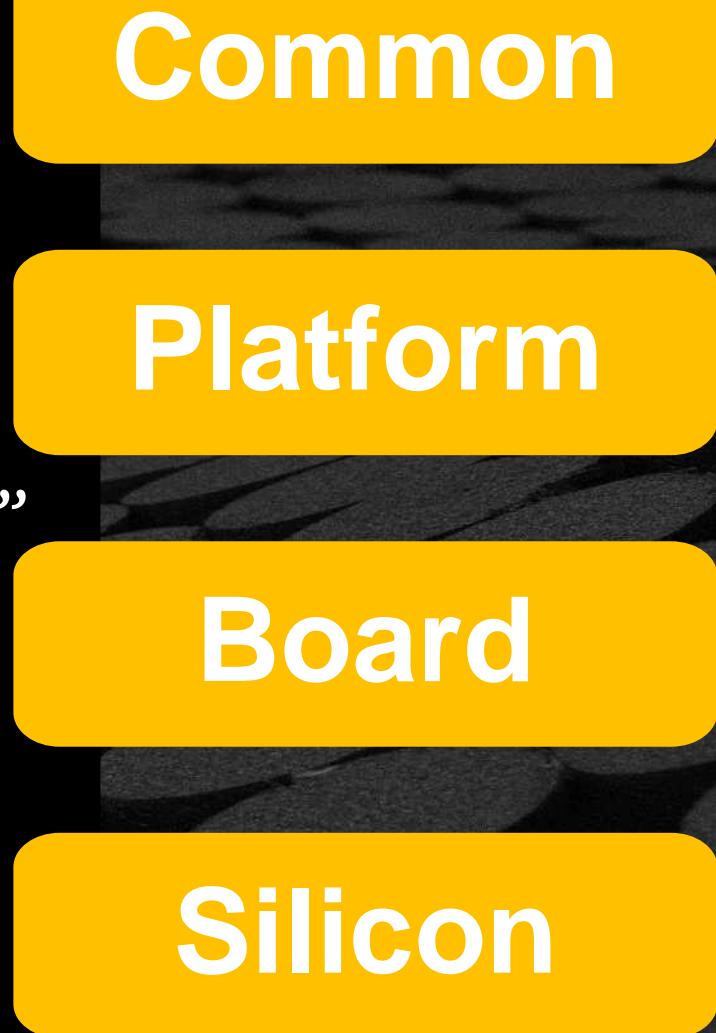
YyyFeaturePkg – represents multiple feature package instances that are mutually exclusive to each other

BoardAbc

BoardAbc – directory for `OpenBoardPkg.dsc`

Open Source EDK II Workspace

MyWorkSpace/
edk2/
 - “*edk2 Common*”
edk2-platforms/
 Platform/ “*Platform*”
 Intel/
 MinPlatformPkg/“*Platform*”
 BoardModulePkg/“*Sharable*”
 XxxOpenBoardPkg/ “*Platform*”
 BoardX/ “*Board*”
 Silicon/ “*Silicon*”
 Intel/
 XxxSiliconPkg/
edk2-non-osi/
 Silicon/
 Intel/
FSP/“*Silicon*”
 . . . /



Open Board Tree Structure

edk2/ <https://github.com/tianocore/edk2> ← **Common**

· · ·

edk2-platform/ <https://github.com/tianocore/edk2-platforms>

Platform/

Intel/

BoardModulePkg

KabylakeOpenBoardPkg

KabylakeRvp3

MinPlatformPkg

UserInterfaceFeaturePkg

← **Common (shareable)**

← **Platform (family)**

← **Board (instance)**

← **Platform**

← **Advanced Feature**

Silicon/

Intel/

KabylakeSiliconPkg

← **Silicon**

· · ·

edk2-non-osi/ <https://github.com/tianocore/edk2-non-osi>

Silicon/

Intel/

KabylakeSiliconBinPkg

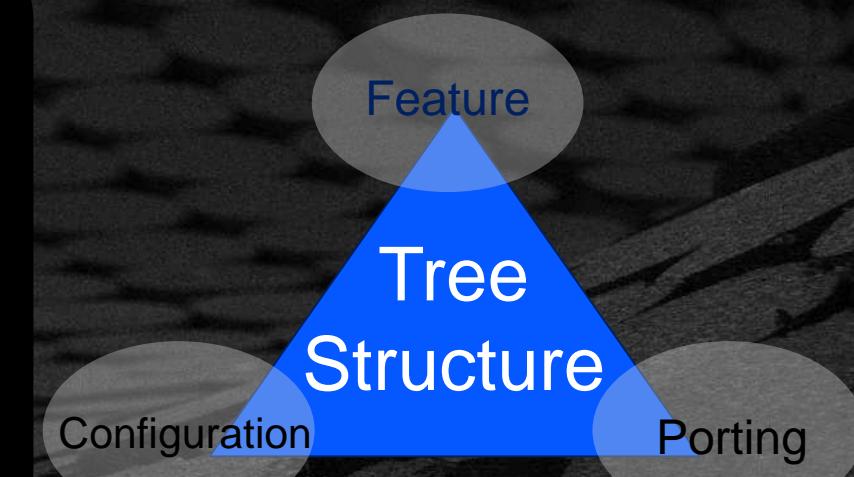
← **Silicon**

PurleySiliconBinPkg

FSP/ <https://github.com/IntelFsp/FSP>

KabylakeFspBinPkg

← **Silicon**



Directory Description

edk2-platform: EDK II repo includes open source platform code

- Platform folder: contains the platform specific modules by architecture
 - `BoardModulePkg`: generic board functionality (board Lib interfaces)
 - `MinPlatformPkg`: generic platform instance to control the boot flow.
 - `XxxFeaturePkg`: package to hold Xxx advanced platform feature .
 - `<Generation>OpenBoardPkg`: the silicon generation specific board package. All of the boards based upon this silicon generation can be located here.
- Silicon folder: contains the silicon specific modules.
 - `<Generation>SiliconPkg`: the silicon generation specific silicon package.

edk2-non-osi: EDK II repo for platform modules in binary format (ex: silicon init binaries).

- `<Generation>SiliconBinPkg`: It is the silicon generation specific binary package. For example, CPU Microcode or the silicon binary FVs.

Ideally, Only `<Generation>OpenBoardPkg` needs updating

FSP Directory Description

FSP: repo for Intel® Firmware Support Package (FSP) binaries

Platform folder Pkg: Each FSP project will be hosted in a separate directory

- ApolloLakeFspBinPkg Intel® Atom™ processor E3900 product family
- ...
- CoffeeLakeFspBinPkg - 8th Generation Intel® Core™ processors and chipsets (formerly Coffee Lake and Whiskey Lake)
- **KabylakeFspBinPkg** 7th Generation Intel® Core™ processors and chipsets
 - Include
 - FSP UPD structure and related definitions used with EDK II build
 - Doc - Integration Guide .PDF documentation
 - **FSP.fd** - Binary to be included with flash device image
 - **FSP.bsf** - Configuration File with IDE configuration tool

FSP each project based on Intel Architecture

Board Package Structure

MinPlatformPkg

```
MinPlatformPkg /  
  <Basic Common Driver>/  
  Include /  
  Library /  
  PlatformInit /
```

Platform Common Driver

Where:

- **<Basic Common Driver>**: The basic features to support OS boot, such as ACPI, flash, and FspWrapper. It also includes the basic security features such as Hardware Security Test Interface (HSTI).
- **Include**: The include file as the package interface. All interfaces defined in MinPlatformPkg.dec are put to here.
- **Library**: It only contains feature independent library, such as PeiLib. If a library is related to a feature, this library is put to <Feature>/Library folder, instead of root Library folder.
- **PlatformInit**: The common platform initialization module. There is PreMemPEI, PostMemPEI, DXE and SMM version. These modules control boot flow and provide some hook point to let board code do initialization.

Board Module Package Structure

```
BoardModulePkg /  
  Include /  
  Library /  
    BiosIdLib /  
    CmosAccessib /  
    PlatformCmosAccessLibNull /
```

Board Generic Functionality

Where:

- **Include**: The include file as the package interface. All interfaces defined in BoardModulePkg.dec are put to here.
- **Library**: It only contains board generic features as independent library, such as BiosIdLib and Cmos Access Lib

Open Board Package Structure

```
<Generation>OpenBoardPkg /  
  <BasicCommonBoardDrivers>/  
    Include /  
    Library /  
    Features /  
      <AdvancedCommonBoardDrivers> /  
    <BoardX> /  
      Include/  
      Library/  
      <BoardSpecificDriver> /  
      OpenBoardPkg.dsc  
      OpenBoardPkg.fdf
```

Where:

- **<BasicCommonBoardDrivers>** and **<AdvancedCommonBoardDrivers>** designate a board generation specific feature. They need to be updated when we enable a board generation.
- **<Board>** contains all the board specific settings. If we need to port a new board in this generation, copy the **<Board>** folder and update the copy's settings

Advanced Feature Package

```
XxxFeaturePkg /  
  Include /  
  Library /  
  Readme.md
```

The advanced features, domains such as SMBIOS table, IPMI, User Interface, Power Management

Where:

Include: The **include** file as the package interface.

Library: Implementation of feature as a library.

Readme.md : Describes the purpose and scope of the feature package with a list of dependencies

One Feature, One directory Guideline

Use a hierarchical layout , KabylakeOpenBoardPkg example

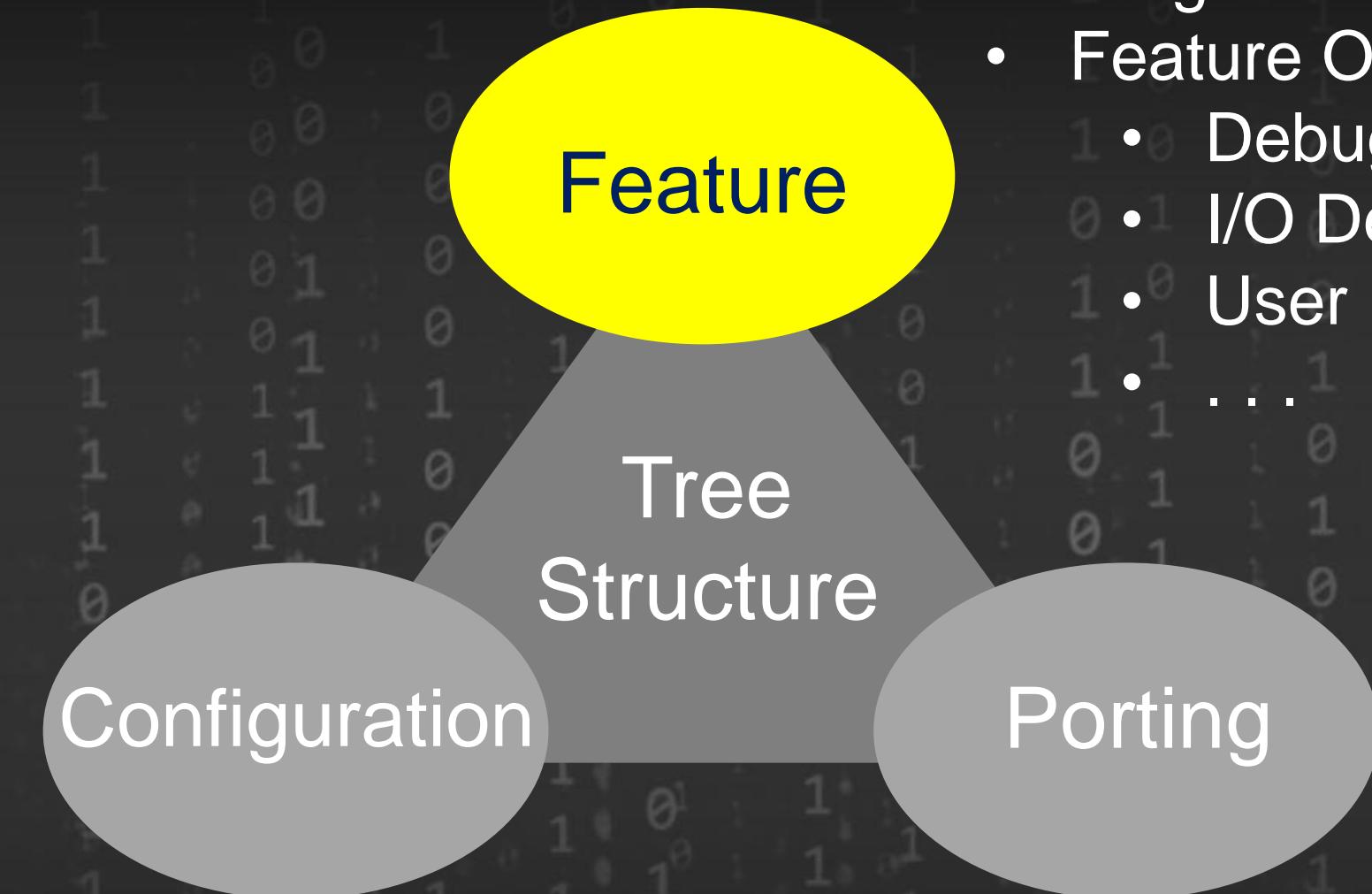
```
KabylakeOpenBoardPkg /  
  Acpi /  
    BoardAcpiDxe /  
  FspWrapper /  
    Library /  
    PeiFspPolicyUpdateLib /  
  Include /  
  KabylakeRvp3  
  Library /  
    BaseEcLib /  
    BaseGpioExpanderLib /  
    PeiI2cAccessLib /  
  Policy /  
    ...
```

```
KabylakeRvp3 / (cont.)  
  Include /  
  Library /  
  OpenBoardPkg.dsc  
  OpenBoardPkg.fdf
```



Only put the basic features into the root directory

Features



- Staged Minimal Baseline
- Feature ON/OFF
 - Debug
 - I/O Devices
 - User Interface
 - ...

Feature Selection

There are three phases of feature selection

Minimum

Manage Stage I-V
options

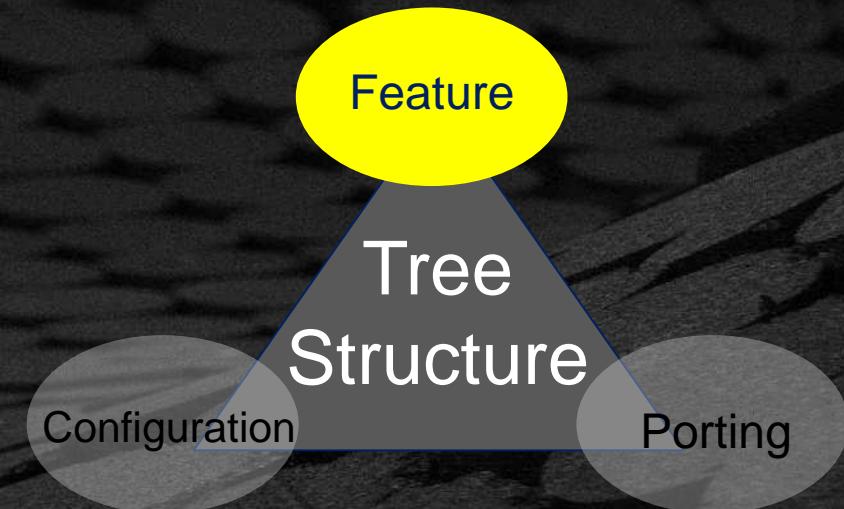
Advanced Feature
Selection

Add rich feature sets
(Stage VI)

Optimization

Remove undesired
features (Stage VII)

Select features through build, prune in binary

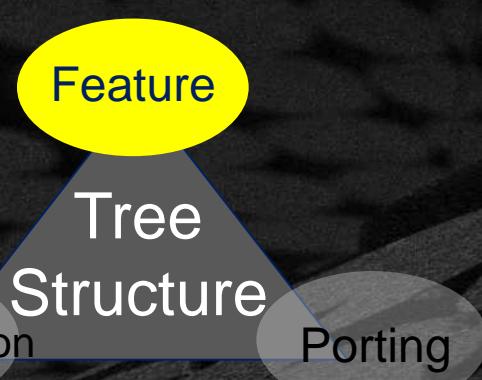


Minimum Platform Feature Selection

Minimum Platform

- Minimum feature selection should be exclusively implemented as Platform Configuration Database (PCD)
- Required PCD are identified in the MPA specification
- PCDs:
 - Declared with defaults in DEC files in different packages
 - Modified in DSC file for the board, if different than the default value

Silicon – FSP Integration from <Generation>FspBinPkg documentation package



All initial porting features selection should be done this way

Advanced Feature Selection

Advanced features implement DSC and FDF files that you can include in your board DSC and FDF files in the correct spots

OpenBoardPkg.dsc File

• • •

<End-of-File>

```
!include YyyAdvancedPkg.dsc
```

OpenBoardPkg.fdf File

FV Advanced Pre-Mem

```
!include YyyAdvancedPkgPreMem.fdf
```

FV Advanced Post-Mem

```
!include YyyAdvancedPkgPostMem.fdf
```

FV Advanced Late

```
!include YyyAdvancedPkgLate.fdf
```

FV Advanced ← (Pre-mem + Post-mem +
Late)

Optimization Feature Selection

Minimum Platform takes advantage of UEFI and EDK II features to enable feature selection to be done by post-processing the built binaries

Essentially, after your system is functioning well, you can remove features using the FMMT tool to remove the drivers that are included as you build up the desired functionality

For example, if you need UEFI Shell during power-on, testing, etc. But you don't want it for final product. Minimum Platform architecture makes it easy to locate and remove the shell by post-processing the image

Link for [FMMT Tool](#)

NV Storage

NV Storage Variable

NV Storage FTW working

NV Storage FTW Spare

FV 6

FV 5

FV 4

FV 3

UEFI Shell

FV 2

FV Microcode

FV FSP

FV 1

Flash Layout

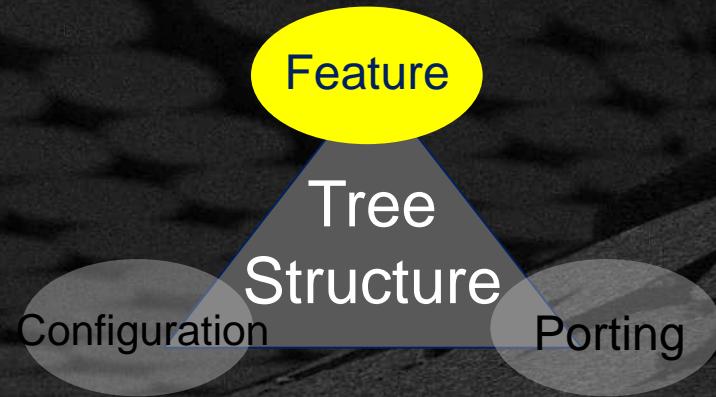
Stage 7:
Remove
with FMMT
Tool



Full Customization Feature Selection

Feature modifications only at the Board / Platform DSC

Preferred modifications at Board (e.g. BoardAbc)



XxxOpenBoardPkg

BoardAbc

BoardAbc – directory for [OpenBoardPkg.dsc](#)

Features Build Enabled

Platform-Board Build Scripts

Many platforms have a script (Python or bash) to pre & post process the EDK II build process: [Build Script](#)

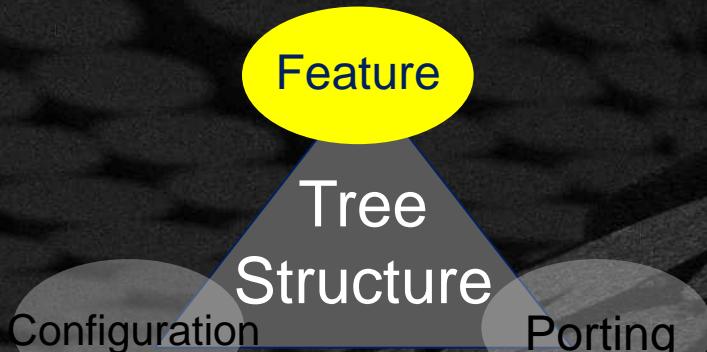
Example: Invoked from the edk2-platforms/Platform/Intel

`python build_bios.py -p <Board-name>`

uses config file `build.cfg` from the `<Board-name>` directory

Configuration Files:

- `edk2-platforms/Platform/Intel/build.cfg` - default settings
- Default settings are under the `DEFAULT_CONFIG` section
- Override the `edk2-platforms/Platform/Intel/. . ./build.cfg` settings from each board in board specific directory

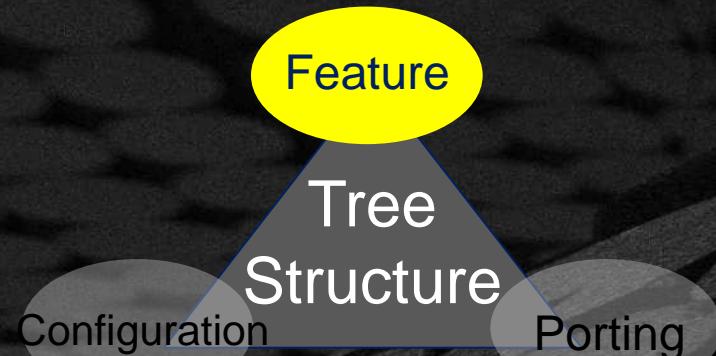


Example Build Config File

Kabylake example of Board specific settings:

<workspace>/edk2-platforms/Platform/Intel/KabylakeOpenBoardPkg/\\
KabylakeRvp3/ build_config.cfg

```
[CONFIG]
WORKSPACE_PLATFORM_BIN = WORKSPACE_PLATFORM_BIN
EDK_SETUP_OPTION =
openssl_path =
PLATFORM_BOARD_PACKAGE = KabylakeOpenBoardPkg
PROJECT = KabylakeOpenBoardPkg/KabylakeRvp3
BOARD = KabylakeRvp3
FLASH_MAP_FDF = KabylakeOpenBoardPkg/Include/Fdf/FlashMapInclude.fdf
PROJECT_DSC = KabylakeOpenBoardPkg/KabylakeRvp3/OpenBoardPkg.dsc
BOARD_PKG_PCD_DSC =
KabylakeOpenBoardPkg/KabylakeRvp3/OpenBoardPkgPcd.dsc
ADDITIONAL_SCRIPTS =
KabylakeOpenBoardPkg/KabylakeRvp3/build_board.py
PrepRELEASE = DEBUG
SILENT_MODE = FALSE
...
```



Platform name & path
to build.cfg file
under [PLATFORMS]

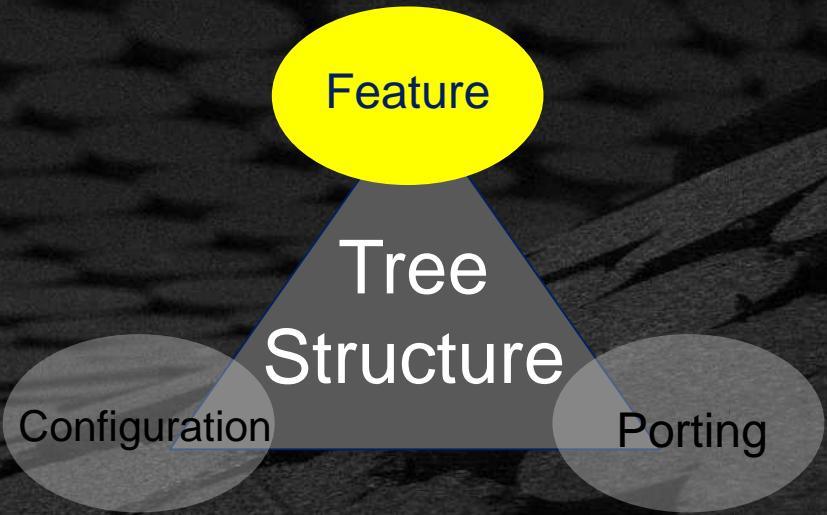
Minimum Platform Stage Selection

Platform Firmware Boot Stage PCD:

OpenBoardPkgConfig.dsc

[PcdsFixedAtBuild]

```
#  
# Please select BootStage here.  
# Stage 1 - enable debug (system deadlock after debug init)  
# Stage 2 - mem init (system deadlock after mem init)  
# Stage 3 - boot to UEFI shell only  
# Stage 4 - boot to OS  
# Stage 5 - boot to OS with security boot enabled  
# Stage 6 - Add Advanced features  
gMinPlatformPkgTokenSpaceGuid.PcdBootStage|4
```



Minimum Platform Stage Selection

Stage selection allows developers to bring up a system in a familiar matter:

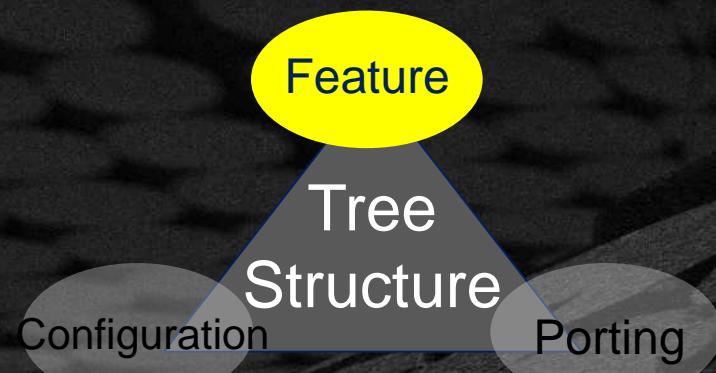
- Set to Stage I. Boot, verify serial debug capability, ready for silicon debug
- Set to Stage II. Boot, verify memory and silicon functionality
- Set to Stage III. Boot, verify board porting from shell: devices, GPIO, etc
- Set to Stage IV. Boot, verify ACPI porting, MADT, DSDT methods, etc.

Developers can exercise functionality gradually.

Verification at each stage

Required set of PCDs in MPA Spec

Link to Required PCDs according to stages



[Flash Map Config](#)

[Debug Config](#)

[Intel® FSP Config](#)

[Post Memory FV](#)

[UEFI FV](#)

[Driver Related](#)

[Memory Type Information](#)

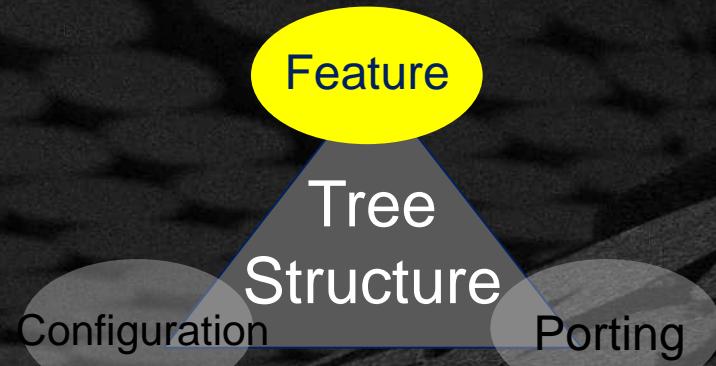
[OS FV](#)

[Security Flash Map](#)

[Stage 5 Features](#)

[Advanced Feature FV](#)

Build Control Files



DSC files

control what gets
compiled and linked

FDF files

control what gets
put in the system
FLASH image

Where are the DSC & FDF files?

Kabylake Open Board

Platform/Intel/KabyLakeOpenBoardPkg/

KabyLakeRvp3/
OpenBoardPkgConfig.dsc

OpenBoardPkgPcd.dsc ← **Modify PCD Here**

OpenBoardPkgBuildOption.dsc

OpenBoardPkg.dsc ← **Add Features Here**

FlashMapInclude.fdf

OpenBoardPkg.fdf ← **Add Features Here**

/edk2-platforms/Platform/

Intel/**MinPlatformPkg/**

Include/

Fdf/

Dsc/

/edk2-platforms/Platform/

Intel/**YyyAdvancedPkg/**

Include/

Fdf/

Dsc/

OpenBoardPkgPcd.dsc File Controls if feature ON or OFF

Example Kabylake Configuration .DSC file

```
[PcdsFixedAtBuild]
#
# Please select BootStage here.
# Stage 1 - enable debug (system deadlock after debug init)
# Stage 2 - mem init (system deadlock after mem init)
# Stage 3 - boot to shell only
# Stage 4 - boot to OS
# Stage 5 - boot to OS with security boot enabled
#
gMinPlatformPkgTokenSpaceGuid.PcdBootStage|4

[PcdsFeatureFlag]
gMinPlatformPkgTokenSpaceGuid.PcdStopAfterDebugInit|FALSE
gMinPlatformPkgTokenSpaceGuid.PcdStopAfterMemInit|FALSE
gMinPlatformPkgTokenSpaceGuid.PcdBootToShellOnly|FALSE
gMinPlatformPkgTokenSpaceGuid.PcdUefiSecureBootEnable|FALSE
gMinPlatformPkgTokenSpaceGuid.PcdTpm2Enable|FALSE

!if gMinPlatformPkgTokenSpaceGuid.PcdBootStage >= 1
    gMinPlatformPkgTokenSpaceGuid.PcdStopAfterDebugInit|TRUE
!endif
```

[Link to Config .dsc file](#)

[Link to EDK II DSC Spec.](#)

Example Kabylake .FDF file

[FV.FvPreMemory]

```
INF UefiCpuPkg/SecCore/SecCore.inf
INF MdeModulePkg/Core/Pei/PeiMain.inf
!include $(PLATFORM_PACKAGE)/Include/Fdf/CorePreMemoryInclude.fdf
INF $(PLATFORM_PACKAGE)/PlatformInit/PlatformInitPei/PlatformInitPreMem.inf
INF IntelFsp2WrapperPkg/FspmWrapperPeim/FspmWrapperPeim.inf
INF $(PLATFORM_PACKAGE)/PlatformInit/SiliconPolicyPei/SiliconPolicyPeiPreMem.inf
```

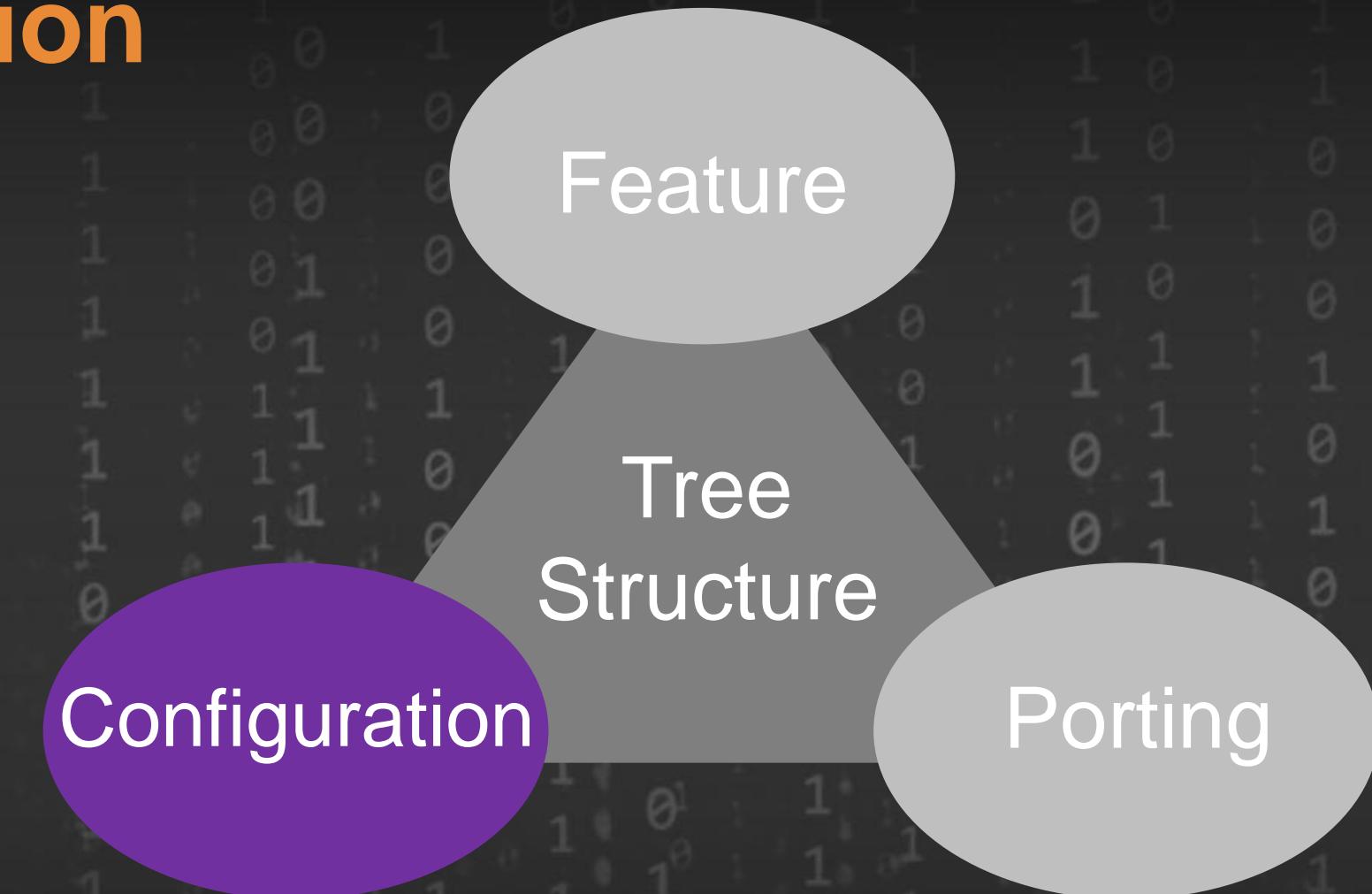
[FV.FvPostMemoryUncompact]

```
!include $(PLATFORM_PACKAGE)/Include/Fdf/CorePostMemoryInclude.fdf
# Init Board Config PCD
INF $(PLATFORM_PACKAGE)/PlatformInit/PlatformInitPei/PlatformInitPostMem.inf
INF IntelFsp2WrapperPkg/FspsWrapperPeim/FspsWrapperPeim.inf
INF $(PLATFORM_PACKAGE)/PlatformInit/SiliconPolicyPei/SiliconPolicyPeiPostMem.inf
!if gSiPkgTokenSpaceGuid.PcdPeiDisplayEnable == TRUE
FILE FREEFORM = 4ad46122-ffeb-4a52-bfb0-518cfca02db0 {
SECTION RAW = $(PLATFORM_FSP_BIN_PACKAGE)/SampleCode/Vbt/Vbt.bin
SECTION UI = "Vbt"
}
FILE FREEFORM = 7BB28B99-61BB-11D5-9A5D-0090273FC14D {
SECTION RAW = MdeModulePkg/Logo/Logo.bmp
}
```

[Link to Kabylake .FDF](#)

[Link to EDK II FDF Spec](#)

Configuration



- Staged
- Defined PCD
- Policy Hob/PPI/Protocol

Configuration Options

There might be many sources of platform configuration data.

PI PCD

Configuration
Block

CMOS

UEFI Variable

Global NVS

MACRO

FSP UPD-
Silicon Policy
Hob/PPI/ Protocol

Platform signed
data blob

MPA Configuration Options

Platform configuration data for Minimum Platform

PI PCD

- The PI PCD could be static data fixed at build time or dynamic data updatable at runtime.

FSP UPD- Silicon
Policy Hob/PPI/
Protocol

- FSP UPD can be static default configuration, or a dynamic updatable UPD. It is policy data constructed at runtime or it can be a hook for silicon code

Global NVS

- ACPI region, passes configuration from C code to ASL code.

TIP: Use PCD Instead of UEFI Variable

UEFI Variable

```
//  
// Get config from setup variable  
//  
VarDataSize = sizeof (SETUP_DATA);  
Status = GetVariable (  
    L"Setup",  
    &gSetupVariableGuid,  
    NULL,  
    &VarDataSize,  
    &mSystemConfiguration  
);
```

PCD

```
//  
// Get setup configuration from PCD  
//  
CopyMem (  
    &mSystemConfiguration,  
    PcdGetPtr (PcdSetupConfiguration),  
    sizeof(mSystemConfiguration)  
);
```

DEC

PCD defined in the DEC file from any package

[Guids.common]

PcdTokenSpaceGuidName={0x914AEBE7, 0x4635, 0x459b, { 0xAA, . . . }}

• • •

[Pcds...]

PcdTokenSpaceGuidName.PcdTokenName | Value[| DatumType[| MaxSize]] | Token

INF

PCD usage listed in INF file for module

[...Pcd...]

PcdTokenSpaceGuidName.PcdTokenName | [Value]

DSC

Value of PCD set in OpenBoardPkg...dsc

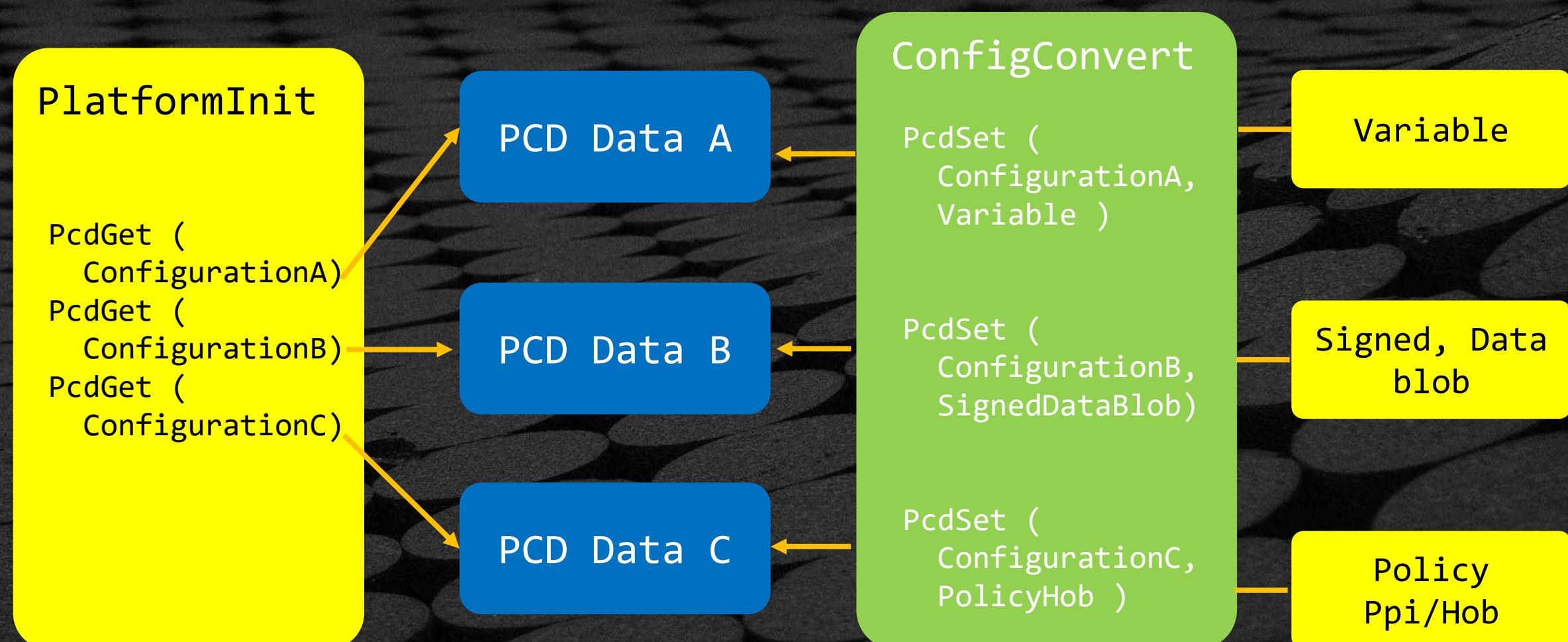
[Pcds...]

PcdTokenSpaceGuidName.PcdTokenName | Value[| DatumType[| MaximumDatumSize]]

How to Map PCD to Configuration Data

Using “**Callback**” mechanism to convert PCD to Configuration data

Platform driver should use PcdGet() to retrieve policy data, and PcdSet() to update policy data.



“C” Data Structure as PCDs

Example: AdvancedFeaturePkg.dec for SMBIOS type 0 data structure

```
gAdvancedFeaturePkgTokenSpaceGuid.PcdSmbiosType0BiosInformation| \
    {0x0}|SMBIOS_TABLE_TYPE0|0x80010000 {
    <HeaderFiles>
        IndustryStandard/Smbios.h
    <Packages>
        MdePkg/MdePkg.dec
        AdvancedFeaturePkg/AdvancedFeaturePkg.dec
}
gAdvancedFeaturePkgTokenSpaceGuid.PcdSmbiosType0BiosInformation.Vendor|0x1
gAdvancedFeaturePkgTokenSpaceGuid.PcdSmbiosType0BiosInformation.BiosVersion|0x2
gAdvancedFeaturePkgTokenSpaceGuid.PcdSmbiosType0BiosInformation.BiosSegment|0xF000
gAdvancedFeaturePkgTokenSpaceGuid.PcdSmbiosType0BiosInformation.BiosReleaseDate|0x3
gAdvancedFeaturePkgTokenSpaceGuid.PcdSmbiosType0BiosInformation.BiosSize|0xFF
gAdvancedFeaturePkgTokenSpaceGuid.PcdSmbiosType0BiosInformation.BiosCharacteristics.\
    PciIsSupported|1
gAdvancedFeaturePkgTokenSpaceGuid.PcdSmbiosType0BiosInformation.BiosCharacteristics.\
    PlugAndPlayIsSupported|1
```

Example of DSC xRef (.DEC & .h)

Purley Pkg DEC File

```
## gEfiSetupVariableGuid
OemSkuTokenSpaceGuid.PcdSetupData|{0x0}| \
SYSTEM_CONFIGURATION|0x000F0001 {
<HeaderFiles>
    Guid/SetupVariable.h
<Packages>
    MdePkg/MdePkg.dec
    PurleyRcPkg/RcPkg.dec
    PurleySktPkg/SocketPkg.dec
    LewisburgPkg/PchRcPkg.dec
    PurleyOpenBoardPkg/PlatPkg.dec
}
```

“C” SetupVariable.h File

```
...
UINT8    FanPwmOffset;
UINT8    WakeOnLanSupport;
UINT8    Use1GPageTable;
UINT8    CloudProfile;
} SYSTEM_CONFIGURATION;
```

StructureConfig.DSC File

```
gOemSkuTokenSpaceGuid.PcdSetupData. \
CloudProfile|0x0

gOemSkuTokenSpaceGuid.PcdSetupData. \
Use1GPageTable|0x1

gOemSkuTokenSpaceGuid.PcdSetupData. \
FanPwmOffset|0x0

gOemSkuTokenSpaceGuid.PcdSetupData. \
WakeOnLanSupport|0x0
```

...

Configuration Multi-SKU PCD – Board ID

DSC File – SKU Set at BUILD time

```
• • •  
SKUID_IDENTIFIER = ?  
  
[SkuIds]  
0|DEFAULT  
4|BoardX  
0x42|BoardY  
  
[PcdsDynamicDefault.common.BoardX]  
gBoardModuleTokenSpaceGuid.PcdGpioPin|0x8  
gBoardModuleTokenSpaceGuid.PcdGpioInitValue|\  
{0x00, 0x04, 0x02, 0x04, ...}  
  
[PcdsDynamicDefault.common.BoardY]  
gBoardModuleTokenSpaceGuid.PcdGpioPin|0x4  
gBoardModuleTokenSpaceGuid.PcdGpioInitValue|\  
{0x00, 0x02, 0x01, 0x02, ...}
```

SKU PCD Set Dynamically

```
BoardXBoardDetect( VOID)  
{  
    . . .  
    if (LibPcdGetSku () != 0) {  
        return EFI_SUCCESS;  
    }  
    if (IsBoardX ()) {  
        LibPcdSetSku (BoardIdIsBoardX);  
        ASSERT (LibPcdGetSku() ==  
                BoardIdIsBoardX);  
    }  
    return EFI_SUCCESS;  
}
```

Default Stores PCD – for Configuration

DSC File –

```
• • •  
VPD_TOOL_GUID = 8C3D856A-9 ...
```

```
[DefaultStores]  
0|STANDARD  
1|MANUFACTURING  
2|SAFE
```

- Special PCD to support the default stores concept in UEFI specification
- Can be Dynamically set

```
[PcdsDynamicExVpd.common.DEFAULT]  
gEfiMdeModulePkgTokenSpaceGuid.PcdNvStoreDefaultValueBuffer|*  
[PcdsDynamicEx.common.DEFAULT.STANDARD]  
gOemSkuTokenSpaceGuid.PcdSetupData.CloudProfile|0x0  
gOemSkuTokenSpaceGuid.PcdSetupData.Use1GPageTable|0x1  
[PcdsDynamicEx.common.DEFAULT.MANUFACTURING]  
gOemSkuTokenSpaceGuid.PcdSetupData.CloudProfile|0x1  
gOemSkuTokenSpaceGuid.PcdSetupData.Use1GPageTable|0x0
```

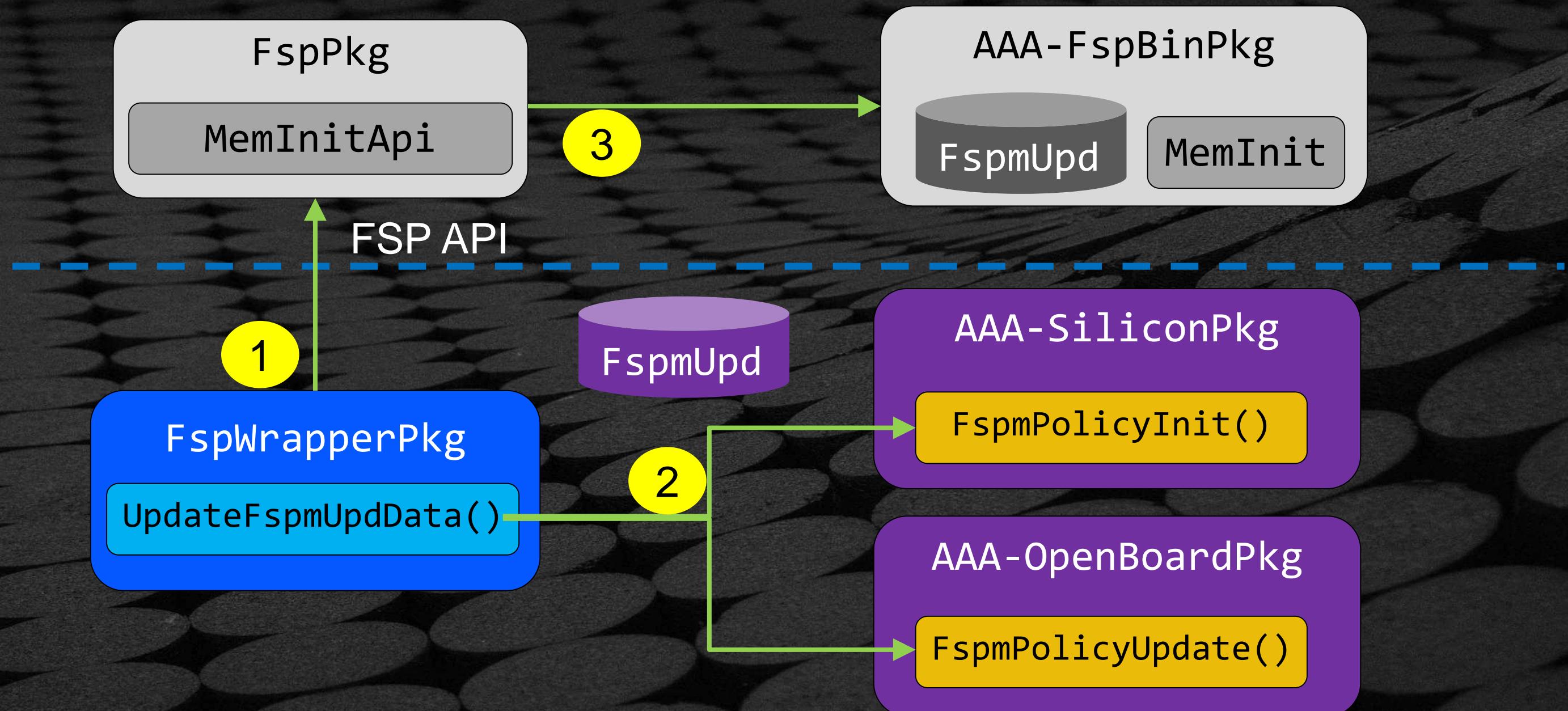
Silicon Policy Data Flow Guidelines

Silicon Module Provides Default Silicon Policy Data

Board Module Updates the Silicon Policy Data

- Typedef data structure
- PCD database, Setup Variable, Binary Blob, etc.

Example: FSP policy in MinPlatformPkg



Update Silicon Policy example

KabylakeOpenBoardPkg/FspWrapper/Library/PeiSiliconPolicyUpdateLibFsp

```
EFI_STATUS  
EFIAPI  
PeiFspSaPolicyUpdatePreMem (   
    IN OUT FSPM_UPD *FspmUpd  
)  
{  
    VOID *Buffer;  
    // Override MemorySpdPtr  
    CopyMem((VOID *)(UINTN)\br/>        FspmUpd->FspmConfig.MemorySpdPtr00,\br/>        (VOID *)(UINTN)PcdGet32 (PcdMrcSpdData), \br/>        PcdGet16 (PcdMrcSpdDataSize));  
    CopyMem((VOID *)(UINTN)\br/>        FspmUpd->FspmConfig.MemorySpdPtr10,\br/>        (VOID *)(UINTN)PcdGet32 (PcdMrcSpdData), \br/>        PcdGet16 (PcdMrcSpdDataSize));
```

```
    • • •  
    // Updating Dq Pins Interleaved,Rcomp Resistor &  
    // Rcomp Target Settings  
  
    Buffer = (VOID *) (UINTN) PcdGet32 \br/>        (PcdMrcRcompTarget);  
    if (Buffer) {  
        CopyMem ((VOID *)\br/>            FspmUpd->FspmConfig.RcompTarget, \br/>            Buffer, 10);  
    }  
    return EFI_SUCCESS;  
}
```

Link to file: [PeiSaPolicyUpdatePrMem.c](#)

Dynamically Set Defaults

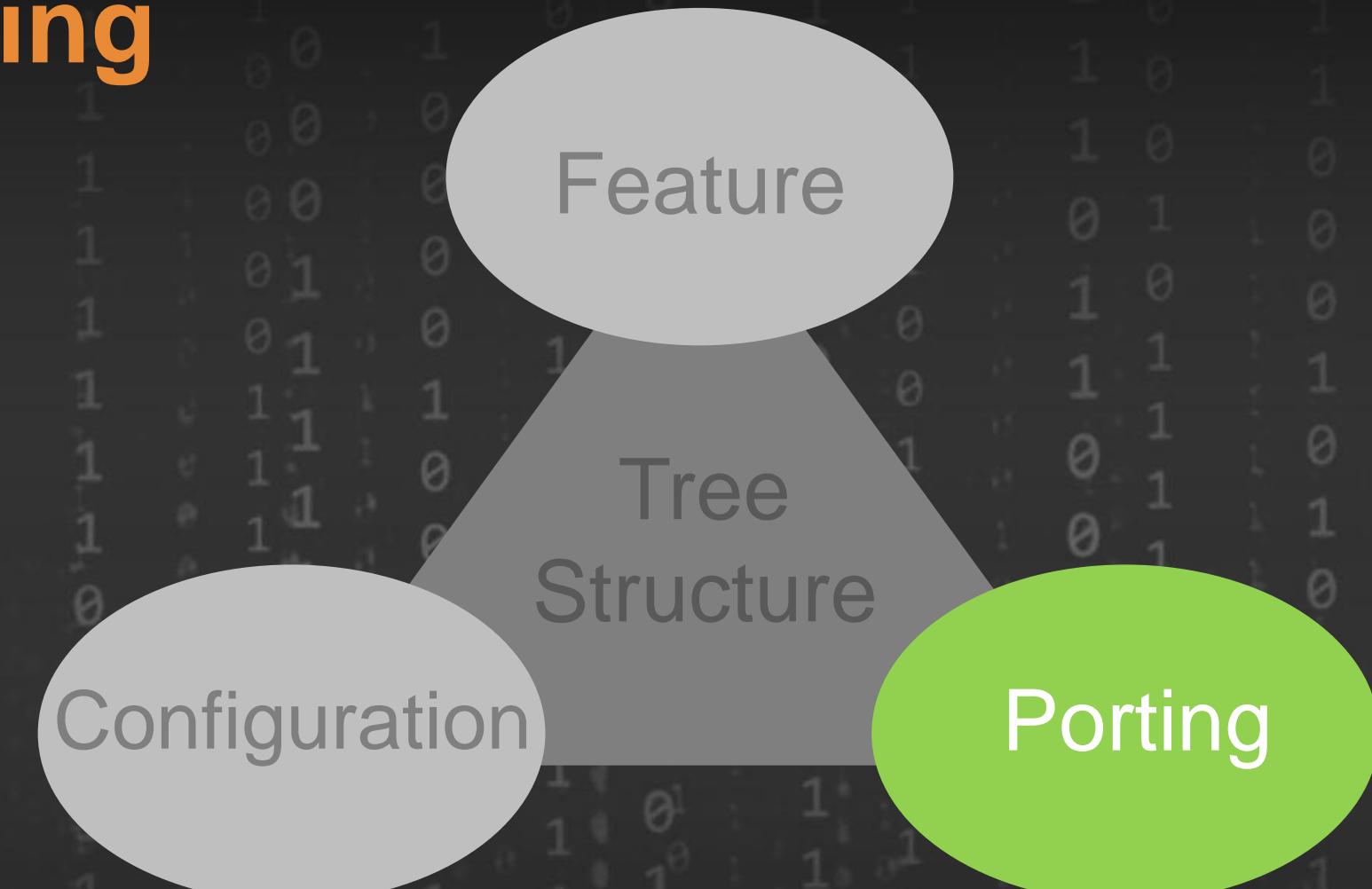
The Default Store PCD is also a dynamic PCD.

During boot, the board initialization code checks the boot mode and selects the default store.

This step must be after SetSku. Otherwise, the default setting may be wrong.

```
...
if (NeedDefaultConfig()) {
    PcdSet16S (PcdSetNvStoreDefaultId, 0x0);
}
```

Board Porting



- Staged
- GPIO
- SIO
- ACPI

Staged Approach by Features

- Platform Firmware Boot Stage PCD

PCD Variable:

gPlatformModuleTokenSpaceGuid.PcdBootStage

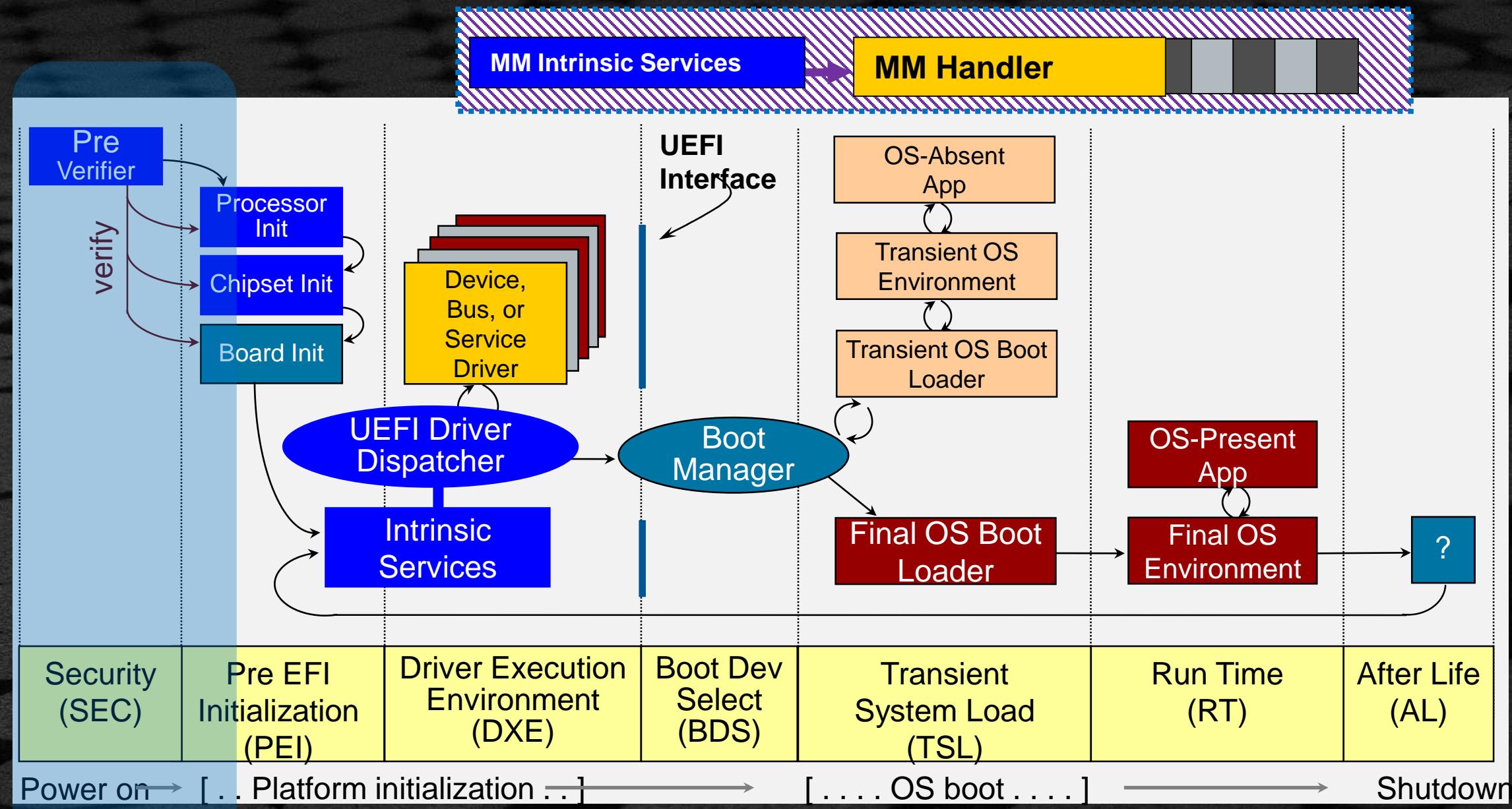
Stage 1	enable debug
Stage 2	memory initialization
Stage 3	boot to UEFI shell only
Stage 4	boot to OS
Stage 5	boot to OS w/ security enabled
Stage 6	Advanced Feature Selection
Stage 7	Performance Optimizations



PCD Is tested within .fdf to see
which modules to include

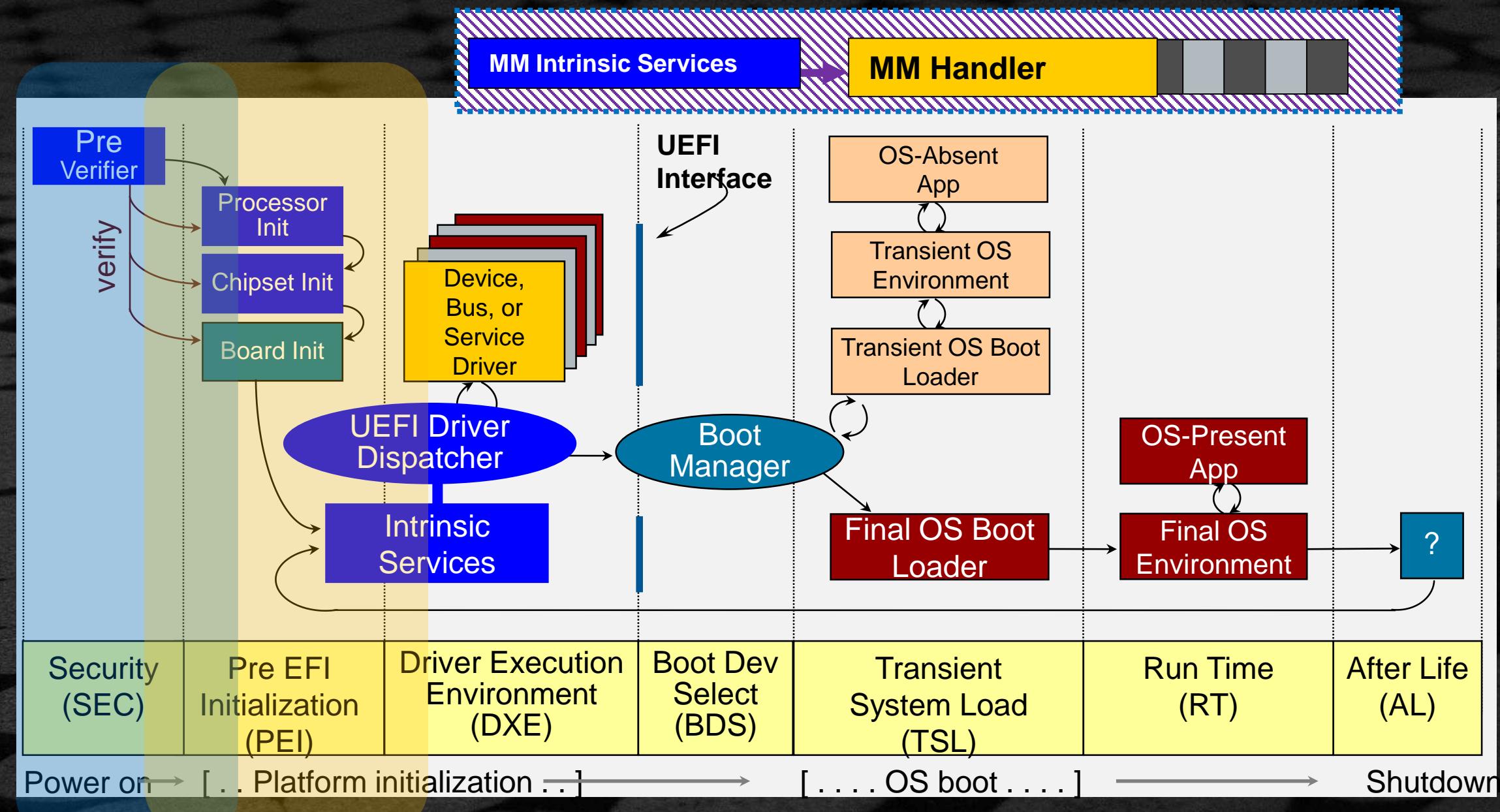
Stages vs. Boot Flow

Stage 1



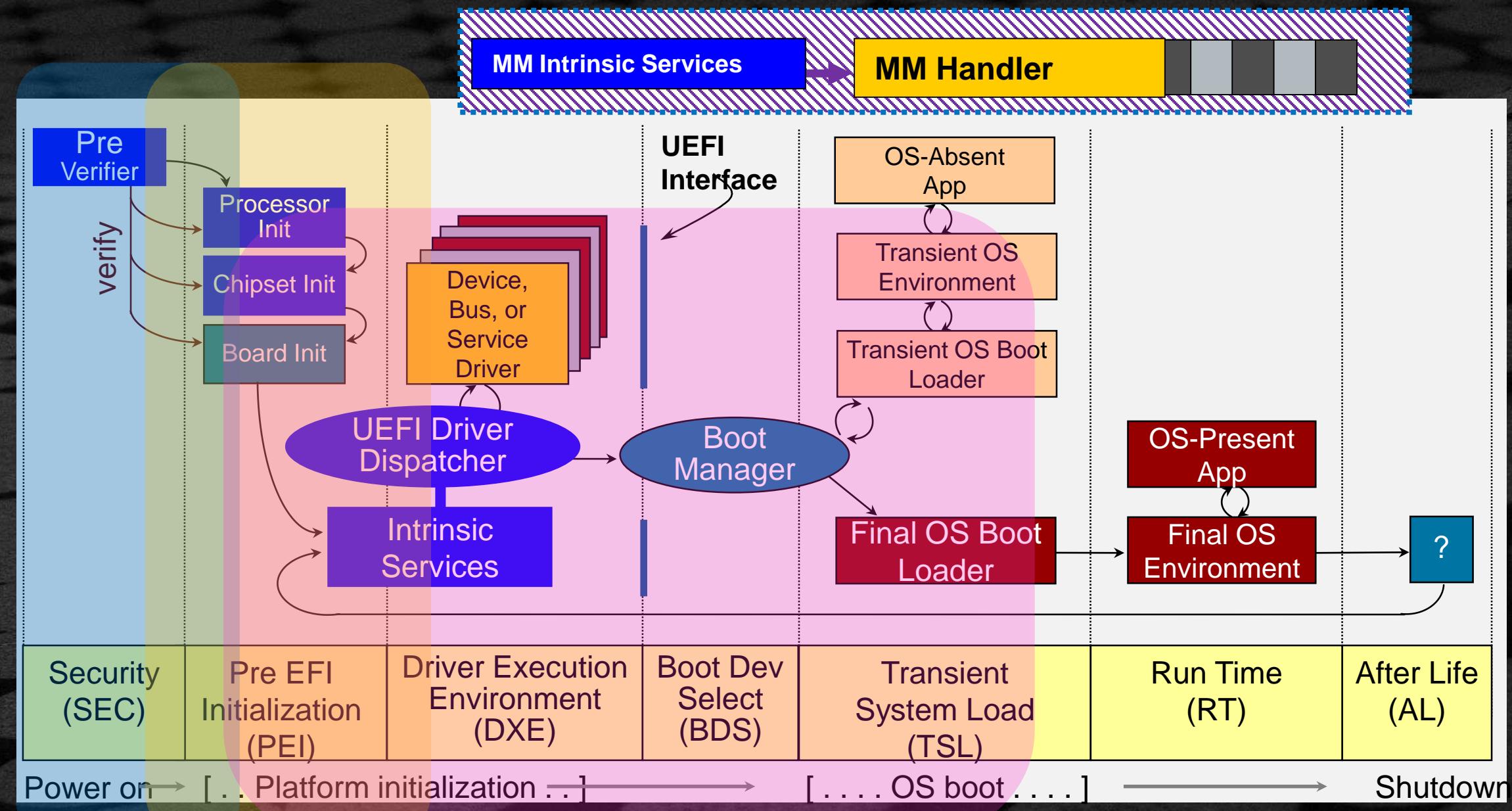
Stages vs. Boot Flow

Stage 1 Stage 2

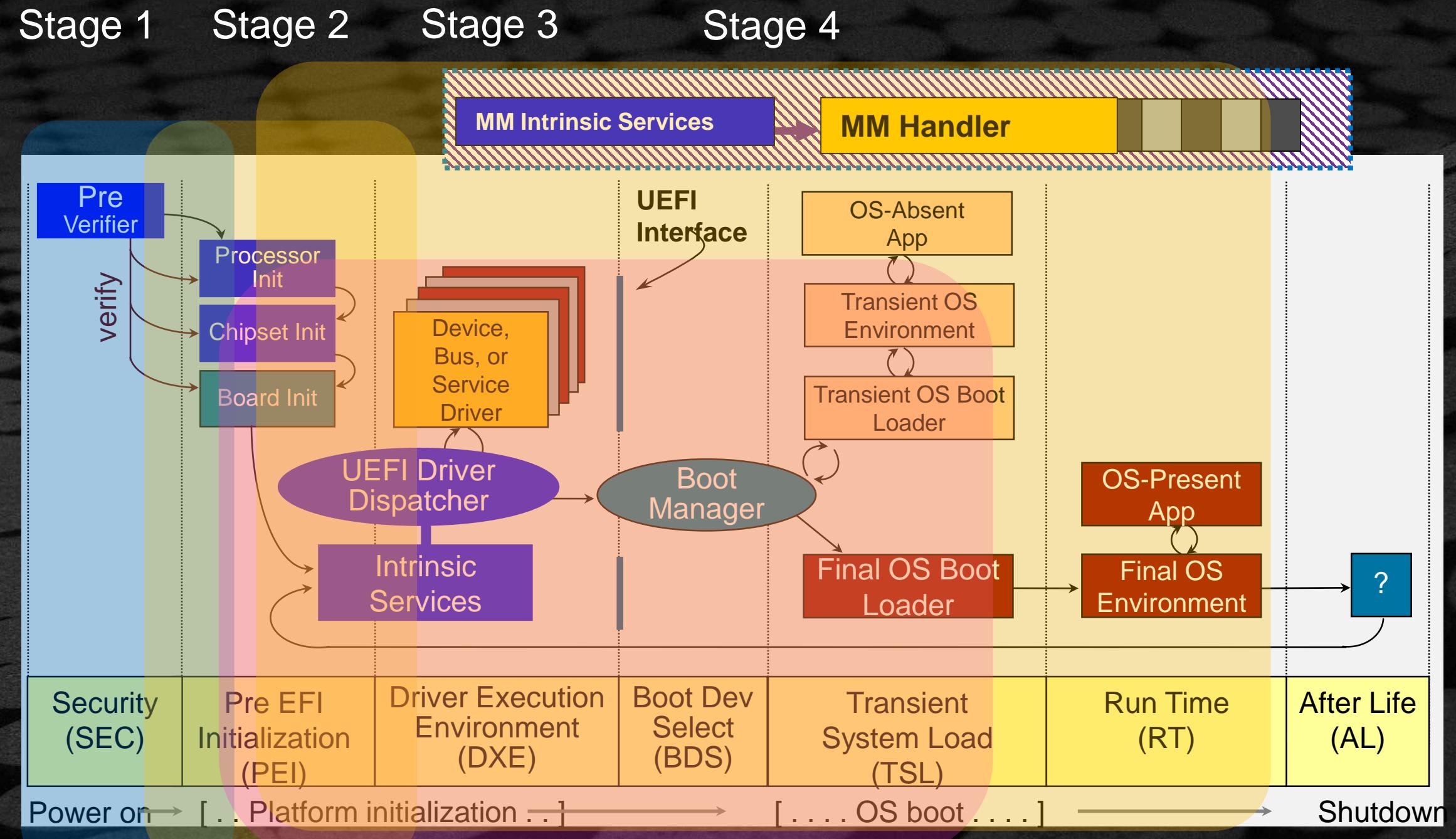


Stages vs. Boot Flow

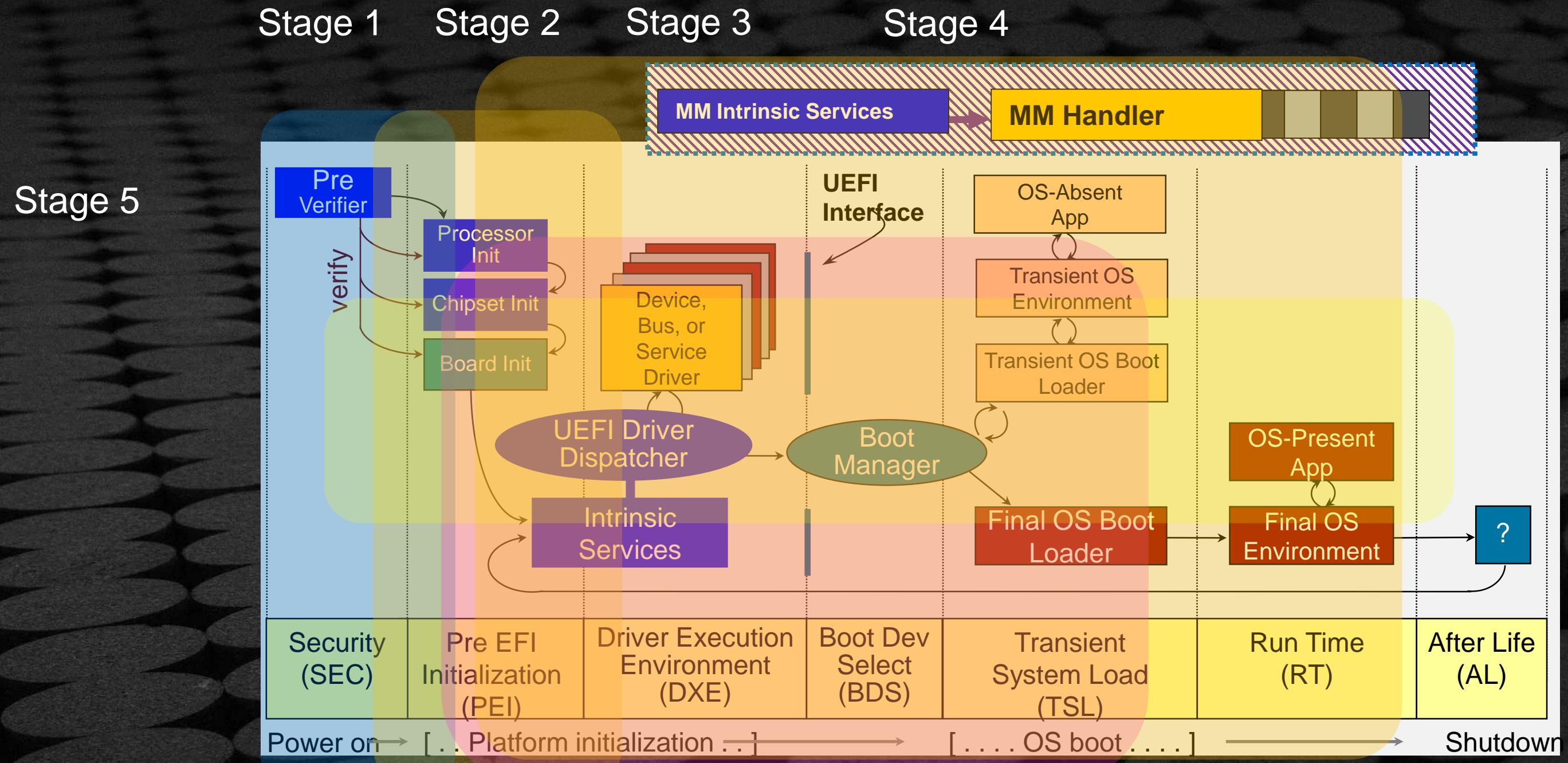
Stage 1 Stage 2 Stage 3



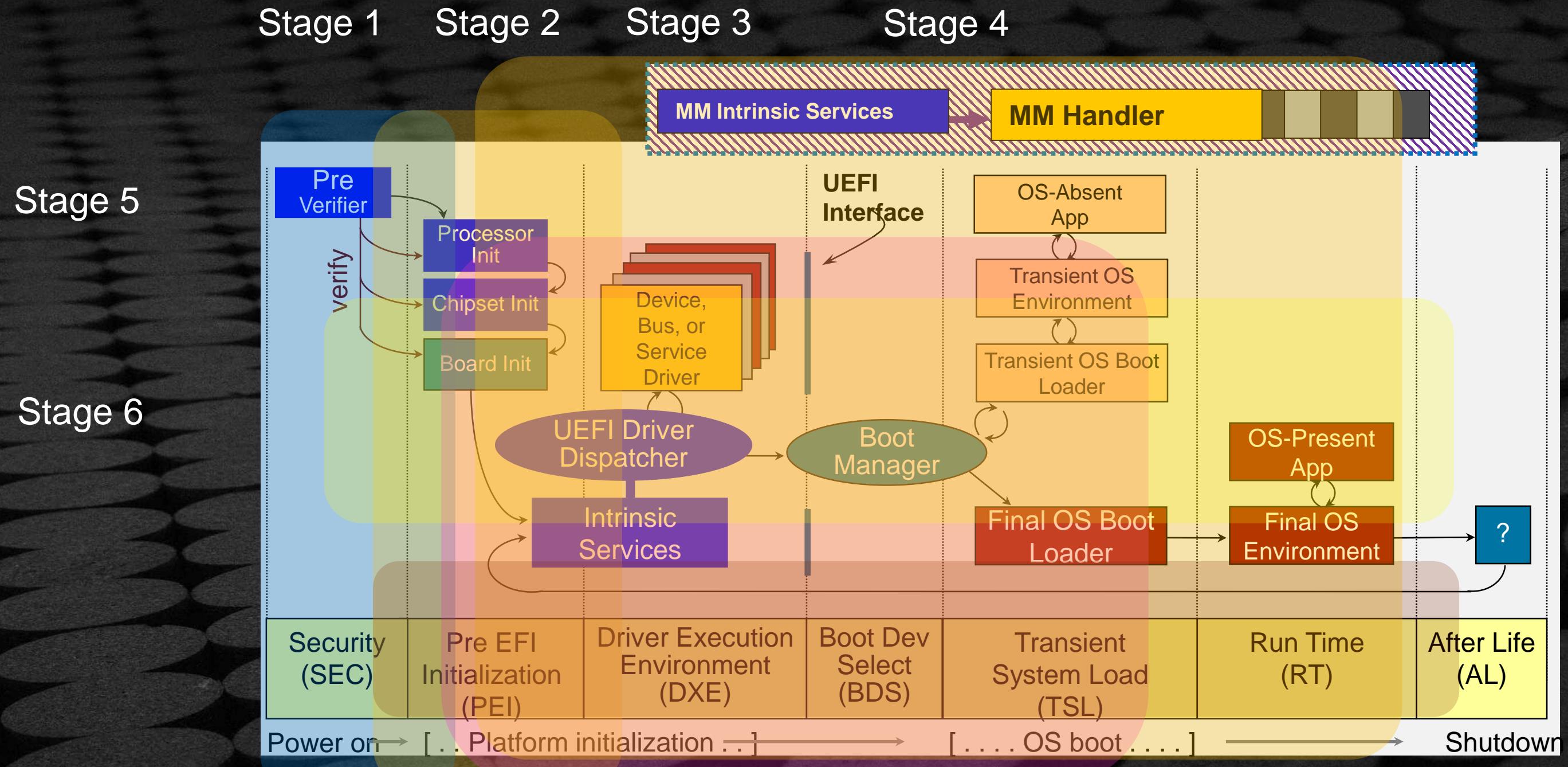
Stages vs. Boot Flow



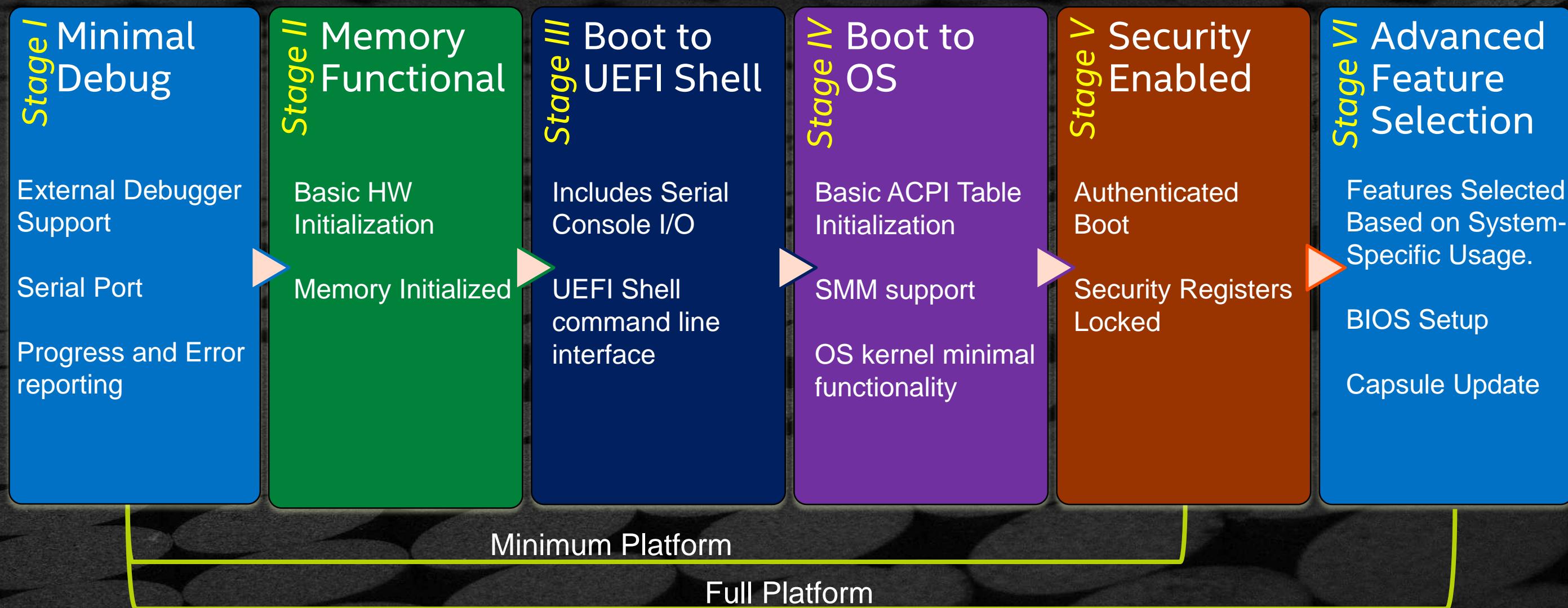
Stages vs. Boot Flow



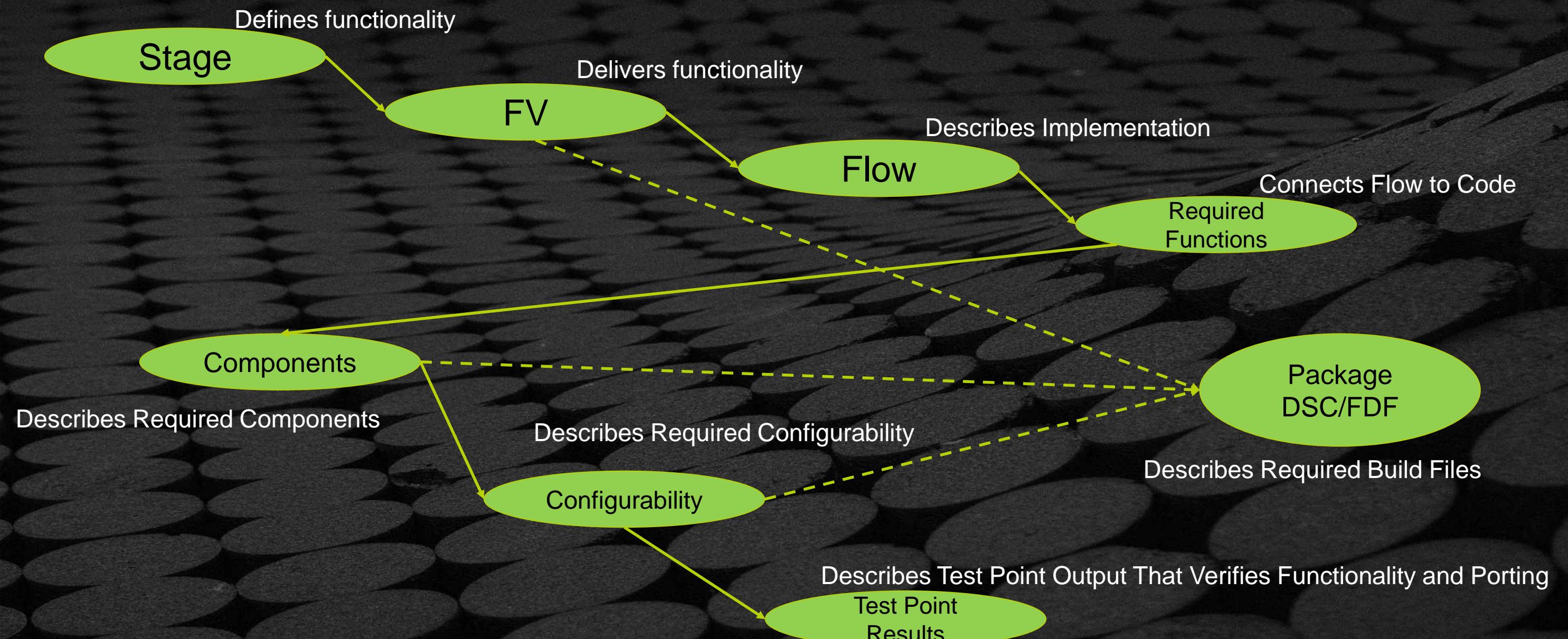
Stages vs. Boot Flow



Minimum Platform + Intel® FSP Boot Flow - Staged Approach

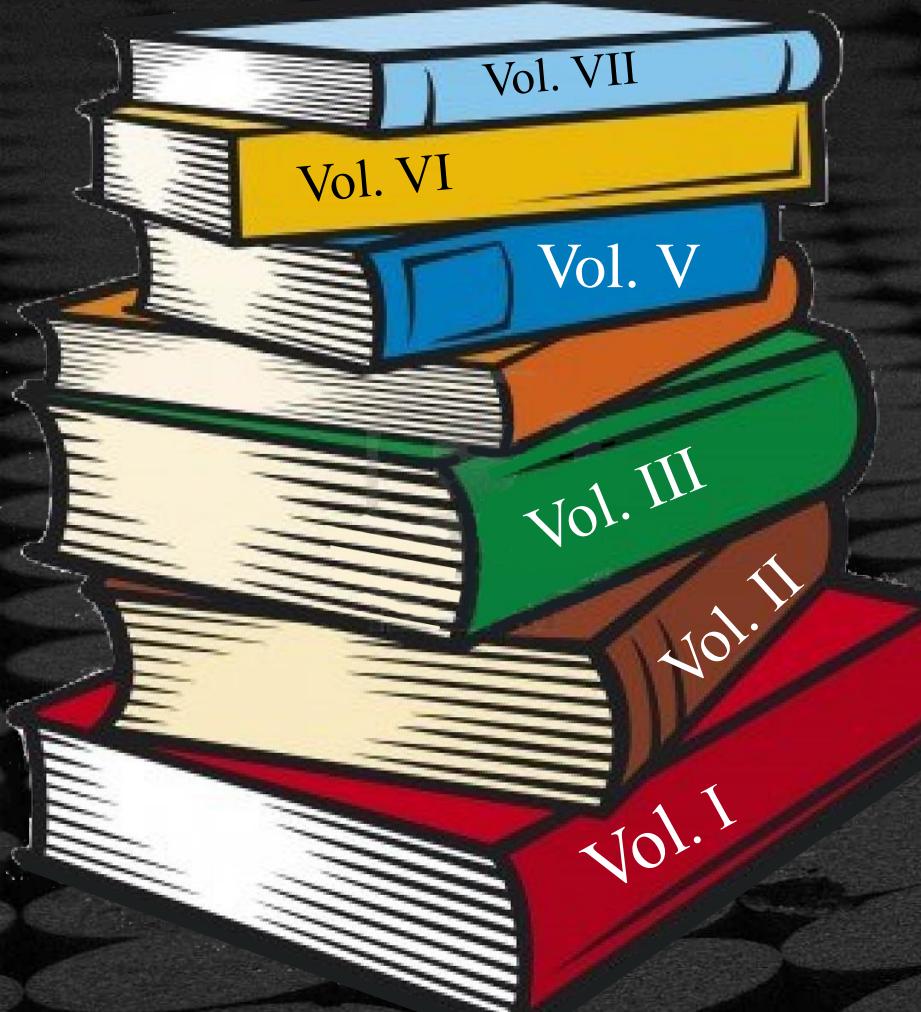


Stages Organize the MPA Specification



Staged Approach by Features

- Firmware Volume

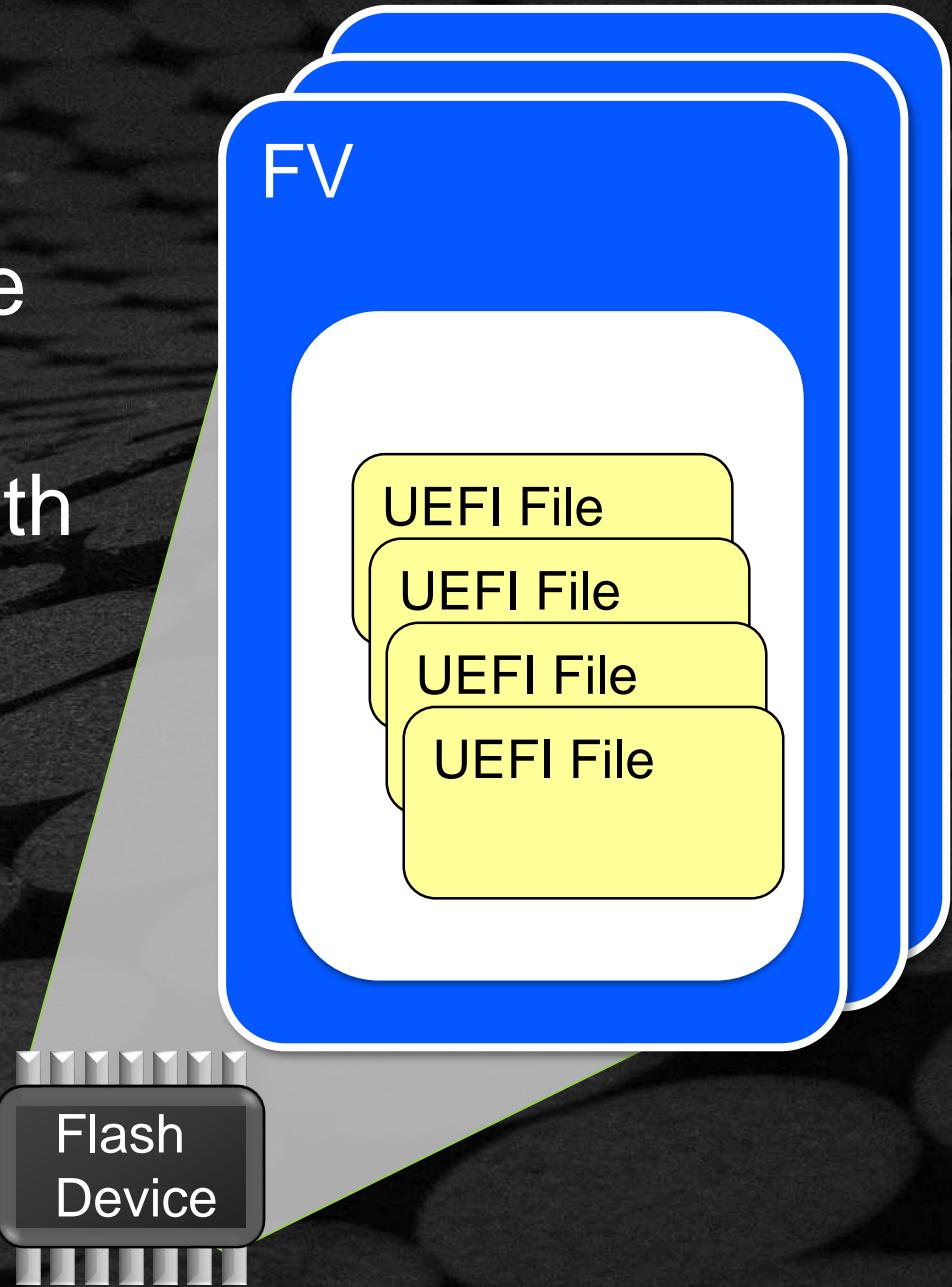


Modules organized by Firmware
Volumes according to the different
boot stages

UEFI Firmware Volumes (FV) - Review

Platform Initialization - Firmware Volume

- Basic storage repository for data and code is the Firmware Volume (FV)
- Each FV is organized into a file system, each with attributes
- One or more Firmware File Sections (FFS) files are combined into a FV
- Flash Device may contain one or more FVs.
- .FDF file controls the layout → .FD image(s)



Standardize FV By Stages

Pre-Memory

- **FvPreMemory** – The PEIM dispatched before the memory initialization. Also included **FSP - FV**

Post Memory

- **FvPostMemory** – The PEIM dispatched after the memory initialization. Also included **FSP - FV**

UEFI Boot

- **FvUefiBoot** – The DXE driver supporting UEFI boot, such as boo to UEFI shell.

OS Boot

- **FvOsBoot** – The DXE driver supporting UEFI OS boot, such as UEFI Windows.

Security

- **FvSecurity** – The security related modules, such as UEFI Secure boot, TPM etc.

Advanced

- **FvAdvanced** – The advanced feature modules, such as UEFI network, IPMI etc.

FSP Firmware Volumes

– created Pre-Build

Fsp.fd Rebased for FVs

MyWorkSpace/
edk2/

- “*edk2 Common*”

edk2-platforms/

Platform/Intel “*Platform*”

KabyLakeOpenBoardPkg/
include/fdf \

FlashMapInclude.fdf

BoardXPkg/ “*Board*”

Silicon/ “*Silicon*”

Intel/MinPlatformPkg/

edk2-non-osi/

Silicon/Intel/

FSP/

BoardXPkg

Fsp.fd

FvFspT

- – Temp Memory

FvFspM

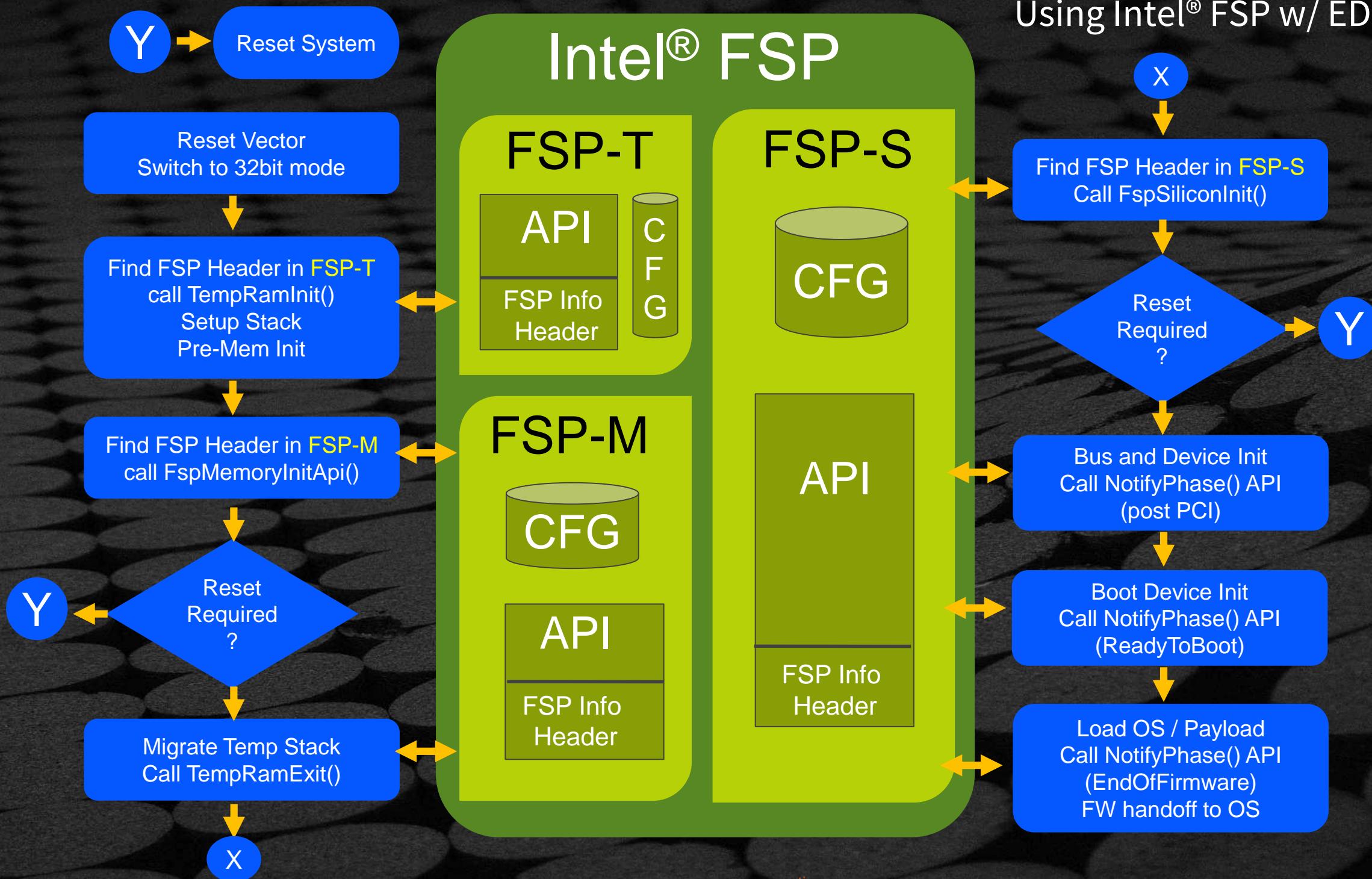
- -> FvPreMemorySilicon

FvFspS

- -> FvPostMemorySilicon

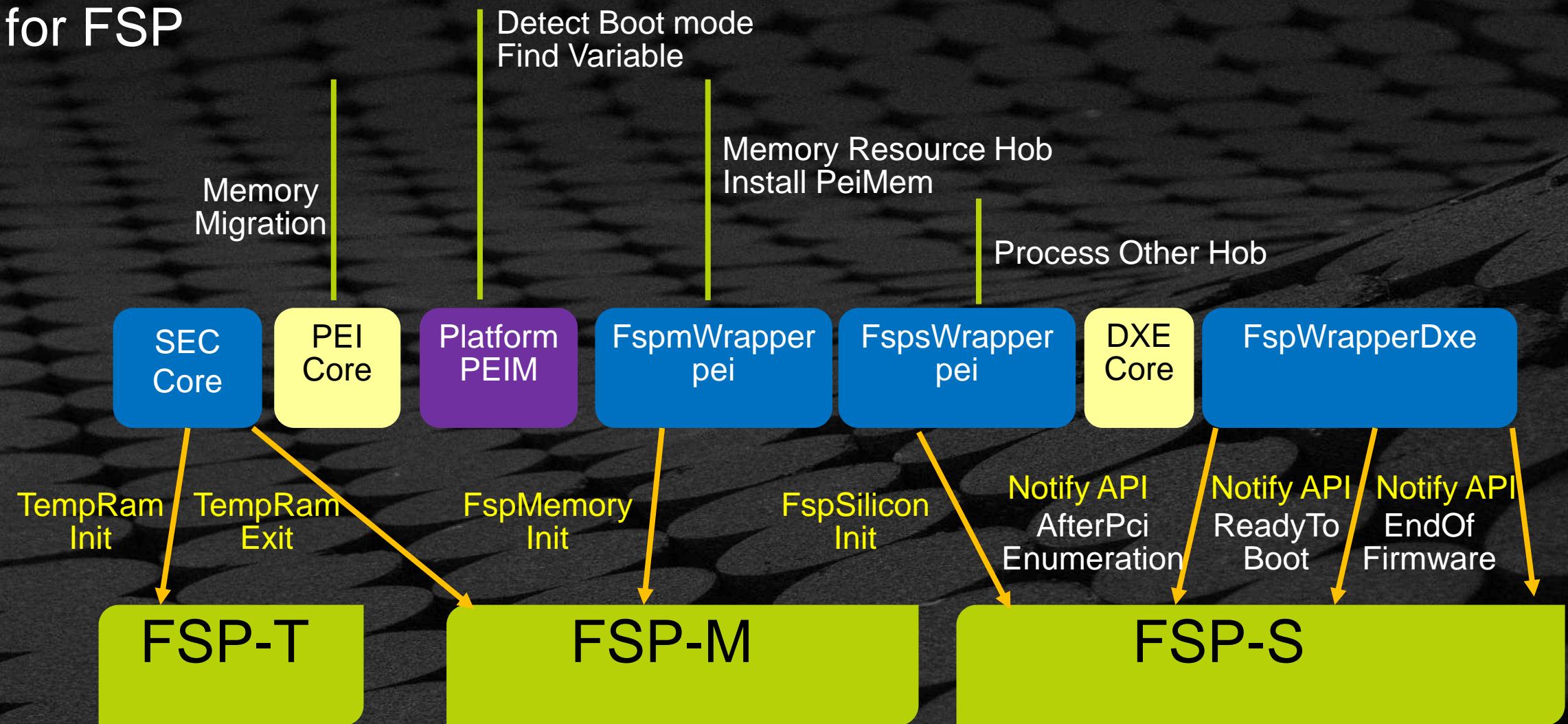
Pre-Build w/
RebaseAndPatchFspBinBaseAddress.py

FSP APIs in FSP Binary



Boot Flow with FSP API Mode

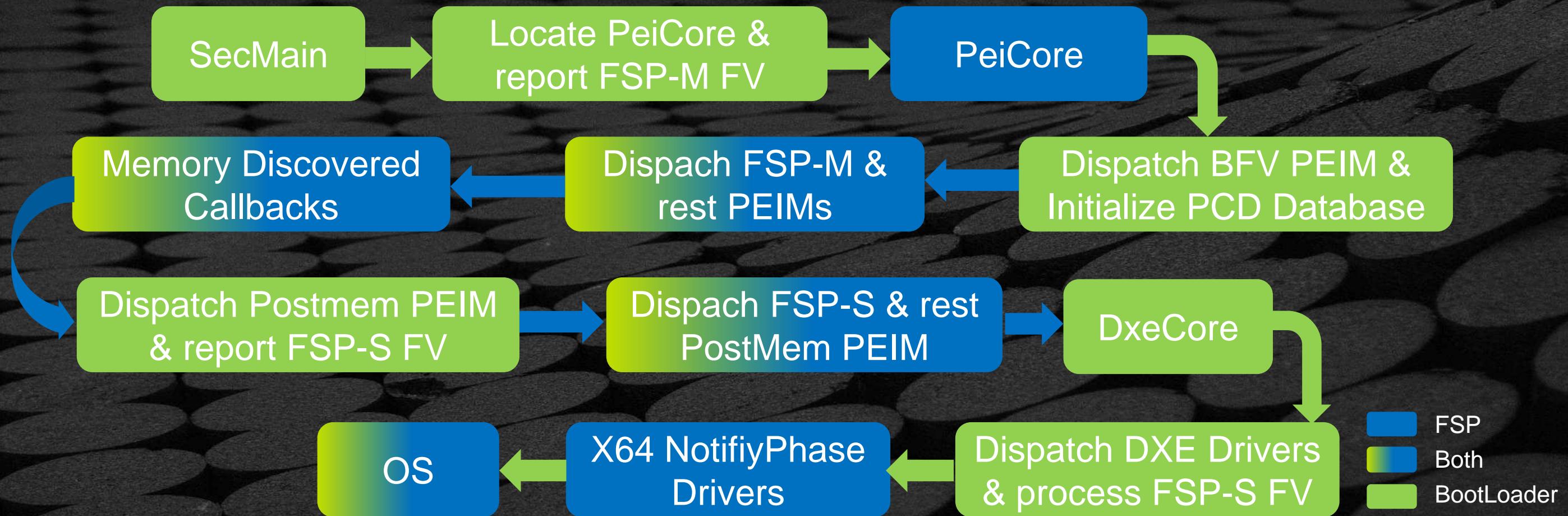
5 APIs for FSP



Source: [Using the Intel® FSP with EDK II \(2.0\)](#) Fig 4.

FSP 2.1 Dispatch Mode Boot Flow

`gIntelFsp2WrapperTokenSpaceGuid.PcdFspModeSelection` 0 - dispatch, 1 – API



PLATFORM HOOKS

Using EDK II Libraries



EDK II Libraries w/ Platform Hooks



DSC maps library class to library-instances

Syntax in DSC file

[libraryclasses]

LibraryClassName|Path/To/LibInstanceNameInstance1.inf

Search INF files for string: “LIBRARY_CLASS =”

Library Classes Section in DSC



DebugLib class example

Library Class Section

```
[LibraryClasses]
  DebugLib|MdePkg/Library/BaseDebugLibNull/BaseDebugLibNull.inf
  ...
  ...
```

```
[LibraryClasses.common.DXE_CORE]
  ...
  DebugLib|IntelFrameworkModulePkg/Library/PeiDxeDebugLibReportStatusCode/
    PeiDxeDebugLibReportStatusCode.inf
  ...
  ...
```

```
[LibraryClasses.common.DXE_SMM_DRIVER]
  DebugLib|MdePkg/Library/BaseDebugLibNull/BaseDebugLibNull.inf
```

Components Section

```
[Components]
  ...
MyPath/MyModule.inf {
<LibraryClasses>
  DebugLib|MdePkg/Library/BaseDebugLibSerialPort.inf
}
```

Platform Initialization Board Hook Modules

MinPlatformPkg/
Include/
Library/
BoardInitLib.h
Library/
.
.
.
PlatformInit/
PlatformInitPei/
PlatformInitPreMem/
PlatformInitPostMem/
PlatformInitDxe/
PlatformInitSmm/

BoardDetect()
BoardDebugInit()
BoardBootModeDetect()
BoardInitBeforeMemoryInit()
BoardInitBeforeTempRamExit()
BoardInitAfterTempRamExit()
BoardInitAfterMemoryInit()
BoardInitBeforeSiliconInit()

BoardInitAfterPciEnumeration()
BoardInitReadyToBoot()
BoardInitEndOfFirmware()

 PEI DXE

Platform Initialization Board Hook Modules

MinPlatformPkg/

• • •

PlatformInit/

PlatformInitPei/

PlatformInitPreMem/

PlatformInitPostMem/

PlatformInitPreMem/

BoardDetect()

BoardDebugInit()

BoardBootModeDetect()

BoardInitBeforeMemoryInit()

• • •

Notify call back

BoardInitAfterMemoryInit()

PEI

PlatformInitPostMem/

BoardInitBeforeSiliconInit()

• • •

BoardInitAfterSiliconInit()

Platform Initialization Board Hook Modules

- Stage 1



```
MinPlatformPkg/  
Include/  
Library/  
BoardInitLib.h ← // hooks  
Library/  
.  
.  
.  
PlatformInit/  
PlatformInitPei/  
PlatformInitPreMem/
```

BoardDetect()
BoardDebugInit()
BoardBootModeDetect()
BoardInitBeforeMemoryInit()

Platform folder PlatformInit controls
the platform initialization flow

MinPlatformPkg/

...

PlatformInit/

PlatformInitPei ->

PlatformInitPreMem.c

BoardDetect()

KabylakeOpenBoardPkg/

...

KabylakeRvp3/

Library/

BoardInitLib ->

PeiBoardInitPreMemLib.c

BoardDetect()

PeiKabylakeRvp3Detect.c

KabylakeRvp3BoardDetect()

Hook - Board Detection

-Kabylake example



Uses PCD Library calls to set / get
Board SKU for Storing Board ID

LibPcdGetSku() & LibPcdSetSku()

KabylakeRvp3BoardDetect() function reads
Board ID from embedded controller (EC) using
the LPC bus

LibPcdSetSku() stores Board ID

LibPcdGetSku() used from that point on

Stage 1 - Board Pre-mem Lib Summary

Example: Kabylake –

KabylakeOpenBoardPkg/KabylakeRvp3/Library/BoardInitLib/**PeiBoardInitPreMemLib**

1. Add Board pre-memory debug initialization code in `BoardDebugInit ()`
2. Ensure all PCDs in the Configuration section are correct (i.e. Serial debug)
3. Verify values of other PCDs are correct
4. Verify the flash layout is compliant
5. Verify the required binaries included in the build
6. Verify debug output during the code execution path for Stage 1
7. Verify the test point results are correct

Staged Approach by Features

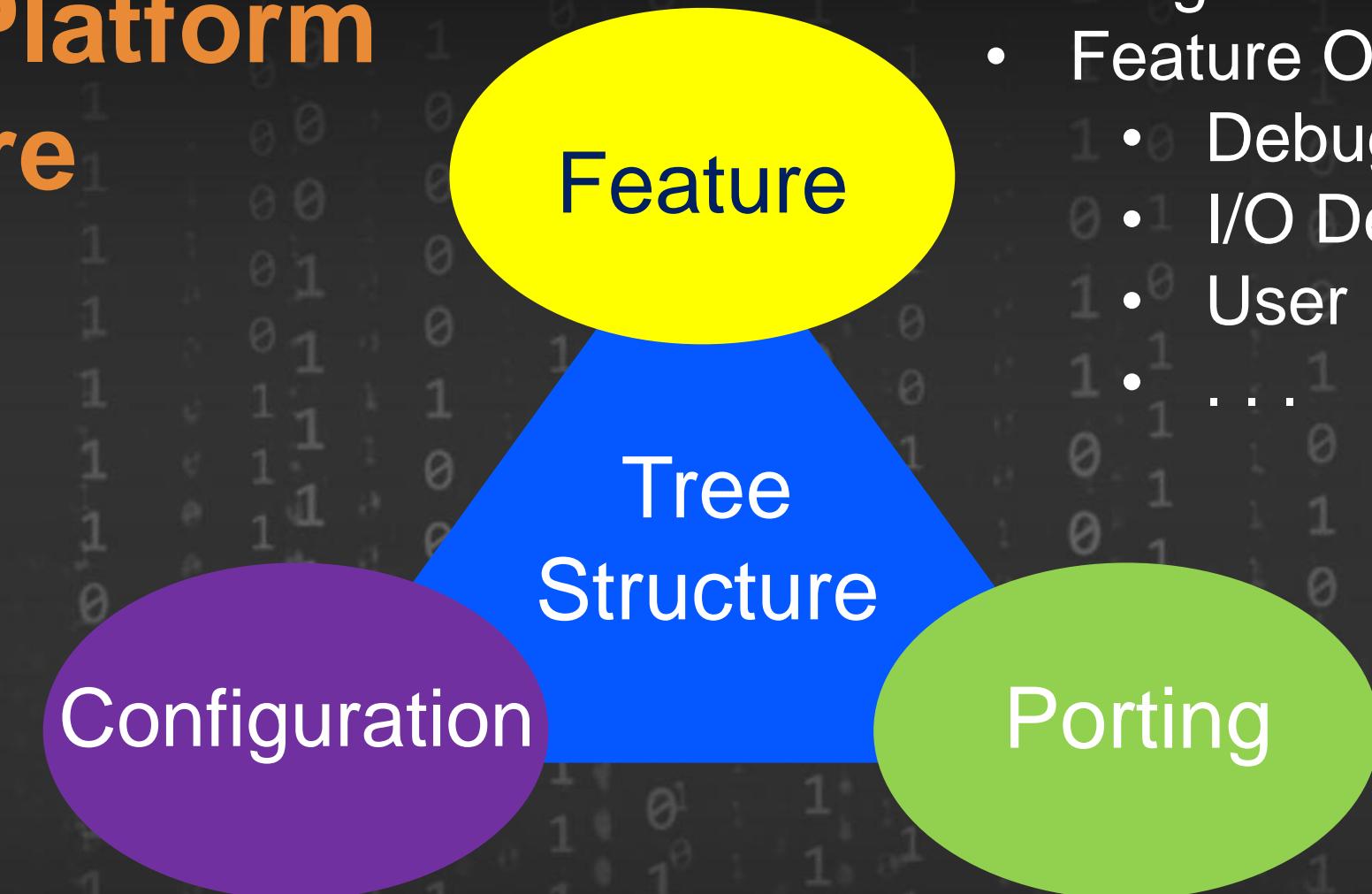
- Platform Firmware Boot Stage PCD

Summary

Stage 1	enable debug	FSP-T, Serial Debug, GPIO
Stage 2	memory initialization	Pre-silicon FSP-M post-silicon
Stage 3	boot to UEFI shell only	FSP-S Dxelpl DxeMain BDS
Stage 4	boot to OS	ACPI S3
Stage 5	boot to OS w/ security enabled	TPM Secure boot
Stage 6	Advanced Feature Selection	Network, SMBIOS
Stage 7	Performance Optimizations	

PCD Is tested within .FDF to see which modules to include

Minimum Platform Architecture Summary



- Staged
- Defined PCD
- Policy Hob/PPI/Protocol

- Staged Minimal Baseline
- Feature ON/OFF
 - Debug
 - I/O Devices
 - User Interface
 - ...

- Staged
- GPIO
- SIO
- ACPI

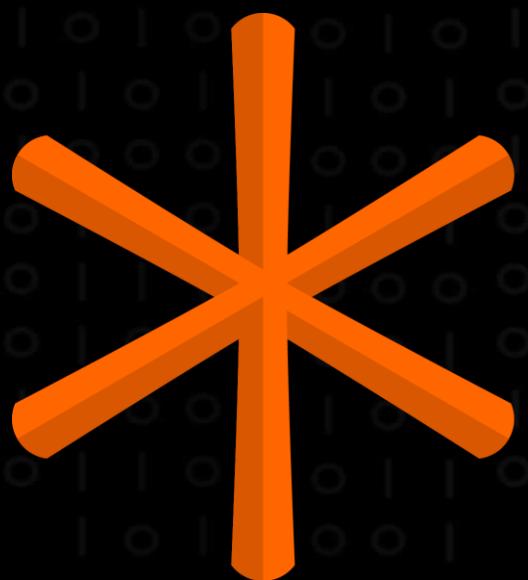
LESSON OBJECTIVE

- ★ Introduce Minimum Platform Architecture (MPA)
- ★ Explain the EDK II Open board platforms infrastructure & focus areas
- ★ Describe Intel® FSP with the EDK II open board platforms

Return to Main Training Page



Return to Training Table of contents for next presentation [link](#)



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BACK UP

Basic Boot Components

UEFI

Variable

Timer

CPU

ACPI

AcpiTable

SMM

SmmAccess

SmmControl

PCI

AcpiSmm

SmmCpu

SmmDispatch

SATA

SpiSmm

FvbSmm

GOP

Platform

Gpio

Sio

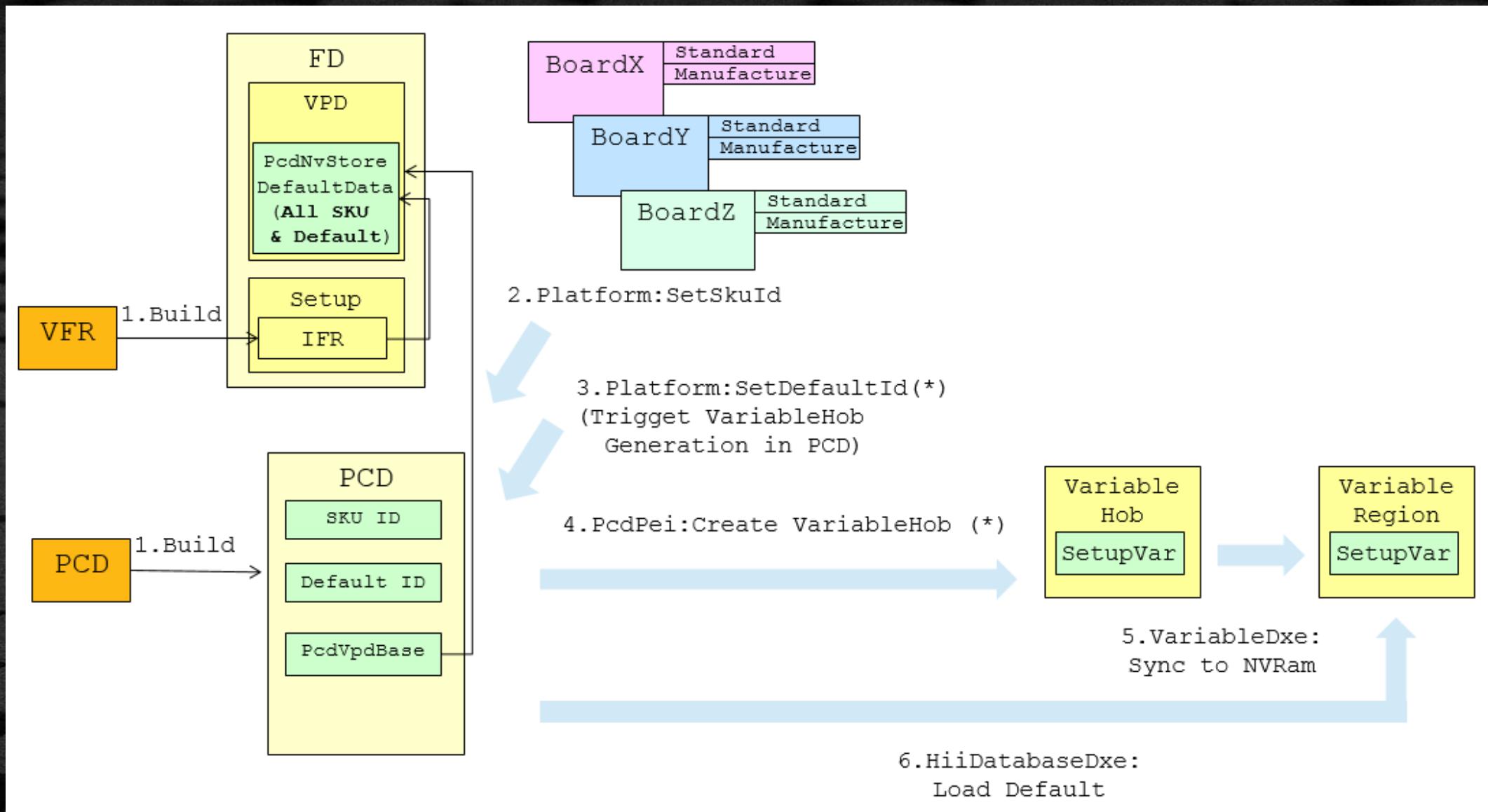
Key -

EDK II

Silicon

Platform

Board default setup variable data



Board Detection and Initialization Flow

