

**# Title:**

CXL CPER updates

**# Status:**

Draft

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UEFI Specification Version 2.*next*

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**# Submitter:**

- Mahesh Natu (Intel)
- Subhada Pugaonkar (Intel)
- Samer El-Haj Mahmoud (Arm)
- Thanu Rangarajan (Arm)
- TianoCore Community (<https://www.tianocore.org>)

**# Summary of the change**

This ECR is related to a proposal to update the current CPER structure for CXL to support CXL 2.0 definitions.

Specifically, the ECR includes the following changes:

1. Updates to section N.2.13 (Compute Express Link (CXL) Protocol Error Section) to accommodate CXL 2.0 specific definitions.

The changes are done in a manner to ensure backward compatibility with existing CXL 1.1 specific definitions.

**# Benefits of the change**

Enables support for error handling on systems that are CXL 2.0 aware.

**# Impact of the change**

Platforms firmware will have to support the new format of the CPER structure, and OS's will require a driver to support the new format. These are both fundamentally new code.

## # Detailed description of the change [normative updates]

Existing text

New text

Deleted Text

## N.2.xx Compute Express Link (CXL) Protocol Error Section

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Table N.xx ~~Table 94.~~ CXL Protocol Error Section

Field	Byte Offset	Byte Length	Description
Validation Bits	0	8	Indicates which of the following fields is valid: Bit 0 – CXL Agent Type field is valid Bit 1 – CXL Agent Address field is valid Bit 2 – Device ID field is valid Bit 3 – Device Serial Number field is valid Bit 4 – Capability Structure field is valid Bit 5 – CXL DVSEC field is valid Bit 6 – CXL Error Log field is valid Bits 7:63 – Reserved
CXL Agent Type	8	1	0 – This error was detected by a CXL 1.1 device 1 – This error was detected by a CXL 1.1 host downstream port 2 – This error was detected by CXL 2.0 device 3 – This error was detected by CXL 2.0 Logical Device 4 – This error was detected by CXL 2.0 Fabric Manager managed Logical device 5 – This error was detected by CXL 2.0 Root Port 6 – This error was detected by CXL 2.0 Downstream Switch Port 7 – This error was detected by CXL 2.0 Upstream Switch Port 8- 255 – Reserved In this table, the term “CXL Device” is used to refer to CXL 1.1 Device, CXL 2.0 Device, CXL 2.0 Logical Device or a CXL 2.0 Fabric Manager Managed Logical Device. In this table, the term “CXL Port” is used to refer to CXL 1.1 host downstream port, CXL Root Port, CXL Downstream Switch Port and Upstream Switch Port.
Reserved	9	7	Must be zero
CXL Agent Address	16	8	If this CXL agent is a CXL 1.1 device, CXL Root Port, CXL Downstream Switch Port or CXL Upstream Switch Port, the PCI compatible device number and bus number information to uniquely identify the Component.  Byte 0 – Function number Byte 1 – Device number Byte 2 – Bus number Bytes 3-4 – Segment number

			<p>Bytes 5-7 – Reserved</p> <p>If CXL agent is a CXL 1.1 host downstream port, Byte 0-7 – CXL Port RCRB Base address</p>
Device ID	24	16	<p>If this CXL agent is a CXL 1.1 device, a CXL Root Port, CXL Downstream Switch Port or CXL Upstream Switch Port, this field provides vendor-specific identifiers for the device, the PCI-compatible device number and bus number information to uniquely identify the device.</p> <p>Bytes 0-1: Vendor ID  Bytes 2-3: Device ID  Bytes 4-5: Subsystem Vendor ID  Bytes 6-7: Subsystem Device ID  Bytes 8-9: Class Code  Byte 10-11:  Bits 0:2: Reserved  Bits 3:15 Slot Number  Byte 12-15 Reserved</p>
Device Serial Number	40	8	<p>If this CXL agent is a CXL 1.1 device:  Byte 0-3: CXL Device Serial Number Lower DW  Byte 4-7: CXL Device Serial Number Upper DW</p>
Capability Structure	48	60	<p>If this CXL agent is a CXL 1.1 device, CXL Root Port, CXL Downstream Switch Port or CXL Upstream Switch Port, this is the PCIe Capability Structure of the agent.</p> <ul style="list-style-type: none"> <li>•The 60-byte structure is used to report device capabilities. This structure is used to report the 36-byte PCIe 1.1 Capability Structure (See Figure 7-9 of the PCI Express Base Specification, Rev 1.1) with the last 24 bytes padded.</li> <li>•This structure is also used to report the 60-byte PCIe 2.0 Capability Structure (See Figure 7-9 of the PCI Express 2.0 Base Specification.)</li> <li>•The fields in the structure vary with different device types.</li> <li>•The "Next CAP pointer" field should be considered invalid and any reserved fields of the structure are reserved for future use.</li> </ul> <p>Note that PCIe devices without AER (PCIe_AER_INFO_STRUCT_VALID_BIT=0) may report status using this structure.</p>
CXL DVSEC Length	108	2	The length in bytes of the CXL DVSEC field
CXL Error Log Length	110	2	The length in bytes of the CXL Error Log field
Reserved	112	4	Must be zero
CXL DVSEC	116	Varies	<p>The length of this variable-length structure is defined by the CXL DVSEC Length field.</p> <p>If the CXL agent is a CXL 1.1 device, this field contains a copy of the CXL Device DVSEC, as defined by the "PCIe CXL DVSEC for Flex Bus Device" structure in the CXL 1.1 Specification.</p>

			<p>If the CXL agent is a CXL 1.1 host downstream port, this field contains a copy of the CXL Port DVSEC, as defined by the “CXL DVSEC for Flex Bus Port” structure in the CXL 1.1 Specification.</p>
CXL Error Log	Varies	Varies	<p>The length of this variable-length structure is defined by the CXL Error Log Length field.</p> <p>For CXL 1.1 devices and host downstream CXL ports, this field contains a copy of the “CXL RAS Capability Structure”, as defined in the CXL 1.1 Specification.</p>