 # Title:
MADT GICC new flags

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Draft

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ACPI 6.4 specification

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 # Submitters:

- James Morse, Lorenzo Pieralisi, Souvik Chakravarty, Thanu Rangarajan, Samer El-Haj-Mahmoud, Sudeep Holla (ARM)
- TianoCore Community (https://www.tianocore.org)

 # Summary of the change
Add new “Online capable” and “Not present” flags in the GICC MADT flags and clarify the usage relevant to the existing “Enabled” flag.

 # Benefits of the change

• On ARM systems physical CPU hotplug is not supported. All CPUs are considered present and this is true throughout the system uptime

• This ECR defines a new “not-present” bit to cater for future-proof CPU physical hotplug

• This ECR also defines a new “online-capable” flag: to signal firmware policy (CPU is not enabled but it can be enabled and onlined)

• MADT GICC entries that are !enabled+online-capable are not onlined at bootstrap by the OS but they are considered available cpus

• Standard ACPI GED notification mechanism to signal a cpu has been “enabled” at runtime (post-boot)

• GIC redistributor region for the disabled+online-capable cpu must be in the GICR (always-on power domain)

 # Impact of the change

- New flags allow OSPM to support virtual CPU hotplug
- Change is backwards compatible with existing OSPM / Software

 # Detailed description of the change [normative updates]

- Insertions in green
- Removals in ~~red~~

Table 5.37: GICC CPU Interface Flags

GIC Flags	Bit Length	Bit Offset	Description
Enabled	1	0	If this bit is set, the processor is ready for use. If ~~zero~~ this bit is clear and the Online Capable bit is also clear, this processor is unusable, and the operating system support will not attempt to use it. If this bit is clear when the Online Capable bit is set, the system supports enabling this processor later during OS runtime.
Performance Interrupt Mode	1	1	0 - Level-triggered | 1 - Edge-Triggered
VGIC Maintenance interrupt Mode Flags	1	2	0 - Level-triggered | 1 - Edge-Triggered
Online Capable	1	3	The information conveyed by this bit depends on the value of the Enabled bit. If the Enabled bit is set, this bit is reserved and must be zero. Otherwise, if this bit is set, the system supports enabling this processor later during OS runtime.
Not Present	1	4	If zero, this bit indicates that the processor is present. This bit must always be zero.
Reserved	~~29~~27	~~3~~5	Must be zero.