UEFI Forum Engineering Change Request (ECR)

# Title:

Add RISC-V INTC APIC Structures in MADT

# Status:

Draft

# Document:

ACPI Specification 6.5.next

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RISC-V Platform HSC (<https://lists.riscv.org/g/tech-unixplatformspec>)

# Summary of the change

This ECR introduces APIC structures for the RISC-V INTC Interrupt Controllers in the MADT.

# Benefits of the Change

This change enables the RISC-V platforms to boot with ACPI support.

# Impact of Change

This change will impact RISC-V firmware, different Operating Systems for RISC-V architecture and also emulation platforms.

# Detailed Description of the Change

Changes in **yellow**

Insertions in **green**

Removals in **~~red~~**

Table 5-21 **Interrupt Controller Structure Types**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Value | Description | \_MAT for Processor object | \_MAT for an I/O APIC object | Reference |
| 0x16 | Bridge I/O Programmable Interrupt Controller (BIO PIC) | no | no | Section 5.2.12.25 |
| 0x17 | Low Pin Count Programmable Interrupt Controller (LPC PIC) | no | no | Section 5.2.12.26 |
| 0x18 | RISC-V Hart Local Interrupt Controller (RINTC) | yes | no | Section 5.2.12.27 |
| 0x19-0x7F | Reserved. OSPM skips structures of the reserved type. | no | no |  |
| 0x80-0xFF | Reserved for OEM use | no | no |  |

**5.2.12.27 RISC-V Interrupt Controller (RINTC) Structure**

The RISC-V platforms need to have a simple, per-hart (hardware thread or logical processor) interrupt controller available to supervisor mode.

For RISC-V platforms, the “Local Interrupt Controller Address” field in the MADT must be ignored by the OSPM.

Table 5.53: **RISC-V Interrupt Controller(RINTC) Structure**

|  |  |  |  |
| --- | --- | --- | --- |
| **Field** | **Byte Length** | **Byte Offset** | **Description** |
| - Type | 1 | 0 | 0x18 RISC-V INTC structure |
| - Length | 1 | 1 | 20 - Length in bytes for this RINTC structure |
| - Version | 1 | 2 | For this version of the specification, the revision is 1. |
| - Reserved | 1 | 3 | Must be zero |
| - Flags | 4 | 4 | See RISC-V INTC Flags |
| - Hart ID of the hart | 8 | 8 | Hart ID (mhartid) of the hart this interrupt controller belongs to. |
| - ACPI Processor UID | 4 | 16 | The OS associates this RINTC structure with a processor device object in the namespace when the \_UID child object of the processor device evaluates to a numeric value that matches the numeric value in this field. |

Table 5.54: **RISC-V INTC Flags**

|  |  |  |  |
| --- | --- | --- | --- |
| **RINTC Flags** | **Bit Length** | **Bit Offset** | **Description** |
| - Enabled | 1 | 0 | If this bit is set the processor is ready for use. If this bit is clear and the Online Capable bit is set, system hardware supports enabling this processor during OS runtime. If this bit is clear and the Online Capable bit is also clear, this processor is unusable, and OSPM shall ignore the contents of the RINTC structure. |
| - Online Capable | 1 | 1 | The information conveyed by this bit depends on the value of the Enabled bit. If the Enabled bit is set, this bit is reserved and must be zero. Otherwise, if this bit is set, system hardware supports enabling this processor during OS runtime. |
| - Reserved | 30 | 2 | Must be zero |