**# Title:**

FEAT\_D128 core registers CPER table

**# Status:**

Draft

**# Document:**

UEFI Specification 2.10

**# License:**

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**# Submitter:**

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**# Summary of the change**

- Add the FEAT\_D128 128-bit TTBR registers as a new register table (type 9)

**# Benefits of the change**

Allows CPER records to represent TTBR registers on machines with FEAT\_D128.

**# Impact of the change**

CPER consumers executing on platforms supporting FEAT\_D128 should integrate the knowledge of this new CPER table.

**# Detailed description of the change [normative updates]**

* Insertions highlighted
* Removals in ~~red~~

#### N.2.4.4. ARM Processor Error Section

**…**

##### N.2.4.4.2. ARM Processor Context Information

**…**

*Table N.31 ARM 128 bit translation table base registers (Type 9)*

|  |  |  |
| --- | --- | --- |
| **Byte Offset** | **Byte Length** | **Field** |
| 0 | 16 | TTBR0\_EL1 |
| 16 | 16 | TTBR0\_EL2 |
| 32 | 16 | TTBR0\_EL3 |
| 48 | 16 | TTBR1\_EL1 |
| 64 | 16 | TTBR1\_EL2 |
| 80 | 16 | VTTBR\_EL2 |

When table N.31 is present, some of its registers may be invalid.

An invalid register in table N.31 must have all 128 bits set.