**Title:**

CPU hot-plug clarifications for Arm based systems (\_STA and MADT).

**# Status:**

Draft

**# Document:**

ACPI Specification 6.next

**# License:**

SPDX-License-Identifier: CC-BY-4.0

**# Submitter:**

* Arm
* TianoCore Community (<https://www.tianocore.org>)

**# Summary of the change**

Clarify that, on Arm, the \_STA.presence (bit[0]) cannot toggle at runtime.

**# Benefits of the change**  
Provide clarity to OSs on the processor status and its consequence on processor hot-plug capabilities.

**# Impact of the change**Codebases are not impacted.

**# Detailed description of the change [normative updates]**

* Insertions highlighted
* Removals in ~~red~~
* Cross-reference highlighted

#### 5.2.12.14. GIC CPU Interface (GICC) Structure

…

|  |  |  |  |
| --- | --- | --- | --- |
| *Table 5.37****GICC CPU Interface Flags*** | | | |
| **GIC Flags** | **Bit Length** | **Bit Offset** | **Description** |
| Enabled | 1 | 0 | If this bit is set, the processor is ready for use. If this bit is clear and the Online Capable bit is set, the system supports enabling this processor during OS runtime. If this bit is clear and the Online Capable bit is also clear, this processor is unusable, and the operating system support will not attempt to use it. |
| Performance Interrupt Mode | 1 | 1 | 0 - Level-triggered | 1 - Edge-Triggered |
| VGIC Maintenance Interrupt Mode Flags | 1 | 2 | 0 - Level-triggered | 1 - Edge-Triggered |
| Online Capable | 1 | 3 | The information conveyed by this bit depends on the value of the Enabled bit. If the Enabled bit is set, this bit is reserved and must be zero. Otherwise, if this bit is set, the system supports enabling this processor later during OS runtime. |
| *Reserved* | 28 | 4 | Must be zero. |

**Note**

All processors are assumed to be always physically present

**Note**

On Arm systems, Bit[0] of the \_STA object for a processor device must not change at runtime, irrespective of the Enabled and Online Capable bits in the MADT entry (Table 5.37) corresponding to that processor.

This means that a processor whose \_STA bit[0] is 0 cannot have that bit set to 1 during runtime. Similarly, a processor whose \_STA Bit[0] is set to 1 cannot have that bit cleared at runtime.