**# Title:**

FPDT generic Host firmware and microcontroller boot performance records.

**# Status:**

Draft

**# Document:**

ACPI Specification 6.next

**# License:**

SPDX-License-Identifier: CC-BY-4.0

**# Submitter:**

* Ampere (Rob Gough, Harb Abdulhamid)
* Arm (Jose Marinho)
* TianoCore Community (<https://www.tianocore.org>)

**# Summary of the change**

Define the performance records for Generic Host firmware components and microcontrollers.

**# Benefits of the change**  
Enable Platform Firmware to represent the boot performance of different Host firmware components – allows for finer granularity of the Host boot performance characterization.

Enable microcontroller boot performance to be presented in a standard manner.

**# Impact of the change**For systems that implement the FPDT table, the boot firmware must record the system counter at the required events (for the present firmware stages) and handoff the information along the boot path.

Knowledge of the new tables must be added to an OS that intends to consume the new performance records.

**# Opens**  
- For platforms where the memory init is done by a microcontroller (instead of the Host) should the memory sub-system init (Table 5.120) have a reference to the microcontroller that does the init (Table 5.117)?

**# Detailed description of the change [normative updates]**

* Insertions highlighted
* Removals in ~~red~~
* New cross-reference in purple

#### 5.2.24.3. Runtime Performance Record Types

The table below describes the various Runtime Performance records and their corresponding Record Types. These records are not contained within the FPDT; they are referenced by their respective pointer records in the FPDT.

|  |  |  |
| --- | --- | --- |
| *Table 5.109****Runtime Performance Record Types*** | | |
| **Record Type Value** | **Type** | **Description** |
| 0x0000 | Basic S3 Resume Performance Record | Performance record describing minimal firmware performance metrics for S3 resume operations. |
| 0x0001 | Basic S3 Suspend Performance Record | Performance record describing minimal firmware performance metrics for S3 suspend operations. |
| 0x0002 | Firmware Basic Boot Performance Data Record | Performance record showing basic performance metrics for critical phases of the firmware boot process. |
| 0x0003 | Microcontroller Boot Performance Data Record | Boot performance record for a microcontroller (Table 5.117). All timestamps in this record type are in the respective microcontroller time axis. |
| 0x0004 | Host Firmware Component Boot Performance Data Record | Boot performance record of a Host firmware component (Table 5.119). |
| 0x0005 | Memory Sub-system Boot Performance Data Record | Performance record of the memory sub-system initialization, during platform boot (Table 5.120). |
| 0x000~~3~~6 - 0x0FFF | Reserved | Reserved for ACPI specification usage. |
| 0x1000 - 0x1FFF | Reserved | Reserved for Platform Vendor usage. |
| 0x2000 - 0x2FFF | Reserved | Reserved for Hardware Vendor usage. |
| 0x3000 - 0x3FFF | Reserved | Reserved for platform firmware Vendor usage. |
| 0x~~4~~000 - 0xFFFF | Reserved | Reserved for future use |

…

#### Microcontroller Boot Performance Data Record

Microcontroller

start

Microcontroller

time axis

Host

start

0

Host

time axis

Time delta

0

t'

t

Table 5.117 contains an array of timestamped events for a microcontroller.  
The timestamps, on this table, are in the microcontroller time axis.  
On some platforms, the time axis of each microcontroller differs from that of the Host.  
The *time delta* field, in Table 5.117, is a signed integer representing the offset between the microcontroller and Host time axis. A positive *time delta* means the clock of the microcontroller started ticking after the Host clock.

*Table 5.117* Microcontroller Boot Performance Data Record

|  |  |  |  |
| --- | --- | --- | --- |
| **Field** | **Byte Length** | **Byte Offset** | **Description** |
| Performance Record Type | 2 | 0 | 0x0003 – Microcontroller Boot Performance Data Record. Multiple records of this type can exist. |
| Revision | 1 | 2 | 1 - Revision of this Performance Record |
| Reserved | 1 | 3 | Reserved |
| Record size | 4 | 4 | The size, in bytes, of the complete record. Encompasses this header and the complete Microcontroller event array. |
| Number of microcontroller events (N) | 2 | 8 | The number of entries on the Microcontroller array. |
| Reserved | 6 | 10 | Reserved |
| Microcontroller identifier. | 8 | 16 | An 8-character string identifying the microcontroller. |
| Time delta | 8 | 24 | Signed integer, the offset (ns) between this microcontroller and the Host time axis. |
| Microcontroller event array[N] | -- | 32 | An Array of microcontroller timestamped event entries (Table 5.118) |

Table 5.118: Microcontroller timestamped event.

|  |  |  |  |
| --- | --- | --- | --- |
| **Field** | **Byte Length** | **Byte Offset** | **Description** |
| Event ID | 2 | 0 | The ID of the timestamped event. The event ID is microcontroller-specific. |
| Reserved | 6 | 2 | Reserved |
| timestamp | 8 | 8 | The time (ns) elapsed this microcontroller started execution. |

**…**

#### 5.2.24.10. Host Firmware Component Boot Performance Data Record

The Host Firmware Component Boot Performance Data Record (Table 5.119) contains the boot timestamps of a Host firmware component.  
Table 5.119 complements the “Firmware Basic Boot Performance Data Record” (Table 5.113).

**Note:** on Arm, the field *Reset End* in Table 5.113 contains the timestamp at which the Non-secure firmware started to execute.

|  |  |  |  |
| --- | --- | --- | --- |
| *Table 5.119 Host Firmware Component Boot Performance Data Record* | | | |
| **Field** | **Byte Length** | **Byte Offset** | **Description** |
| Performance Record Type | 2 | 0 | 0x0004 – Host Firmware Component Boot Performance Data Record. Multiple records of this type can exist. |
| Revision | 1 | 2 | 1 - Revision of this Performance Record |
| Reserved | 1 | 3 | Reserved |
| Record Length | 4 | 4 | The length of this data record, in bytes. |
| Component identifier. | 8 | 0 | An 8-character string identifying the Host Firmware Component. |
| Component boot start | 8 | 8 | The time (ns) when the firmware component starts to boot on the Host. |
| Component boot finish | 8 | 16 | The time (ns) when the firmware component finishes to boot on the Host. |

#### 5.2.24.11. Memory Sub-system Boot Performance Data Record

During platform boot the memory sub-system is initialized. The timestamps of the start and finish of the memory initialization process are representable by the Memory Sub-system Boot Performance Data Record (Table 5.120).

Table 5.120 Memory Sub-system Boot Performance Data Record

|  |  |  |  |
| --- | --- | --- | --- |
| **Field** | **Byte Length** | **Byte Offset** | **Description** |
| Performance Record Type | 2 | 0 | 0x0005 – Memory Sub-system Boot Performance Data Record. At most one of these records will be produced. |
| Revision | 1 | 2 | 1 - Revision of this Performance Record |
| Reserved | 1 | 3 | Reserved |
| Record Length | 4 | 4 | The length of this data record, in bytes. |
| Memory sub-system initialization start | 8 | 8 | The time (ns) when the memory sub-system initialization started. |
| Memory sub-system initialization finish | 8 | 16 | The time (ns) when the memory sub-system initialization completed. |