Unified Extensible Firmware Interface  
Engineering Change Request (ECR)

*Draft for Review*

Title: CPER Definition for CXL RCH

Document: UEFI v2.10

Sponsors:

*Leo Duran (AMD)*

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Verifiers: *Leo Duran (AMD)*

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CPER Definition for CXL RCH

### **# Status:**

Draft

### **# Document:**

UEFI Specification Version 2.10

### **# Submitter:**

Leo Duran (AMD)

### **# Summary of the change**

This ECR addresses a gap in a CPER definition to allow CXL.io errors reported by a CXL RCH (Downstream port) via AER.

### **# Problem Statement**

The standard PCIe CPER definition only allows for a BDF address, whereas a CXL RCH is MMIO-based.

### **# Proposed Solution**

Amend the standard PCIe CPER definition to include the MMIO base address of a Root Complex Register Block (RCRB), as in the case of a CXL RCH.

### **# Benefits of the change**

Enables Firmware-First support of CXL.io errors reported by a CXL RCH (Downstream port) via AER.

### **# Impact of the change**

Would require platform firmware and OSPM changes to support the proposed CPER definition.

**Format for Markups:**

Entries may include “**…**” to indicate unchanged text.

inserted text

~~deleted text~~

**N.2.7 PCI Express Error Section**

Type: {0xD995E954, 0xBBC1, 0x430F, {0xAD, 0x91, 0xB4, 0x4D, 0xCB, 0x3C, 0x6F, 0x35}}

**Table N.33: PCI Express Error Record**

|  |  |  |  |
| --- | --- | --- | --- |
| **Mnemonic** | **Byte Offset** | **Byte Length** | **Description** |
| Validation Bits | 0 | 8 | Indicates which of the following fields is valid:  Bit 0 - Port Type Valid  Bit 1 - Version Valid  Bit 2 - Command Status Valid  Bit 3 - Device ID Valid (PCI Config-Space)  Bit 4 - Device Serial Number Valid  Bit 5 - Bridge Control Status Valid  Bit 6 - Capability Structure Status Valid  Bit 7 - AER Info Valid  Bit 8 - Device ID Valid (RCRB).  NOTE: If this bit is set, then Bit 3 must be 0.  Bit 9 - RCRB High Address Valid  NOTE: If this bit is 0, the RCRB High Address is assumed to be 0.  Bit ~~8~~10-63 – Reserved |
| ~~Reserved~~ RCRB High Address | 20 | 4 | ~~Must be zero~~ Upper DW of the MMIO base address for the RCRB. |
| Device ID | 24 | 16 | PCIe Root Port PCI/bridge PCI compatible device number and bus  number information to uniquely identify the root port or bridge.  Default values for both the bus numbers is zero.  Byte 0-1: Vendor ID  Byte 2-3: Device ID  Byte 4-6: Class Code  ~~Byte 7: Function Number~~  ~~Byte 8: Device Number~~  ~~Byte 9-10: Segment Number~~  If Bit 3 is set in Validation Bits:   * Byte 7: Function Number * Byte 8: Device Number * Byte 9-10: Segment Number   Else if Bit 8 is set in Validation Bits:   * Byte 7-10: Lower DW of the MMIO base address for the RCRB.   Byte 11: Root Port/Bridge Primary Bus Number or device bus number  Byte 12: Root Port/Bridge Secondary Bus Number  Byte 13-14: Bit0:2: Reserved Bit3:15 Slot Number  Byte 15 Reserved |
| **…** | **…** | **…** | **…** |