Unified Extensible Firmware Interface  
Engineering Change Request (ECR)

*Draft for Review*

Title: CPER Definition for CXL RCH DP Port

Document: UEFI v2.10

Sponsors:

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Verifiers: *Leo Duran (AMD)*

### **# Title:**

CPER Definition for CXL RCH

### **# Status:**

Draft

### **# Document:**

UEFI Specification Version 2.10

### **# Submitter:**

Leo Duran (AMD)

### **# Summary of the change**

This ECR addresses a gap in a CPER definition to allow CXL.io errors reported by a CXL RCH Downstream Port (RCH-DP) via AER. It also provides some language clean-ups in the CPER definition for CXL Protocol errors.

### **# Problem Statement**

The standard PCIe CPER definition only allows for a BDF address, whereas a CXL RCH-DP is MMIO-based.

### **# Proposed Solution**

Amend the standard PCIe CPER definition to include the MMIO base address of a Root Complex Register Block (RCRB), as in the case of a CXL RCH-DP.

### **# Benefits of the change**

Enables Firmware-First support of CXL.io errors reported by a CXL RCH-DP via AER.

### **# Impact of the change**

Would require platform firmware and OSPM changes to support the proposed CPER definition.

**Format for Markups:**

Entries may include “**…**” to indicate unchanged text.

inserted text

~~deleted text~~

**N.2.7 PCI Express Error Section**

Type: {0xD995E954, 0xBBC1, 0x430F, {0xAD, 0x91, 0xB4, 0x4D, 0xCB, 0x3C, 0x6F, 0x35}}

**Table N.33: PCI Express Error Record**

|  |  |  |  |
| --- | --- | --- | --- |
| **Mnemonic** | **Byte Offset** | **Byte Length** | **Description** |
| Validation Bits | 0 | 8 | Indicates which of the following fields is valid:  Bit 0 - Port Type Valid  Bit 1 - Version Valid  Bit 2 - Command Status Valid  Bit 3 - Device ID Valid (PCI Config-Space)  Bit 4 - Device Serial Number Valid  Bit 5 - Bridge Control Status Valid  Bit 6 - Capability Structure Status Valid  Bit 7 - AER Info Valid  Bit 8 - Device ID Valid (RCRB).  NOTE: If this bit is set, then Bit 3 must be 0.  Bit 9 - RCRB High Address Valid  NOTE: If this bit is 0, the RCRB High Address is assumed to be 0.  Bit ~~8~~10-63 – Reserved |
| Port Type | 8 | 5 | **…**  4: Root Port ~~5: Upstream Switch Port~~  5: Upstream Switch Port  **…** |
| **…** | **…** | **…** | **…** |
| ~~Reserved~~ RCRB High Address | 20 | 4 | ~~Must be zero~~ Upper DW of the MMIO base address for the RCRB. |
| Device ID | 24 | 16 | PCIe Root Port PCI/bridge PCI compatible device number and bus  number information to uniquely identify the root port or bridge.  Default values for both the bus numbers is zero.  Byte 0-1: Vendor ID  Byte 2-3: Device ID  Byte 4-6: Class Code  ~~Byte 7: Function Number~~  ~~Byte 8: Device Number~~  ~~Byte 9-10: Segment Number~~  If Bit 3 is set in Validation Bits:   * Byte 7: Function Number * Byte 8: Device Number * Byte 9-10: Segment Number   Else if Bit 8 is set in Validation Bits:   * Byte 7-10: Lower DW of the MMIO base address for the RCRB.   Byte 11: Root Port/Bridge Primary Bus Number or device bus number  Byte 12: Root Port/Bridge Secondary Bus Number  Byte 13-14: Bit0:2: Reserved Bit3:15 Slot Number  Byte 15 Reserved |
| **…** | **…** | **…** | **…** |

**N.2.13 Compute Express Link (CXL) Protocol Error Section**

Type: { 0x80B9EFB4, 0x52B5, 0x4DE3, { 0xA7, 0x77, 0x68, 0x78, 0x4B, 0x77, 0x10, 0x48 } }

**Table N.41: CXL Protocol Error Section**

|  |  |  |  |
| --- | --- | --- | --- |
| **Mnemonic** | **Byte Offset** | **Byte Length** | **Description** |
| CXL Agent Type | 8 | 1 | 0 - This error was detected by a CXL ~~1.1 device~~ RCD RCIeP  1 - This error was detected by a CXL ~~1.1 host~~ RCH ~~d~~Downstream ~~p~~Port RCRB  2 - This error was detected by a CXL ~~2.0~~  Endpoint ~~d~~Device  3 - This error was detected by a CXL ~~2.0~~ Logical Device  4 - This error was detected by a CXL ~~2.0~~ Fabric Manager managed Logical ~~d~~Device  5 - This error was detected by a CXL ~~2.0~~ Root Port  6 - This error was detected by a CXL ~~2.0~~ Downstream Switch Port  7 - This error was detected by a CXL ~~2.0~~ Upstream Switch Port  8-255 – Reserved  In this table, the term “CXL Device” is used to refer to a CXL ~~1.1 Device~~ RCD RCiEP, CXL ~~2.0~~ Endpoint Device, CXL ~~2.0~~ Logical Device or a CXL ~~2.0~~ Fabric Manager ~~M~~managed Logical Device.  In this table, the term “CXL Port” is used to refer to a CXL ~~1.1 host~~ RCH ~~d~~Downstream ~~p~~Port RCRB, CXL Root Port, CXL Downstream Switch Port and Upstream Switch Port. |
| Reserved | 9 | 7 | Must be zero |
| CXL Agent Address | 16 | 8 | If this CXL agent is a CXL RCD RCiEP, CXL Endpoint ~~d~~Device, CXL Root Port, CXL  Downstream Switch Port or CXL Upstream Switch Port, then the PCIe compatible device/function number, bus number, and segment number information are used to uniquely identify the Component:  Byte 0 - Function number  Byte 1 - Device number  Byte 2 - Bus number  Bytes 3-4 - Segment number  Bytes 5-7 – Reserved  If CXL agent is a CXL  ~~1.1 host~~ RCH ~~d~~Downstream ~~p~~Port RCRB:  Byte 0-7 - CXL Port RCRB Base address |