**# Title:**

MADT GICC new flags

**# Status:**

Draft

**# Document:**

ACPI 6.4 specification

**# License:**

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**# Summary of the change**

This ECR proposes adding a new “Online capable” flag in the GICC CPU Interface Flags structure in MADT and clarify the usage relevant to the existing “Enabled” flag.

**# Benefits of the change**

• On ARM systems physical CPU hotplug is not supported. All CPUs are considered present and this is true throughout the system uptime.

• This ECR defines a new “online-capable” flag: to signal firmware policy (CPU is not enabled but it can be enabled and onlined)

• This enables OSPM to support virtual CPU hotplug (on virtual platforms for instance).

• MADT GICC entries that are !enabled+online-capable are not onlined at bootstrap by the OS but they are considered available CPUs

• Standard ACPI GED notification mechanism to signal a cpu has been “enabled” at runtime (post-boot)

• GIC redistributor region for the disabled+online-capable cpu must be in the GICR (always-on power domain)

**# Impact of the change**

* New flags allow OSPM to support virtual CPU hotplug
* Change is backwards compatible with existing OSPM / Software

**# Detailed description of the change [normative updates]**

* Insertions in green
* Removals in ~~red~~

Table 5-19 Multiple APIC Description Table (MADT) Format

|  |  |  |  |
| --- | --- | --- | --- |
| **Field** | **Byte Length** | **Byte Offset** | **Description** |
| Header |  |  |  |
| … | … | … | … |
| Revision | 1 | 8 | ~~5~~6 |
| … | … | ... | … |

**Table 5.37: GICC CPU Interface Flags**

|  |  |  |  |
| --- | --- | --- | --- |
| **GIC Flags** | **Bit**  **Length** | **Bit Offset** | **Description** |
| Enabled | 1 | 0 | If this bit is set, the processor is ready for use. If this bit is clear and the Online Capable bit is set, the system supports enabling this processor during OS runtime. If ~~zero~~ this bit is clear and the Online Capable bit is also clear, this processor is unusable, and the operating system support will not attempt to use it. |
| Performance Interrupt  Mode | 1 | 1 | 0 - Level-triggered | 1 - Edge-Triggered |
| VGIC Maintenance interrupt  Mode Flags | 1 | 2 | 0 - Level-triggered | 1 - Edge-Triggered |
| Online Capable | 1 | 3 | The information conveyed by this bit depends on the value of the Enabled bit. If the Enabled bit is set, this bit is reserved and must be zero. Otherwise, if this bit is set, the system supports enabling this processor later during OS runtime. |
| Reserved | ~~29~~28 | ~~3~~4 | Must be zero. |

**Note**: All processors are assumed to be always physically present