# # Title:

Armv9 TRBE support

# # Status:

Draft

# # Document:

ACPI Specification Version 6.*next*

# # License:

SPDX-License-Identifier: CC-BY-4.0

# # Submitter:

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# # Summary of the change

This ECR is related to a proposal to update the current GIC CPU (GICC) structure in the MADT to describe the Armv9 Trace Buffer Extension (TRBE) feature. TRBE uses a platform-specific interrupt to signal events. The interrupt is a Processor Private interrupt (PPI).

# # Benefits of the change

Enables support for Armv9 extensions on Arm systems.

# # Impact of the change

Platforms firmware will have to support publishing the TRBE GSIV based on the updated GIC CPU structure, and OS’s (or OS drivers) will similarly need changes to comprehend and support the new GIC CPU format. These are both fundamentally new code.

# # Detailed description of the change [normative updates]

Existing text

New text

~~Deleted text~~

**5.x.x Multiple APIC Description Table (MADT)**

…

**5.x.x.y GIC CPU Interface (GICC) Structure**

…

**Table 5.z GICC Structure**

|  |  |  |  |
| --- | --- | --- | --- |
| **Field** | **Byte Length** | **Byte Offset** | **Description** |
| … | … | … | … |
| SPE overflow interrupt | 2 | 78 | … |
| TRBE Interrupt | 2 | 80 | Trace Buffer Extension interrupt GSIV. This interrupt  is a level triggered PPI. Zero if TRBE feature is not supported  by this processor. |