Name: Teng Tian
Gender: Male
Data of Birth: 27 MAY 1995
Place of Birth: Anhui, China
Mobile Phone: (+86) 133 3926 5658
E-mail: tianteng@mail.ustc.edu.cn

Education

AUG, 2018 - NOW

- University of Science and Technology of China
- Ph.D. Candidate Microelectronics
- Research Focus: Computer Architecture, High Performance Computing

AUG, 2016 - JUN, 2018

- University of Science and Technology of China
- Master Candidate Microelectronics
- Research Focus: Computer Architecture, High Performance Computing
- Score Point Average: 91.44/100

AUG, 2012 - JUN, 2016

- University of Science and Technology of China
- B.S. Applied Physics
- GPA: 3.58/4.3 (Score Point Average: 86.33/100)

Honors and Awards

- 2018 -- 2019 Second-class Graduate School Scholarship
- 2017 -- 2018 First-class Graduate School Scholarship
- 2017 Hua Wei Scholarship
- 2016 -- 2017 First-class Graduate School Scholarship

Publications

- **Tian, T**., Wang, T., & Jin, X. (2017, December). An Efficient Hardware Prefetcher Exploiting the Prefetch Potential of Long-Stride Access Pattern on Virtual Address. In 2017 IEEE International Symposium on Parallel and Distributed Processing with Applications (ISPA) (pp. 48-57). IEEE.
- Guo, S., Wang, T., Tao, L., **Tian, T**., Xiang, Z., & Jin, X. (2018). RP-Ring: A Heterogeneous Multi-FPGA Accelerator. International Journal of Reconfigurable Computing, 2018.
- Xu, R., Jin, X., Tao, L., Guo, S., Xiang, Z., & **Tian, T**. (2018, March). An efficient resource-optimized learning prefetcher for solid state drives. In 2018 Design, Automation & Test in Europe Conference & Exhibition (DATE) (pp. 273-276). IEEE.

TOEFL iBT Scores

- Total Score: 92
- Reading: 28 Listening: 25 Speaking: 19 Writing: 20

GRE Scores

- Verbal: 152 Quantitative: 166 Writing: 2.5

Project Experience

- I have participated in Huawei Innovation Research Program (YB2015090102) researching the linear scalability of multicore/multiprocessor system. Generally, the performance increment is not proportional to the number of cores due to the resource sharing and contention. Our work is studying how the performance increases with the number of ARMv8 cores and

optimizing the cache configuration and the interconnection network to reduce the loss of linearity. During the project period, we built an ARMv8 multicore system with customized cache hierarchy and prefetch mechanism using Gem5 simulator, and evaluated SPEC jbb & SPEC CPU benchmarks on modified hardware platforms. We have submitted a patent of invention about a dynamic reconfigurable last level cache scheduling method, and I have published a long paper on hardware prefetcher design in 2017 IEEE International Symposium on Parallel and Distributed Processing with Applications (ISPA).

- I have experience in Verilog coding and FPGA development. I have built a scalable parallel Particle-Particle(PP) accelerator accelerating N-Body simulation, and PP is one of the N-body simulation methods with $O(N^2)$ algorithm complexity. By utilizing a dedicated pipeline structure and optimizing resource utilization, the PP accelerator can implement 20 pipelines on Xilinx KC705 evaluation board and achieves more than 55x speedups compared to Intel Xeon E5 2620v4 CPU. I've also built a A-star search accelerator on KC705 evaluation board recently, and evaluated it with a pathfinding application on a large map which is 1000x1000. The result shows that A-star search accelerator achieves 153x speedups compared to software implementation running on Intel Core i5-6300HQ CPU.
- My current work is building reconfigurable and scalable deep neural network accelerator with hardware-software co-design. During this project, many compressing method, such as quantization and sparsification, and novel hardware architecture like CGRA will be exploited to address the computing and communicating problems caused by large scale neural networks.