

module block\_nonblock(Clk, Rst, a, b, c, out);

    input Clk;

    input Rst;

    input a, b, c;

    output reg [1:0] out;

    // out = a + b + c;

    // d = a + b

    // out = d + c

    reg [1:0]   d;

    always@(posedge Clk or negedge Rst)

    if(!Rst)

        out = 2'b0;

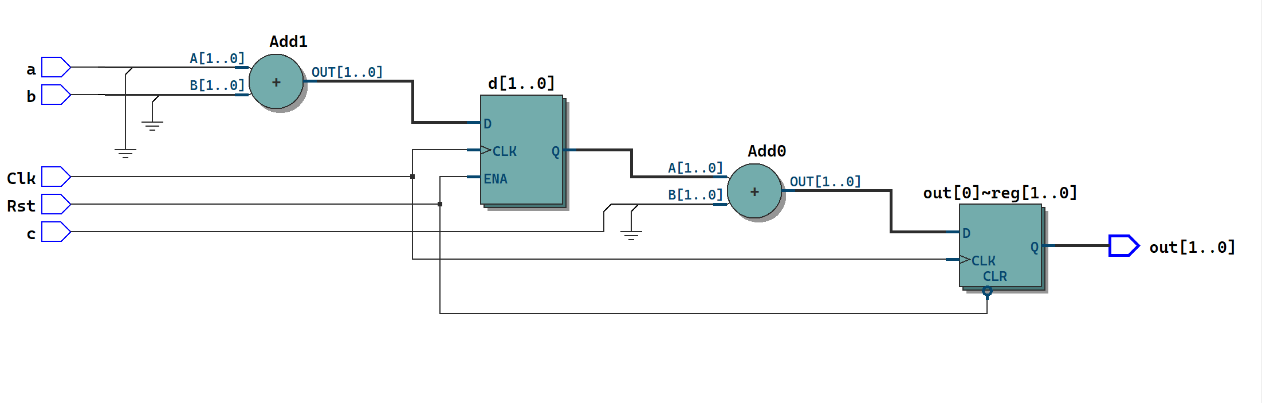
    else begin

        d = a + b;

        out = d + c;

    end

endmodule



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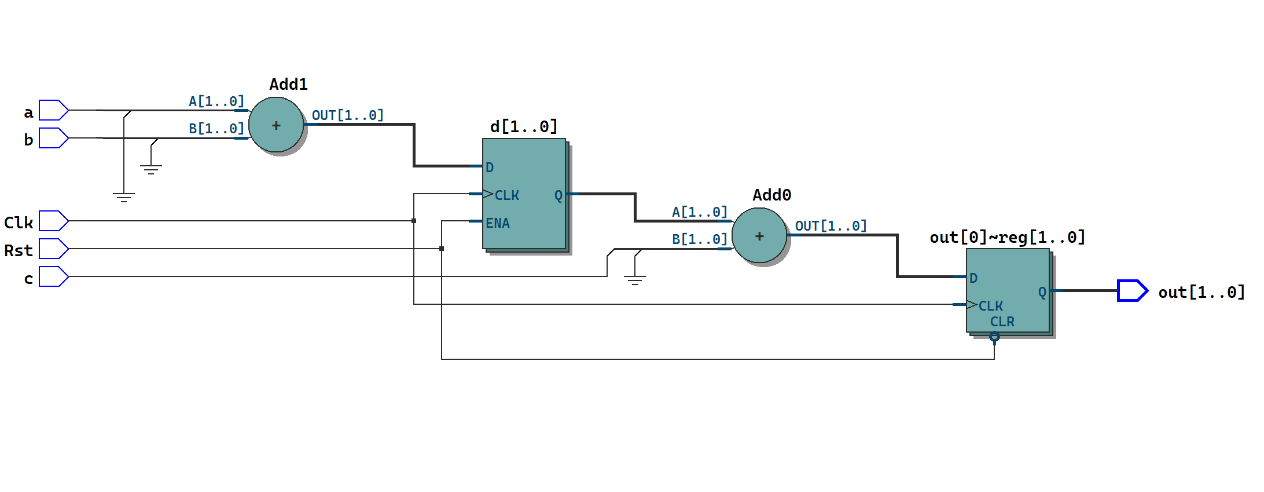
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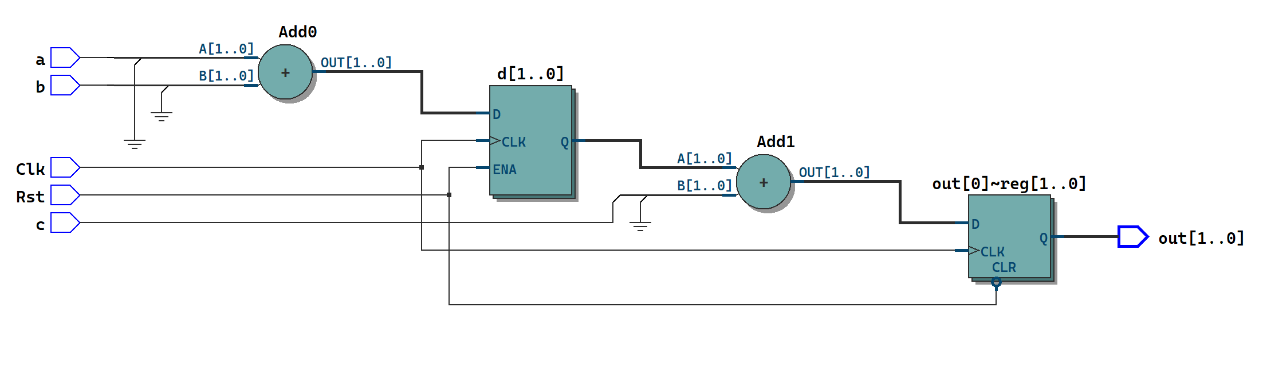
    else begin

        out <= d + c;

        d <= a + b;

    end

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    else begin

        d <= a + b;

        out <= d + c;

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阻塞赋值会以时钟为基准，在时钟信号到来时才会获取输入并输出结果。