Technical innovation in designing next generation PCIe Gen5 Client SSD

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Background

- PCIe Gen.4 SSD overwhelm PC OEM SSD very soon when it was introduced. We believe Gen.5 SSD will follow the same path.
- Pursuit of storage bandwidth never cease. In current platform, storage continue to play important roles such as fast data accessing, serving as DRAM cache, “Direct Storage API”, etc… All these applications need high performance SSDs

SiliconMotion SMI 1st PCIe Gen5 Client SSD Ctrl.

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- High Performance
  - Sequential read can saturate PCIe Gen5x4 bandwidth, up to 15GB/s
  - Random read/write up to 2.5M IOPS
- Low power consumption
  - 3.5W (Max.) in Active mode
  - 2.5mW in PS4 state
- Flexible peripheral interface
  - Platform resilience support
  - Upgradable design

Performance excellence

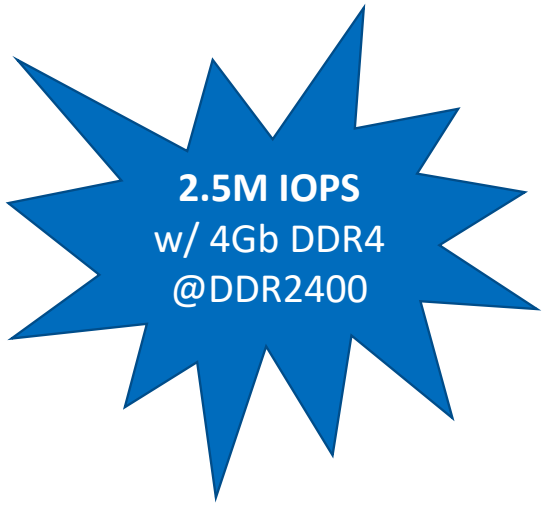
- SM2508 use quad core Cortex-R8 CPU which is capable of higher speed and efficiency
- SMP (Symmetric Multi-Processing) enables automatic load balancing across multi-cores, the architecture is optimal for handling mixed workloads.
- SMP simplifies the code maintenance and make the transfer to the next designs easier. In contrast, the dedicated acceleration HW are hard for code debugging and no portability

Feature	Cortex-R8
Instruction Set Architecture	Armv7-R
Pipeline Depth	11 stage out-of-order, superscalar
Symmetric Multi-Processing (SMP)	SMP support, up to Qual-core
Dhrystone Benchmark MIPS/MHz	2.5 DMIPS/MHz
CoreMark®/ MHz*	4.62

DRAM cache cost reduction

- DRAM is used to store the mapping table and cache data, so the bandwidth of DRAM on SSD is crucial to SSD performance
- SM2508 enhance DRAM controller design to reduce the DRAM interface latency and thus reduce the need of high bandwidth DRAM
- The improvement enables SM2508 to achieve peak performance with low-cost DRAM and reduces total BOM cost

Items	Spec
DRAM Device	DDR4 or LPDDR4
Bit width	X16 or X32
Speed grade	DDR2400 or higher
Density (DRAM/NAND)	1/1000 or 1/2000 or 1/4000 …



SiliconMotion Performance-power balance arch.

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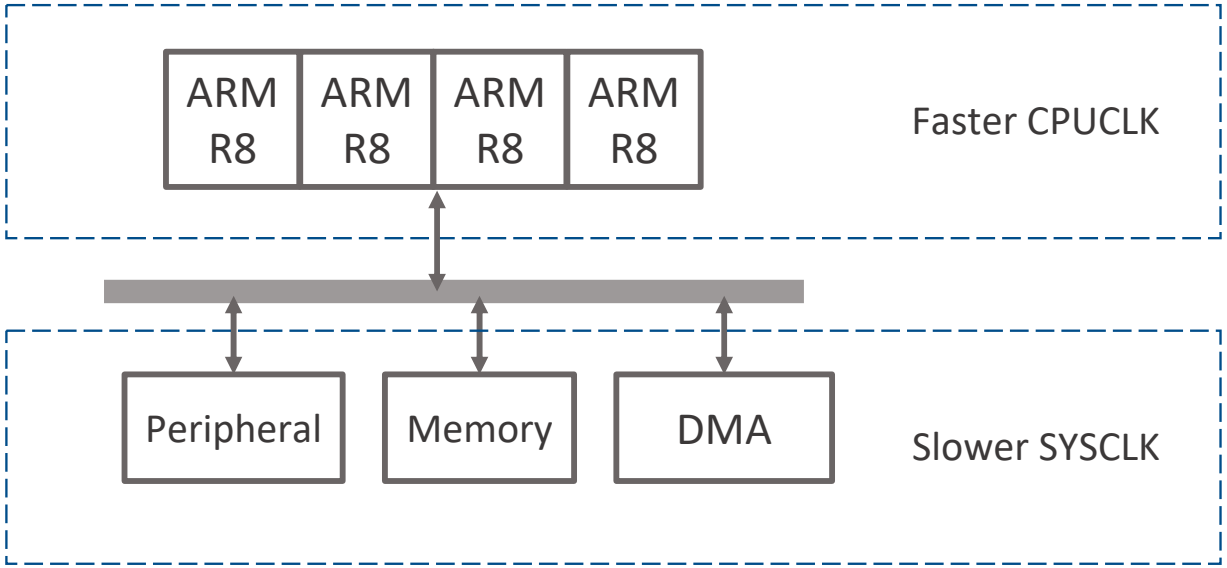
- SM2508 use an asynchronous architecture for CPU and the system bus
- Maximize CPUCLK to execute instructions faster, lower down SYSCLK to achieve low power
- Overall performance efficiency (GB/s per Watt) is improved by the new architecture



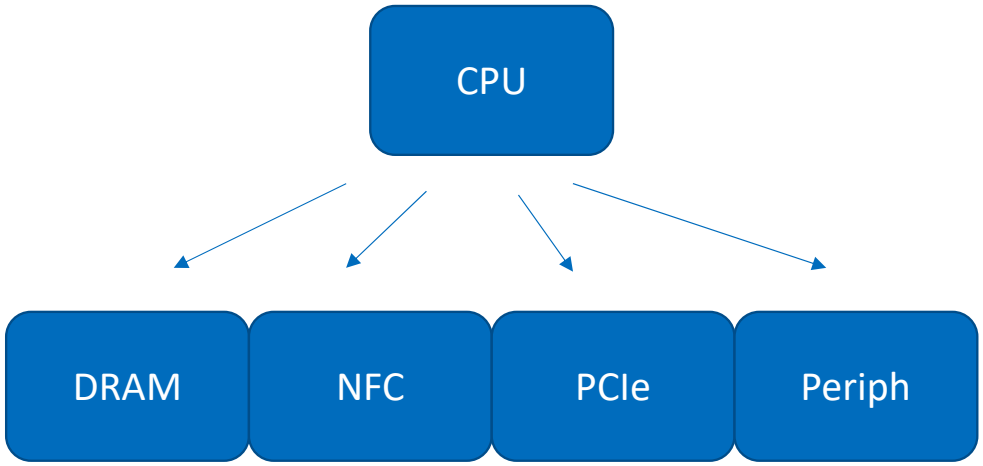
Best-in-class power consumption

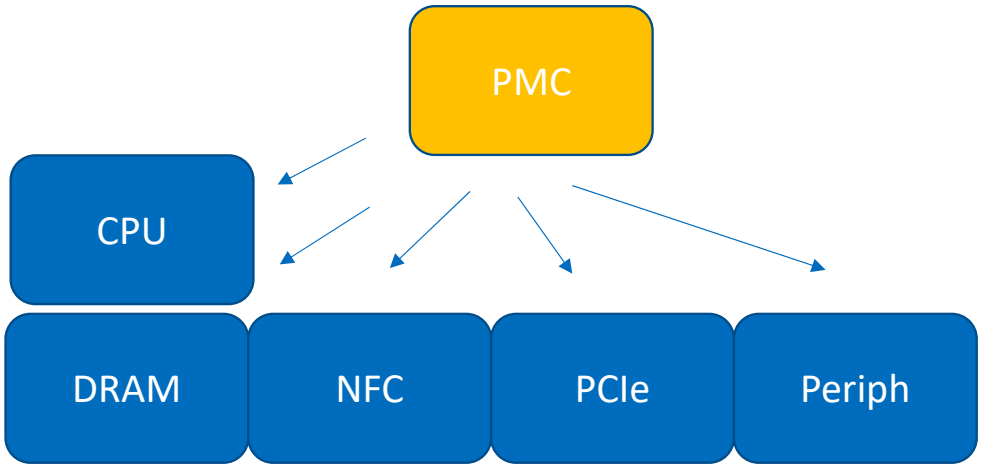
- Contemporary laptops are thinner and lighter, so it is challenging to dissipate increasing heat brought by higher speed components. The power consumption of PCIe Gen5 SSD controller is 50% higher than Gen4 in 12nm based on our estimation
- SM2508 is fabricated with TSMC 6nm process. Comparing to 12nm, it can bring about 30% power reduction. With advanced process and optimized design, SM2508 can achieve less than 3.5W. PCIe Gen5 SSD become a workable option for PC OEMs.

Process	Mode	ASIC Power	Diff%
TSMC 12nm	L0 Gen5	5W	100%
TSMC 6nm	L0 Gen5	**<3.5W**	70%

Low power mode policy

- The conventional way is using CPU to control the power states. The problem is CPU itself consumes meaningful power
- PMC (Power Management Controller) is a programmable controller dedicated in power domain control and power management policy execution





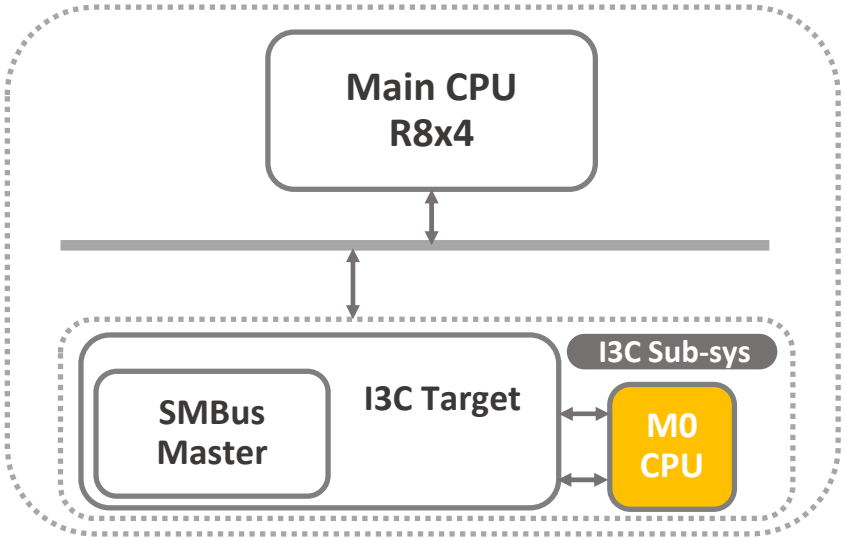
The Advantages with PMC

Scenario	Conventional	With PMC
IDLE	CPU keep alive until system IDLE	CPU can enter sleep when no task.
Power state switching	Different power domains need to be turned on/off by a fixed order	No limitation on sequence because PMC is an always-alive circuit.
Event trigger in sleep mode	It takes long latency to resume and re-entry to low power mode.	No need to wake up CPU for some cases (Ex. Host access Register via SMBUS/PCIe/NVMe)

Flexible peripheral interface design

- SSD used to operate as a standalone device. The only traffic with host was data read/write commands
- Nowadays, hosts like to cooperate more with SSD, e.g., thermal monitoring, platform resilience/attestation/recovery, and even in-system debugging
- All these operations need sideband interfaces such as SMBus or I2C and now I3C

Flexible peripheral interface design



- The conventional way is to use a pure hardware circuit. Not complicated but there is no flexibility
- SMI PCIe Gen5 SSD controllers introduce an ARM M0 CPU to do the dedicate controls
- Upgradable through code changes whenever a new standard is published

Peripheral interface capability

Standard	SMI Gen5 controller
SMBus Spec	3.1
NVMe MI Spec	1.2
I3C Spec	1.1.1
Operation freq.	≦12.5MHz
Low power resume time	<5us, depends on M0 power resume
Address Resolution Protocol (ARP)	Support
Alert	Support
Vital Product Data	Support
NVMe Basic Management Command (NVMe MI Appendix A/C)	Support
MCTP SMBus/I3C	Support
SPDM SMBus/I3C	Support
NVMe MI SMBus/I3C	Support

Summary

- SMI 1st PCIe Gen.5 SSD controller, SM2508, incorporate lots of innovations for the balance between performance and power. We believe this chip will be best for client SSD usages
- As a leading SSD controller vendor, SMI will continue to explore new technology and work with our customers to provide the best SSD solutions to the market

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Meet us at booth #315

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