

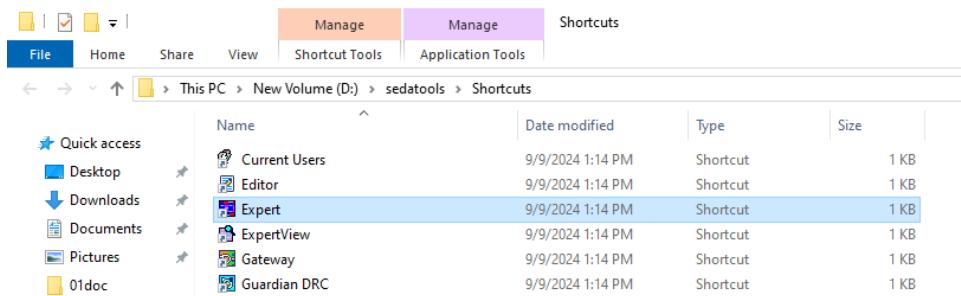
Expert 使用教程 (包含 DRC, LVS)

DRC: design rule check

LVS: layer vs. schematic

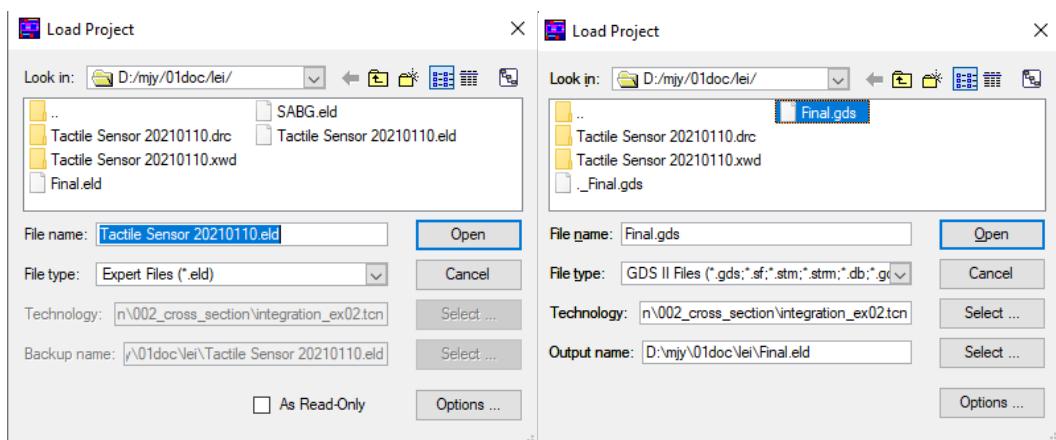
Expert: 用来画版图的

1. 双击 expert 软件

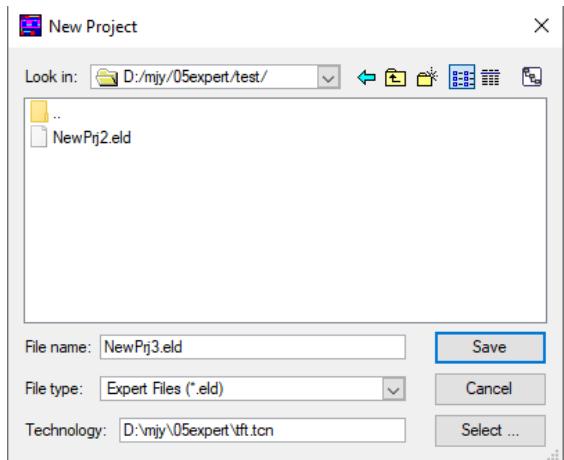


2. 如果已有文件，则 file -> load project

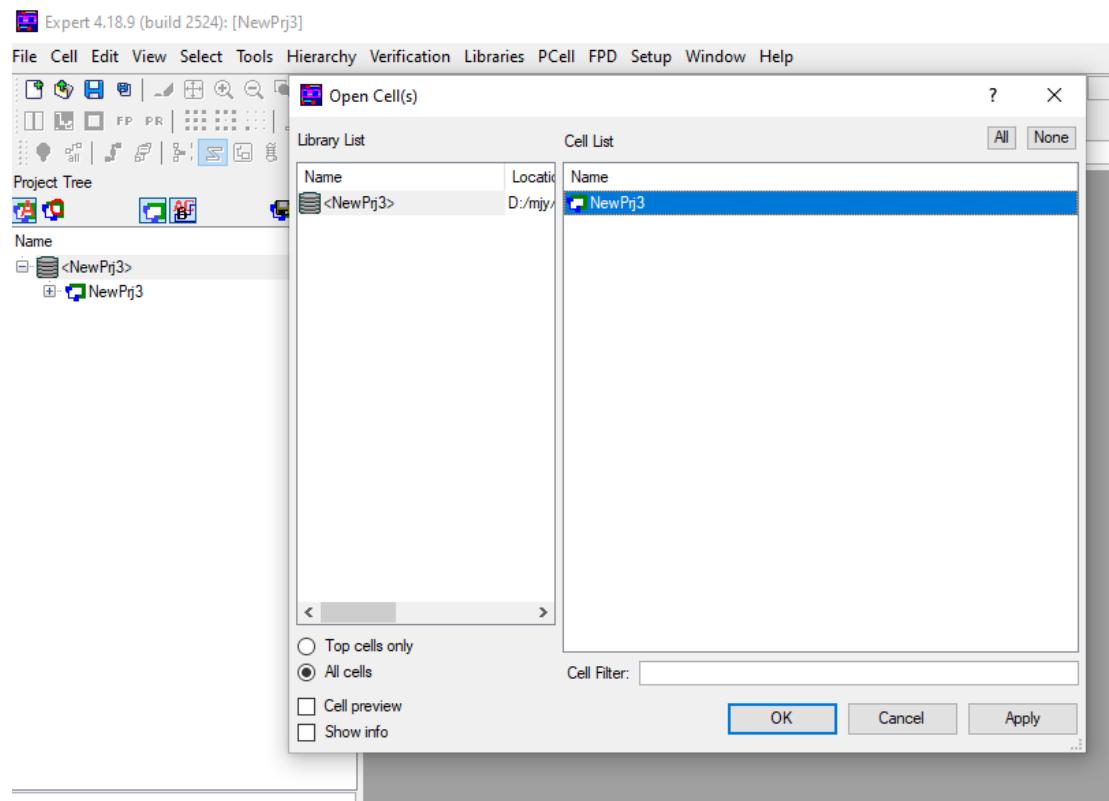
有两种文件格式: gds 不包含 tcn 文件，所以要自己选择 technology 文件；eld 文件包含 tcn 文件，所以不用选择 tcn 文件



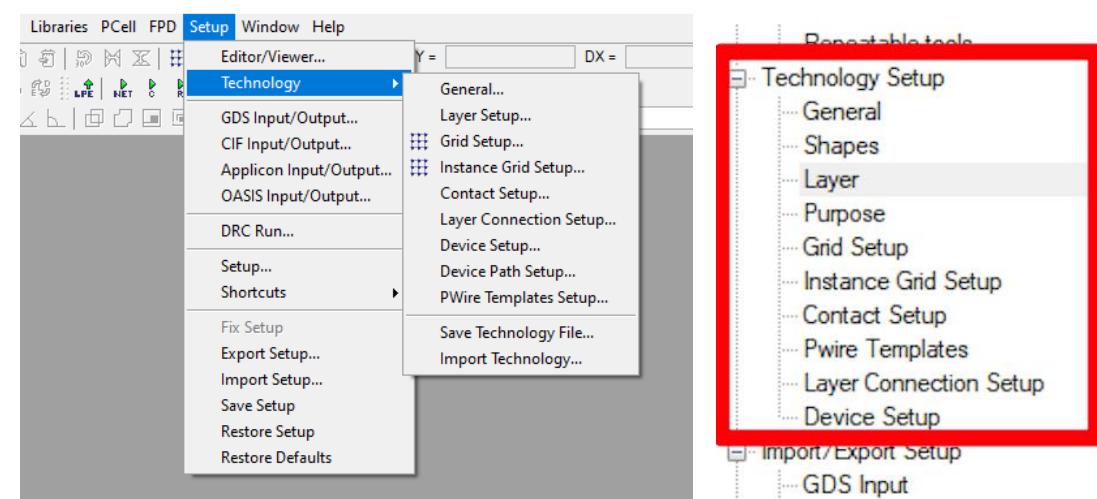
如没有文件，则新建 project，新建的时候可以选择 gds，或 eld 文件，在新建的时候要选择 tcn 文件



3. 打开/新建 project 后，新建 cell，可以每个元器件都新建一个 cell，因为这个 cell 可以直接拖入新的 cell 中。



4. 新建 project 后，一定要修改 (check) technology，check technology 里面的每一部分内容。



Layer 层：工艺的步骤

TG 是 gate 层，AC 是 channel 层，via_gds 层是通孔层，DS 是源漏层；

G_TXT 是 gate 层端口的文字标注，用来产生 port 端的；

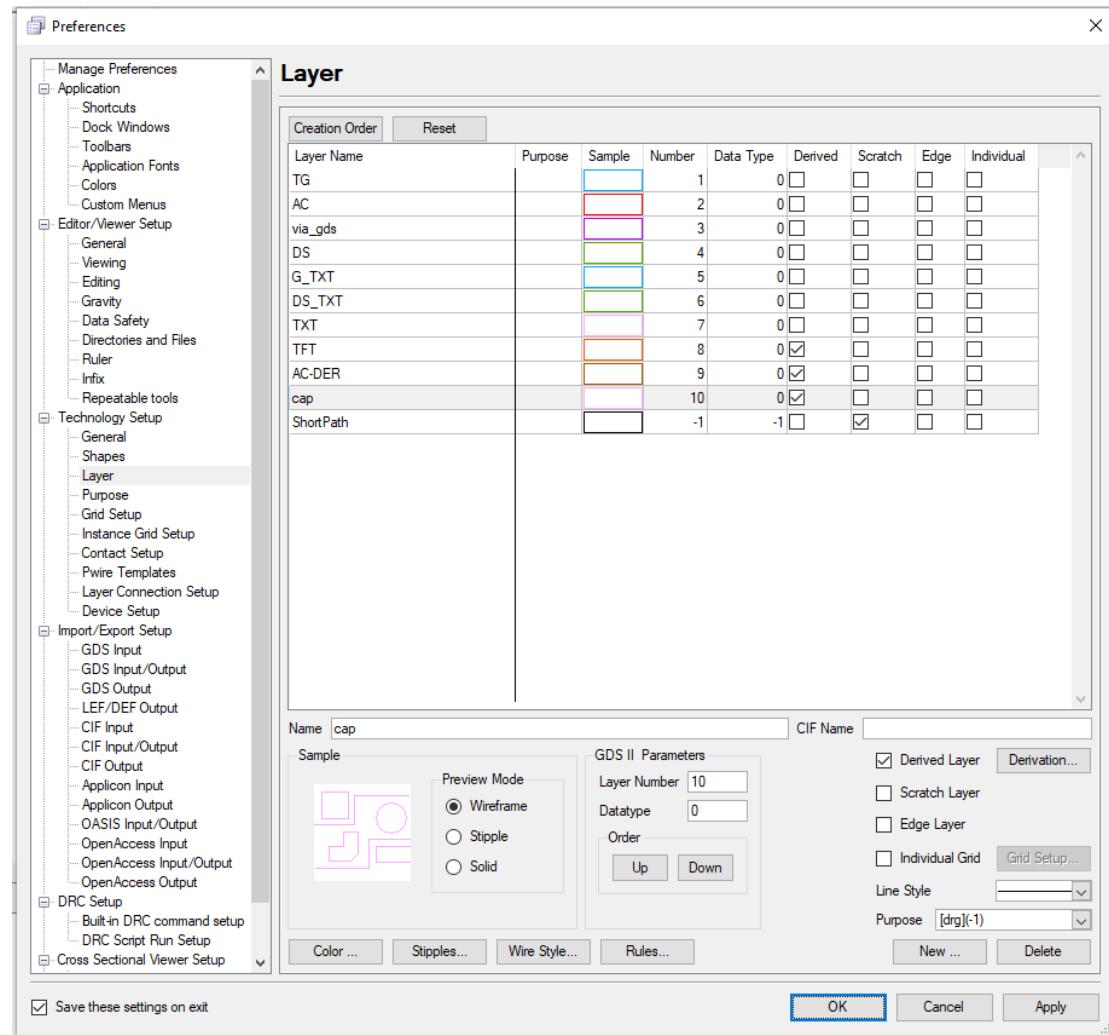
DS_TXT 是 DS 层端口的文字标注，用来产生 port 端的；

TXT 是标注，没有任何实质作用；

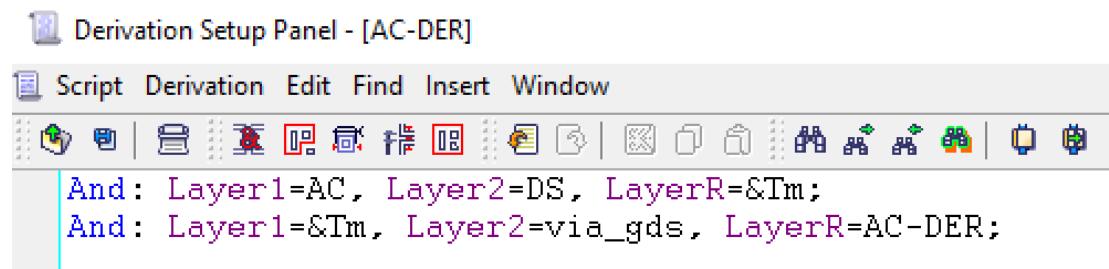
TFT 是派生层，用来识别是不是 TFT 的；

AC-DER 是派生层，用来新建一种层的；

Cap 是派生层，用来识别是不是 cap 的。



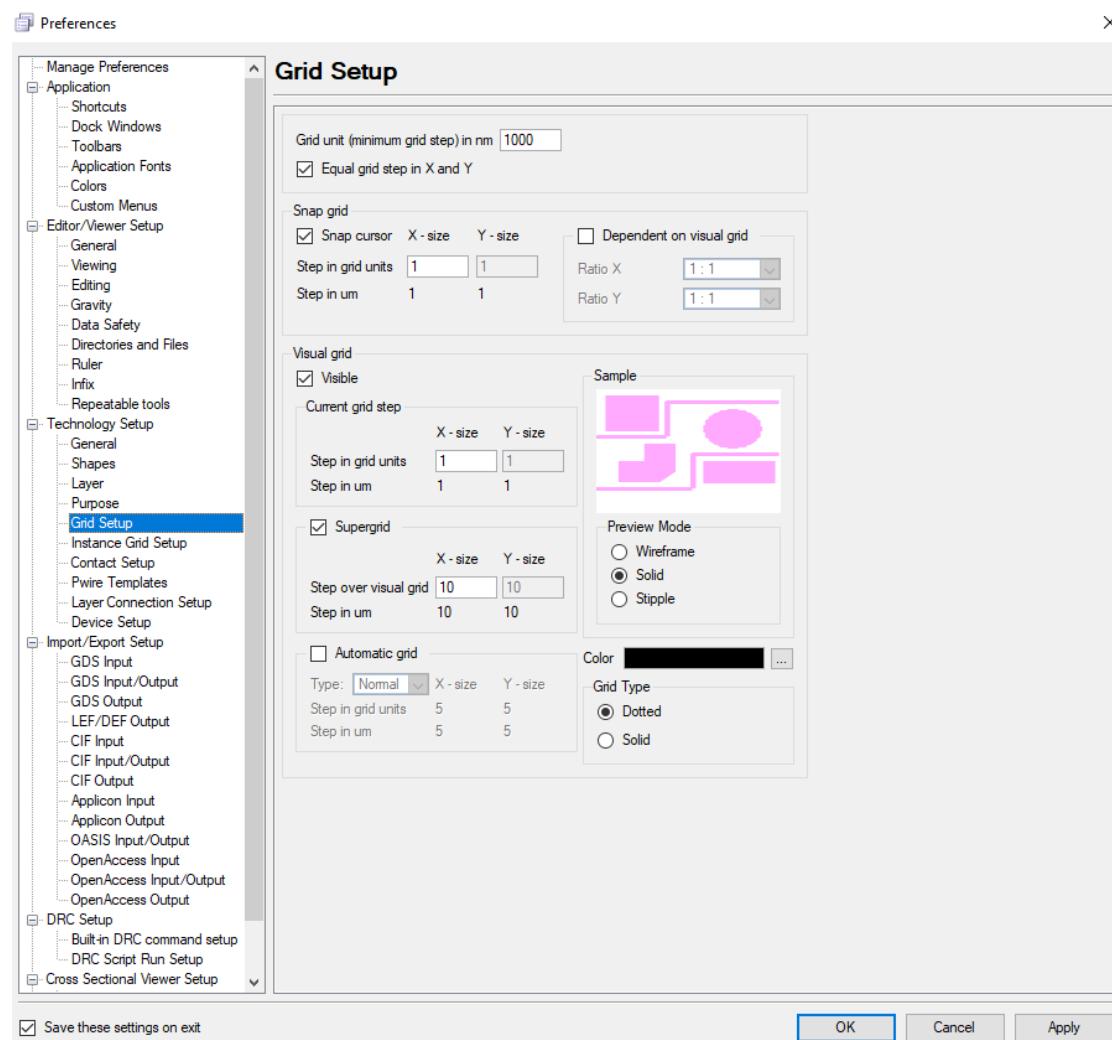
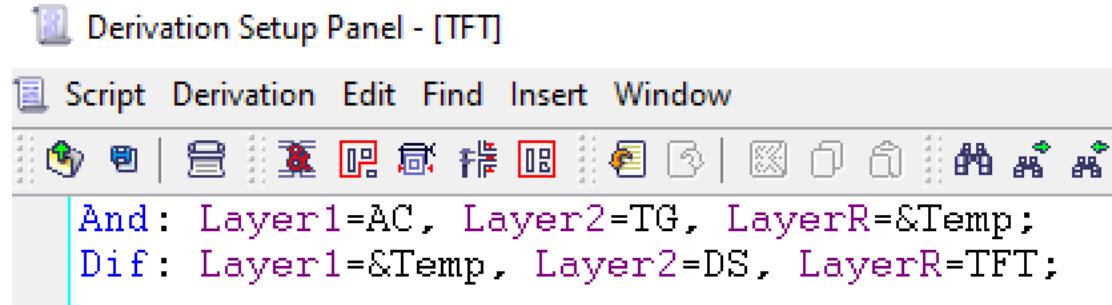
AC-DER 是当 DS 和 gate 层不搭上的时候，TFT 是识别不出来的，所以 AC-DER 是 DS 和 AC 层以及通孔层的交集。



以下是 TFT 的识别派生层，gate 层和有源层的重叠部分，再将该重叠部分去掉 DS 部分，如此即可识别出 TFT 以及 TFT 的宽长。

注意：DS 部分和 gate 层和有源层的重叠部分一定要有重叠或是搭上，否则出现 bad device 的错误!!!

Dif 语言： DIF A B AB 表明 A 中不包含 B 的部分

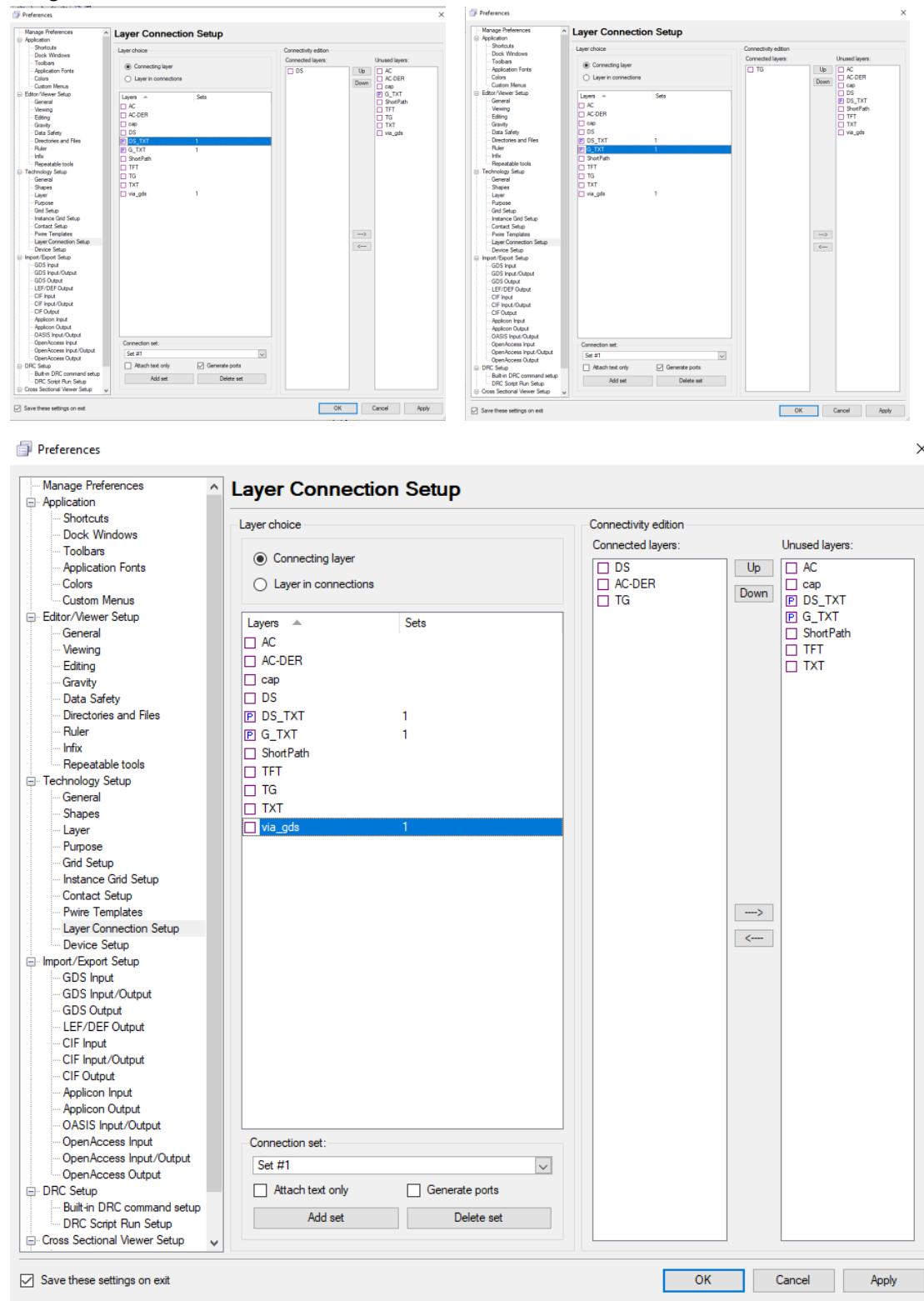


Connect 层设置也比较重要，用来设置哪一层可以让哪些层连在一起

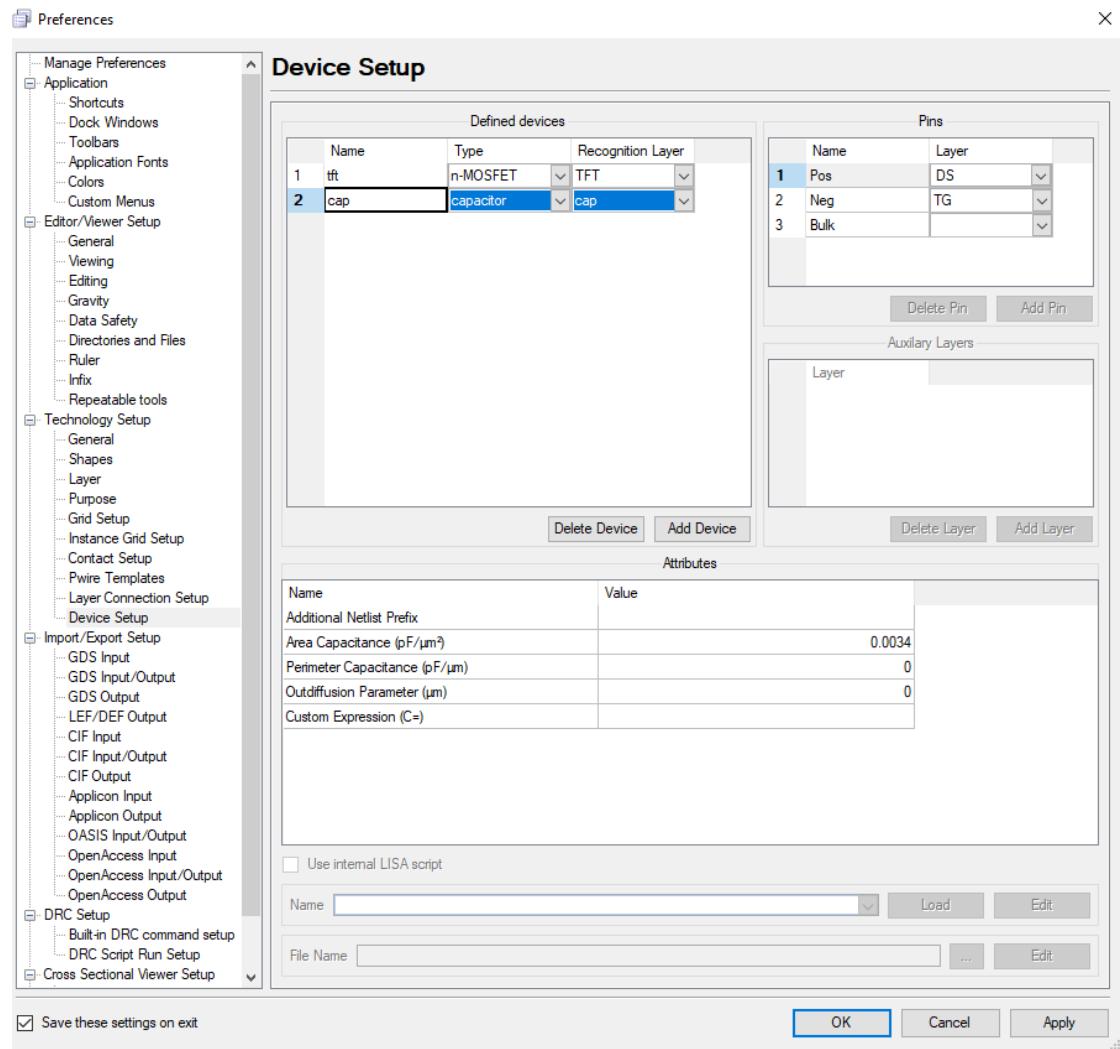
比如，DS-TXT 需要和 DS 层相连，

G-TXT 需要和 gate 层相连

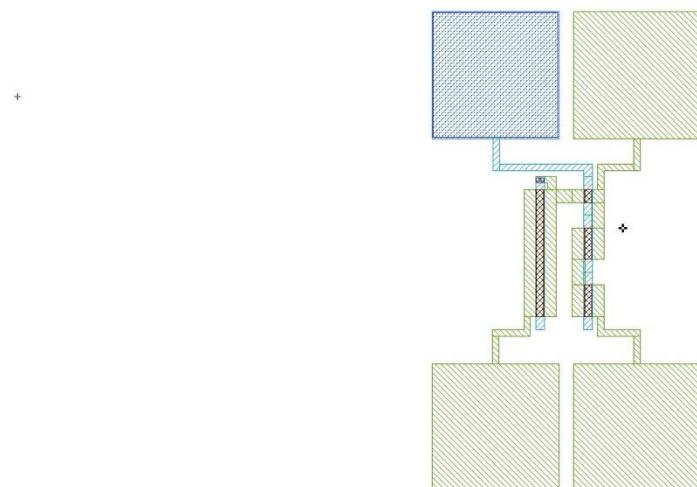
Via-gds 需要和 TG,DS,AC-DER 相连



然后 device setup, tft 选择 n-mosfet, 识别层就是刚刚建的派生层 TFT, 然后右边的 pin 是 DS,TG,DS
 (如果 DS 没有接触到 gate 的话, 则是 AC-DER,TG,AC-DER)
 如果是 cap 的话, 需要确定他的面电容

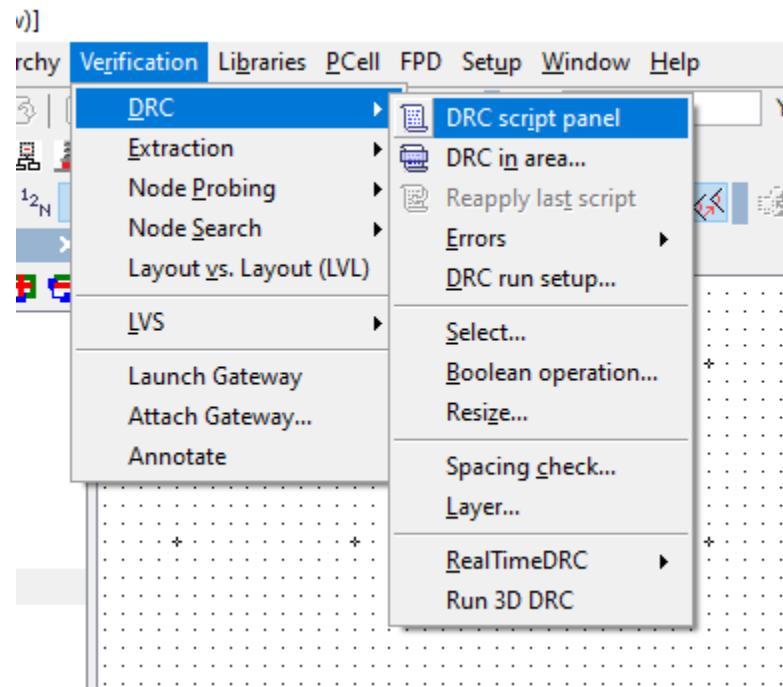


5. 在设置完 technology 后, 可以开始画版图了。注意: 如果遇到宽长比较大的情况, 为了让版图更好看, 比如 200u/10u, 可以画四个 50u/10u 并联的 tft 来代替。



6. 画完版图后是 DRC (design rule check), 这个 DRC 的规则是由自己来编写的, 主要来检查版图的最小线宽, 最小间距这类的。

1) 在 expert 软件中, verification -> DRC -> DRC script panel



以下是 DRC 规则的编写格式, 主要包括 5 中语法: boolean, check, flow, resize, select。具体的用法参考说明书和 examples 文件夹中的实例

```
Scope: hierarchy;

//merge all layers
Merge: Layer=G_M, LayerR=G_M;
Merge: Layer=SD_M, LayerR=SD_M;
Merge: Layer=GSD, LayerR=GSD;
//merge_input: on;

//Width and Spacing for G_M layer
width: layer=G_M, limits<6, id="minimum width of gate_metal is 6um";
outdistance: layer=G_M, limits<6, id="minimum spacing of gate_metal is 6um";

//Width and Spacing for SD_M layer
width: layer=SD_M, limits<6, id="minimum width of sd_metal is 6um";
outdistance: layer=SD_M, limits<6, id="minimum spacing of sd_metal is 6um";

//Width for VIA layer
Width: Layer=G_VIA, Limits < 15, ID="g via is too small";
Width: Layer=SD_VIA, Limits < 15, ID="g via is too small";

//DRC rule for VIA
CompDistance: Layer1=G_VIA, Layer2=G_M, Limits <3,
ID="gm gvia error";
CompDistance: Layer1=G_VIA, Layer2=SD_M, Limits <3,
ID="gm gvia error";
CompDistance: Layer1=G_VIA, Layer2=GSD, Limits <8,
ID="gm gvia error";

//Spacing between GSD and AA
OutDistance: Layer1=GSD, Layer2=AA, Limits <5,
ID="aa is too close to gsd";
```

DRC Script Panel - [D:/mjy/01doc/lei/DRC.dsf - [w50I10](auto)]

File Edit Find Insert DRC Setup Window

```

Scope: hierarchy;

Merge: Layer=BG, LayerR=BG;
Merge: Layer=DS, LayerR=DS;

Width: layer=BG, limits<10, id="minimum width of gate_metal is 10um";
Outdistance: layer=BG, limits<10, id="minimum spacing of gate_metal is 10um";

Width: layer=DS, limits<10, id="minimum width of sd_metal is 10um";
Outdistance: layer=DS, limits<10, id="minimum spacing of sd_metal is 10um";

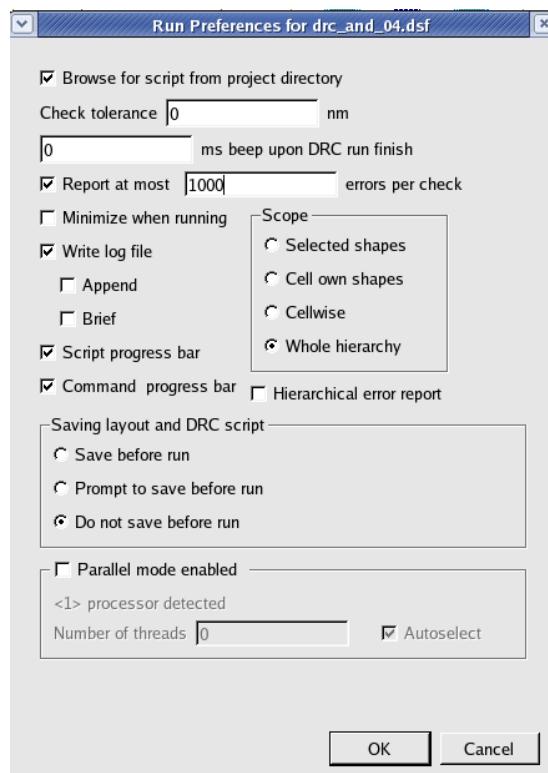
Width: Layer=via_gds, Limits<5, ID="via is below 10um";

InDistance: Layer1=via_gds, Layer2=DS, Limits<2,
ID="gm gvia error";
InDistance: Layer1=via_gds, Layer2=BG, Limits<2,
ID="gm gvia error";

OutDistance: Layer1=BG, Layer2=DS, Limits < 2,
ID="aa 2 is too close to gsd";

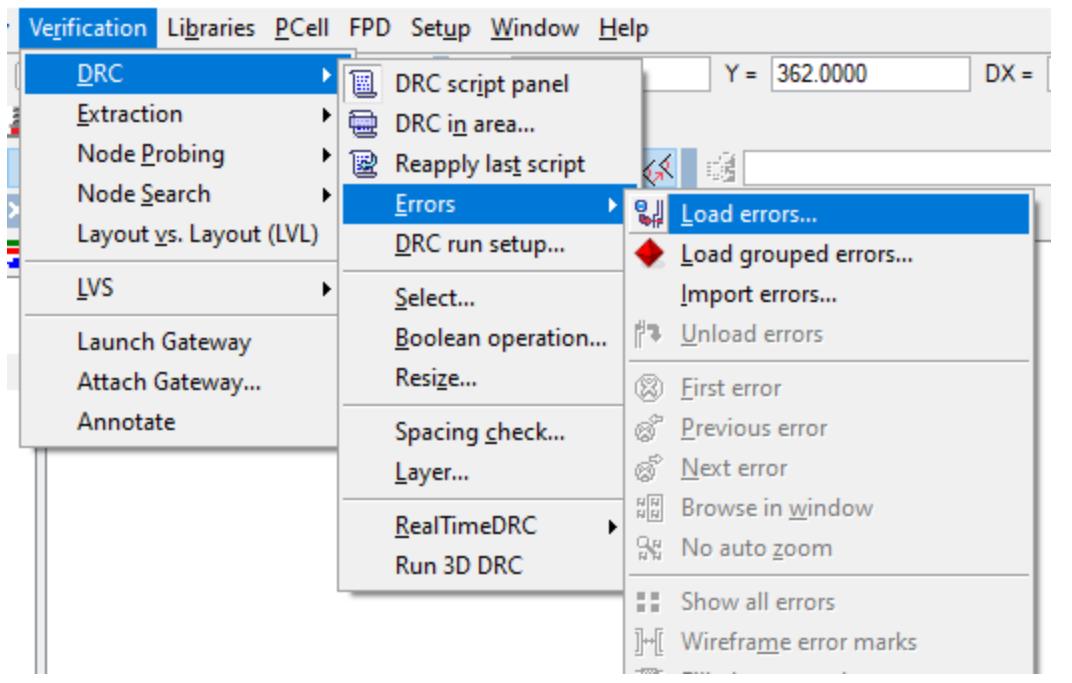
```

2) 在 DRC 脚本页面, 设置 DRC 报告参数, Setup-Current DRC script run preferences



3) 设置好后点 OK, 然后在 DRC 脚本页面选择 DRC-Run, 就会生成后缀为.log 的文件, 该文件里包含 DRC 的检查结果。

4) 检查错误: 在 Expert 界面, 选择 Verification-DRC-Errors-Load errors



Load DRC Errors

Runs

Cell	Scope	Hierarchy	Started	Finished	Errors	Script	Comments	Actions
inv	Whole hierarchy	No	09/13/24 21:42:03	09/13/24 21:42:03	1	DRC.dsf		<button>Delete...</button>
inv	Whole hierarchy	No	09/13/24 21:42:13	09/13/24 21:42:13	1	DRC.dsf		<button>Delete All...</button>

Checks

Operation	Layer(s)	Errors	ID	Comments	Actions
3.Width < 10.0000	TG	1	minimum width ...		<button>Select All</button> <button>Delete...</button> <button>Show All</button> <input checked="" type="checkbox"/> <button>Display color</button>

Errors and Cells

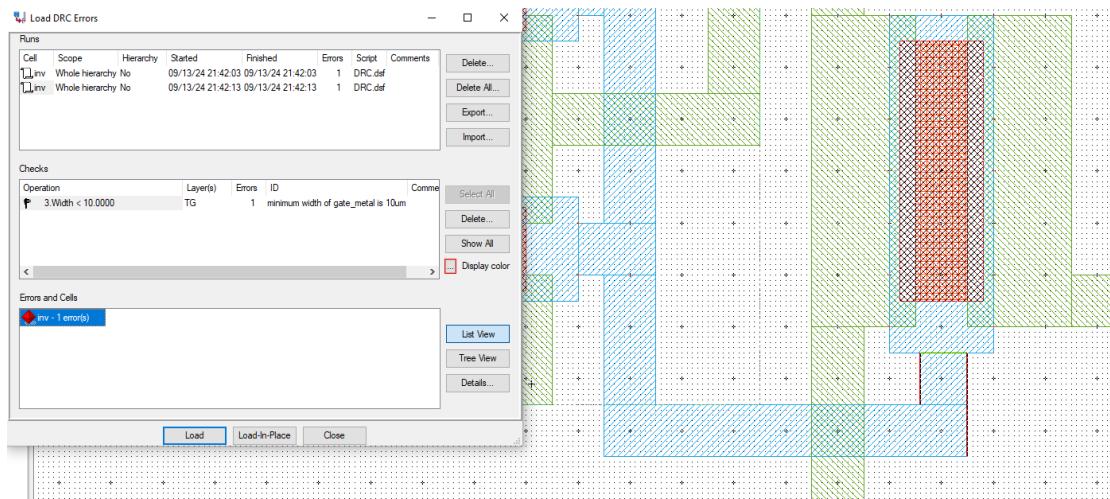
inv - 1 error(s)

List View
Tree View
Details...

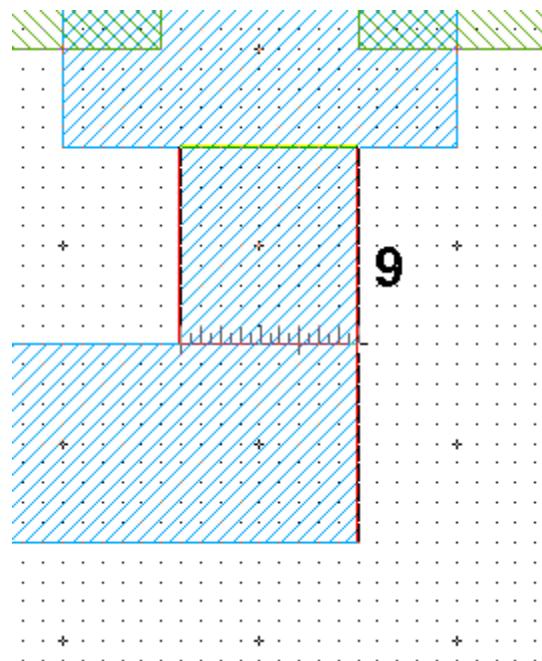
Buttons

Load Load-In-Place Close

- 5) 选中需要查看的错误，点击页面最下方的 Load，然后选择 Verification-DRC-Errors-First error(next error)，就能在版图中查看到具体的错误的地方。

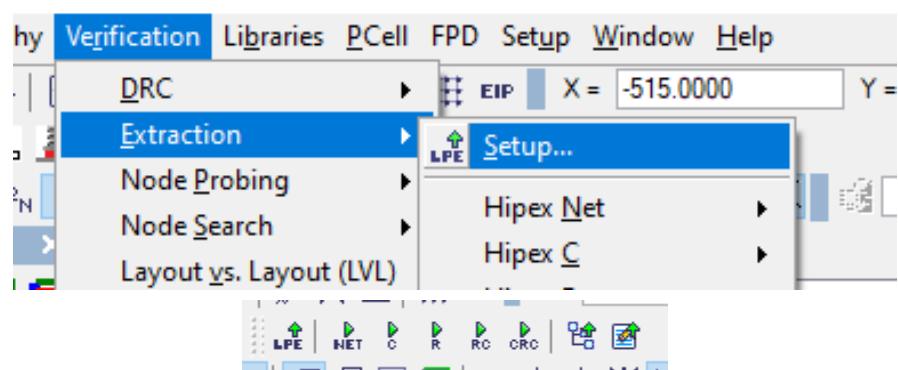


测量了一下，线宽是 9um，自己定义的最小线宽是 10um，所以报错了。

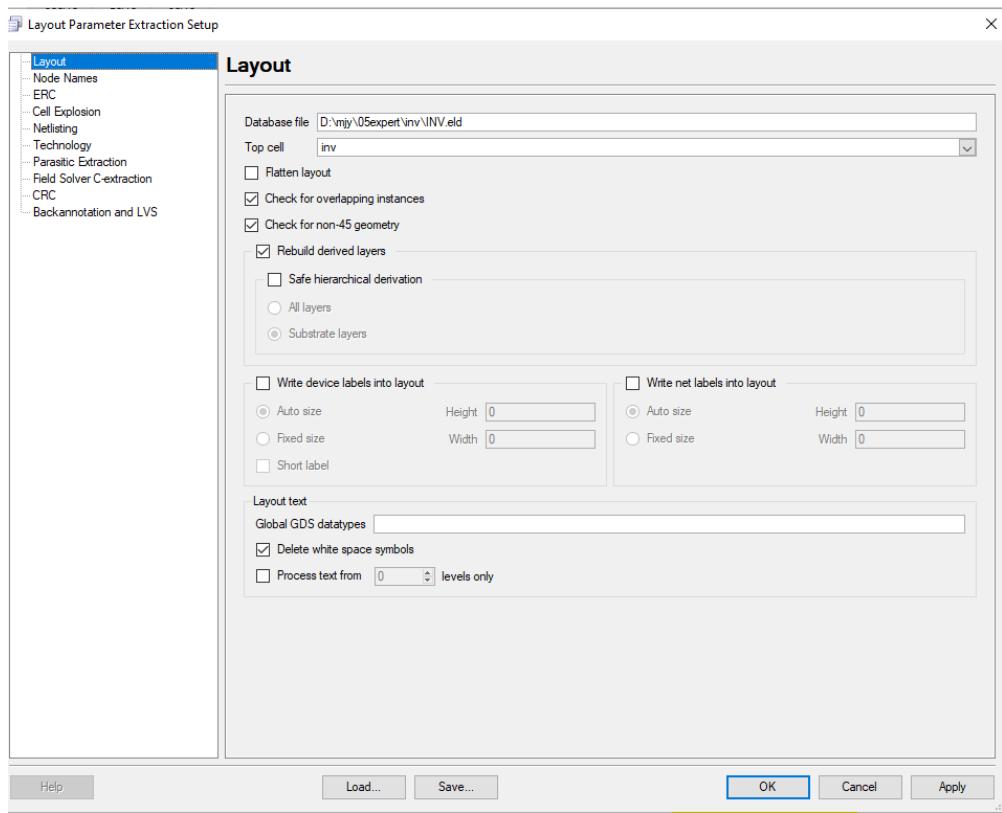


7. 接下来是 LVS, layer vs. schematic, 是来检查原理图和版图的电路连接关系是不是对的

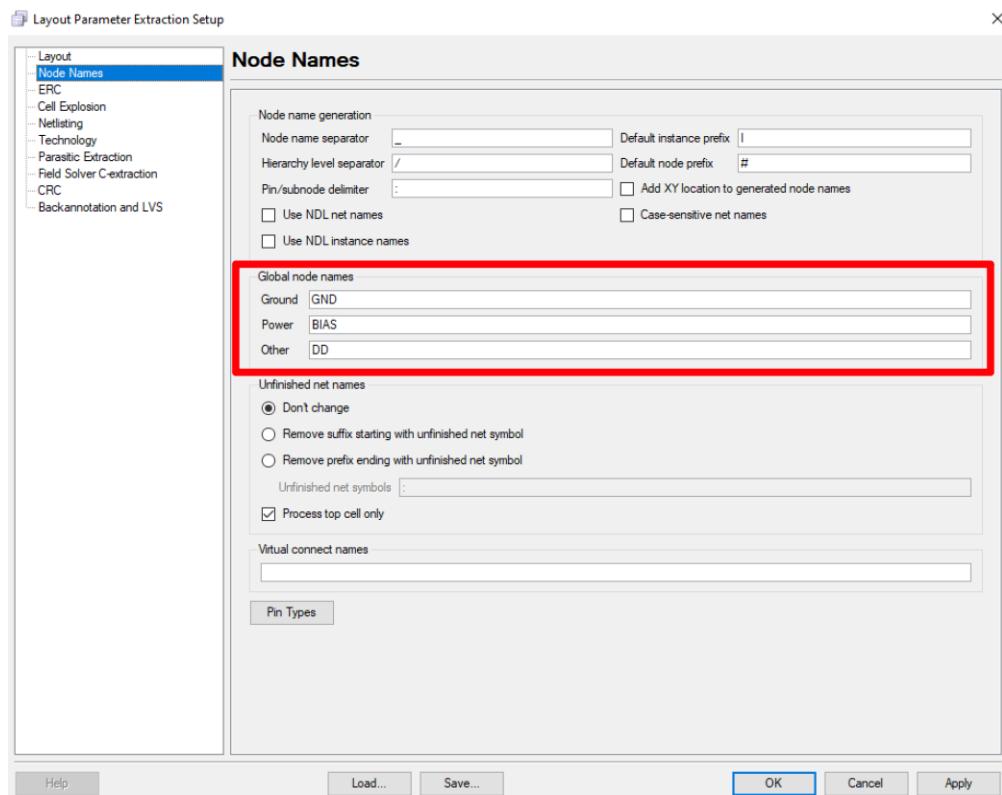
1) Verification -> extraction -> setup, 当然也可以在工具栏中的下图标进行设置。



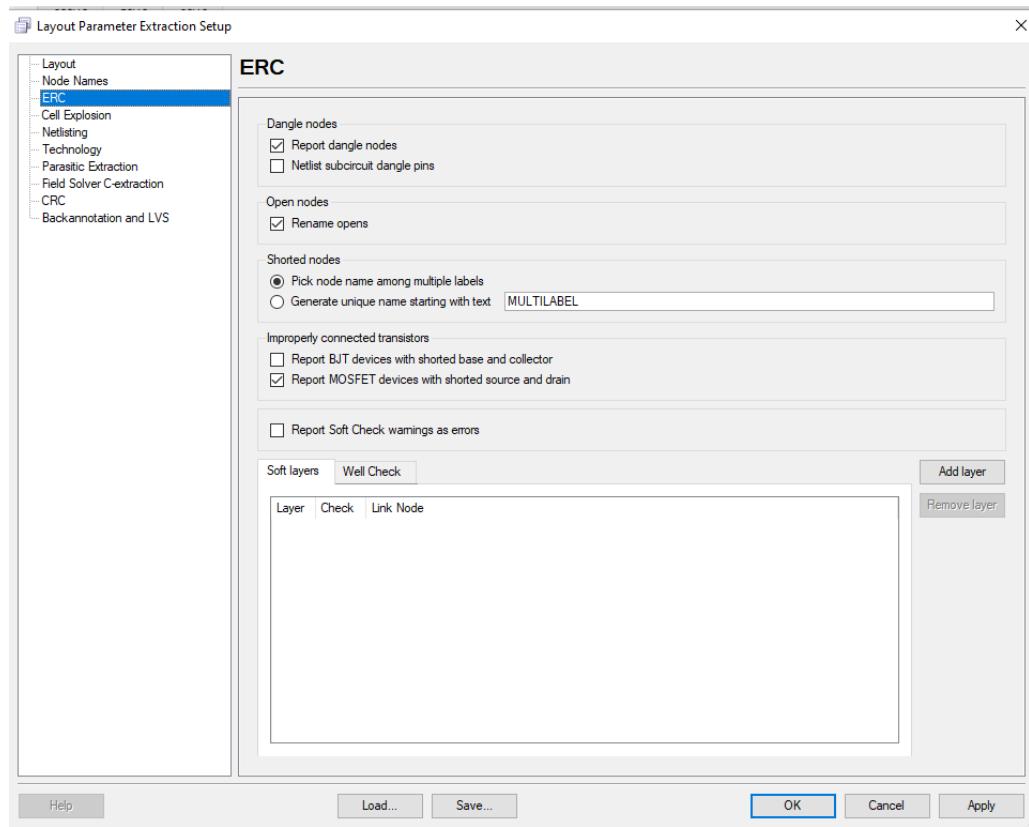
可以先按照这样来设置，验证过是可以的



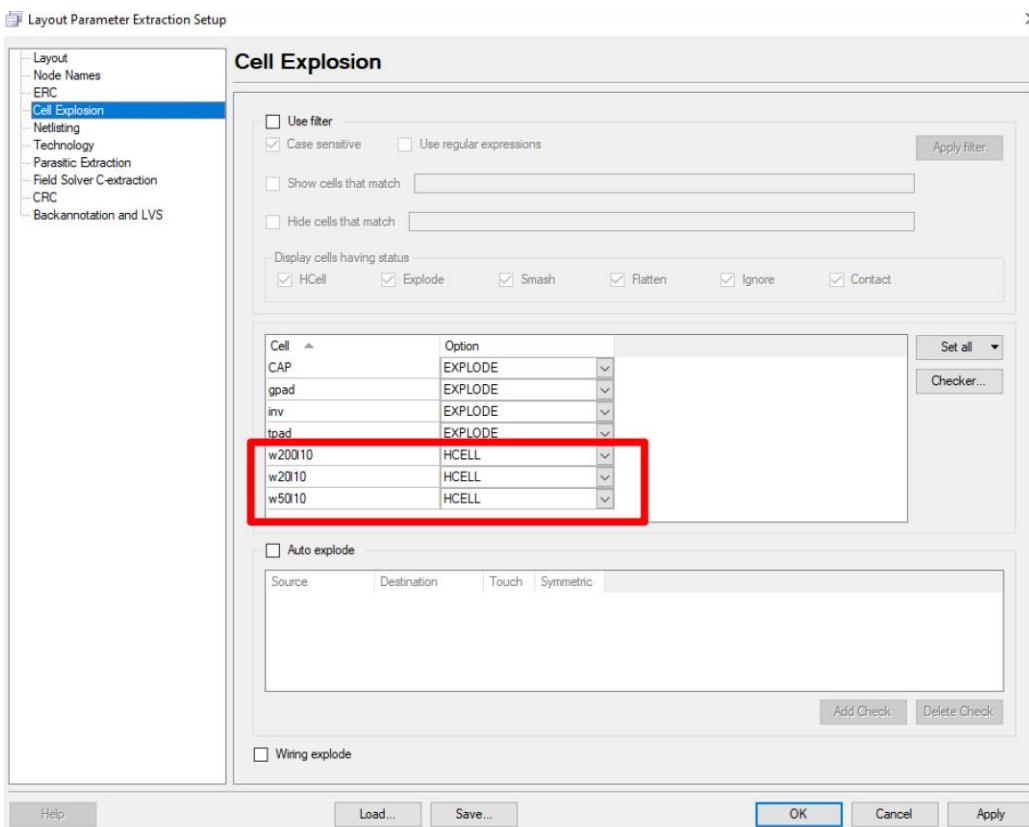
红色部分是在进行寄生电容参数提取的时候，要设置共同的地和 power

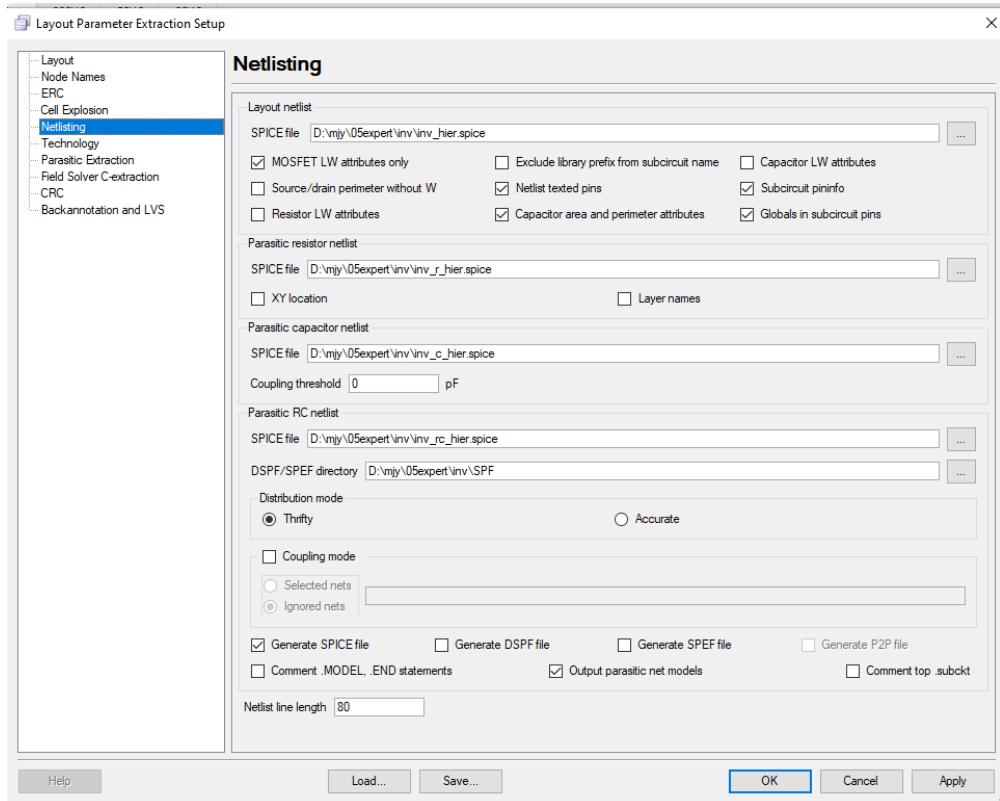


先按照这个来设置

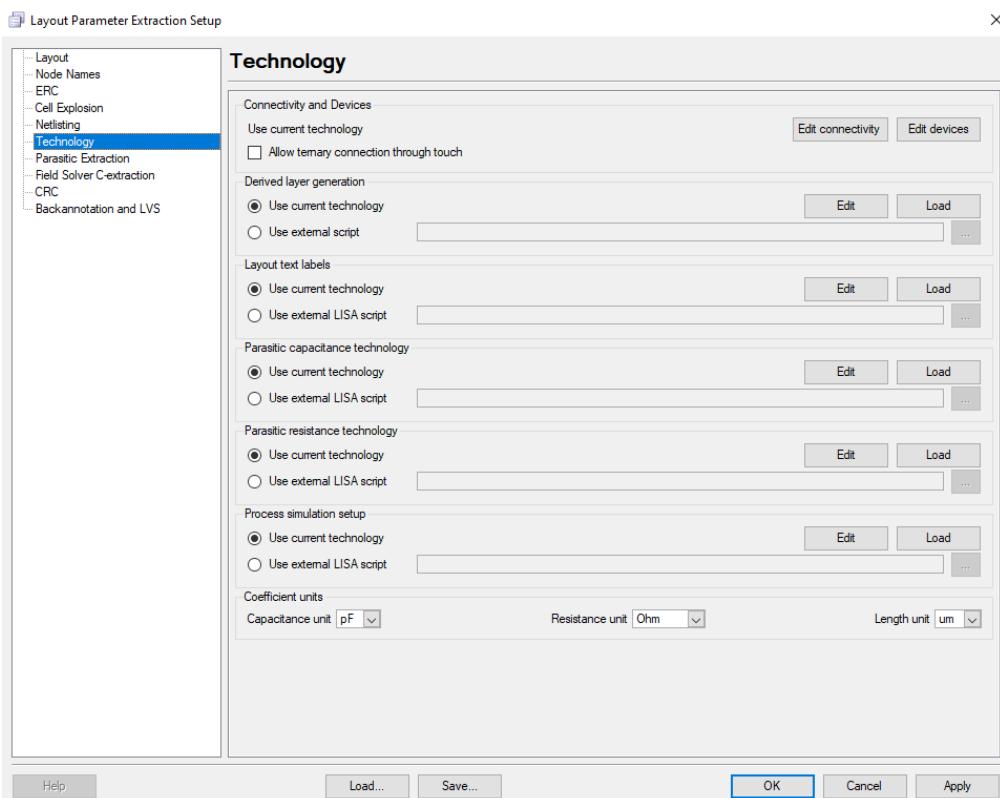


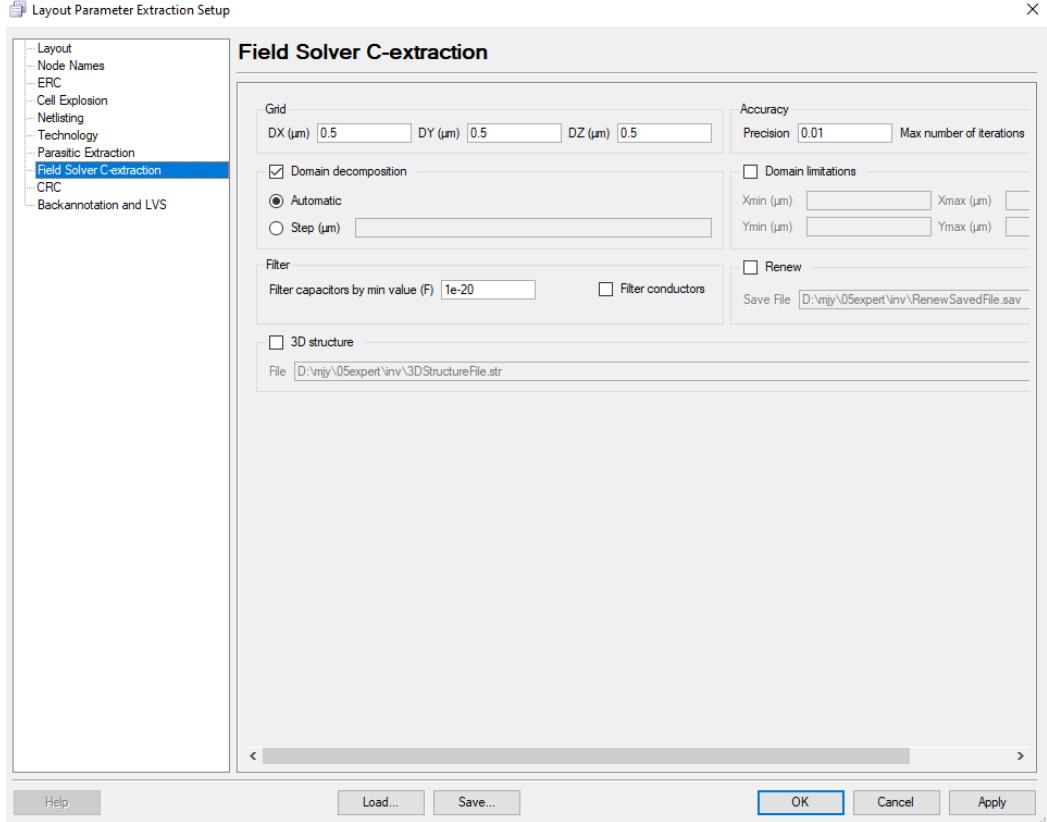
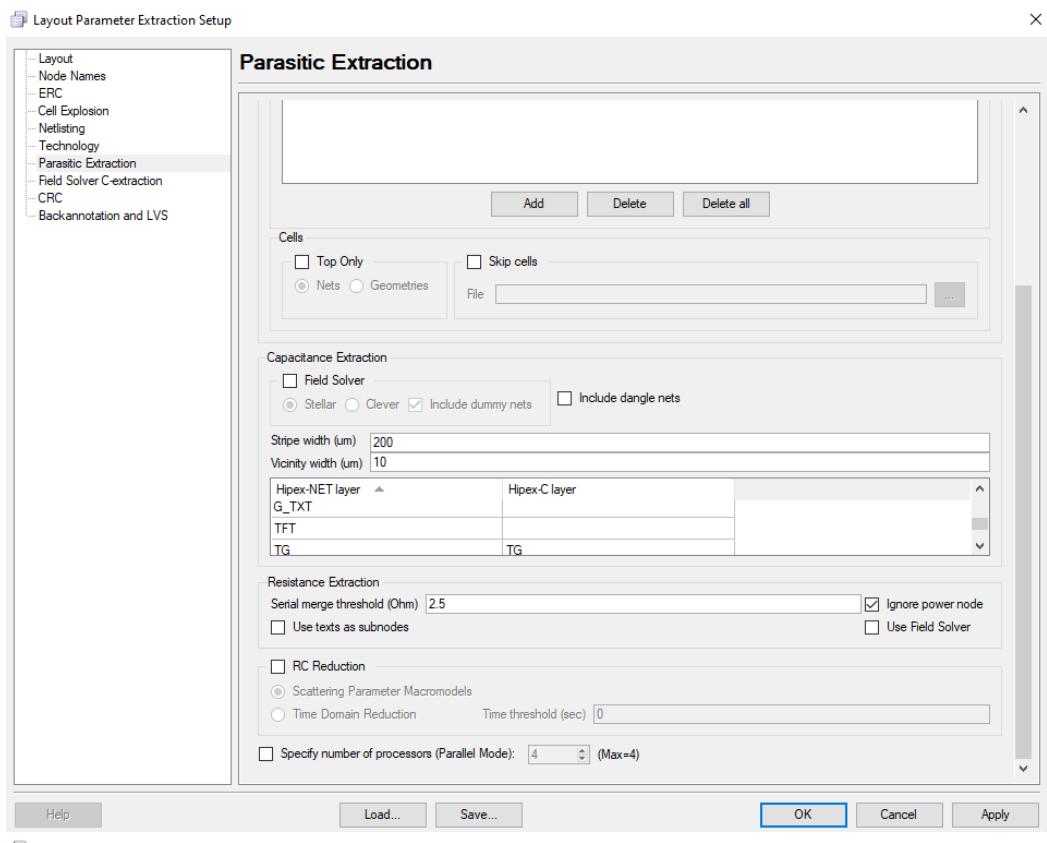
这个要注意，尽量还是把 tft 和 cap 来设置成 HCELL，如果设置成 explode，可能会报短路的错误

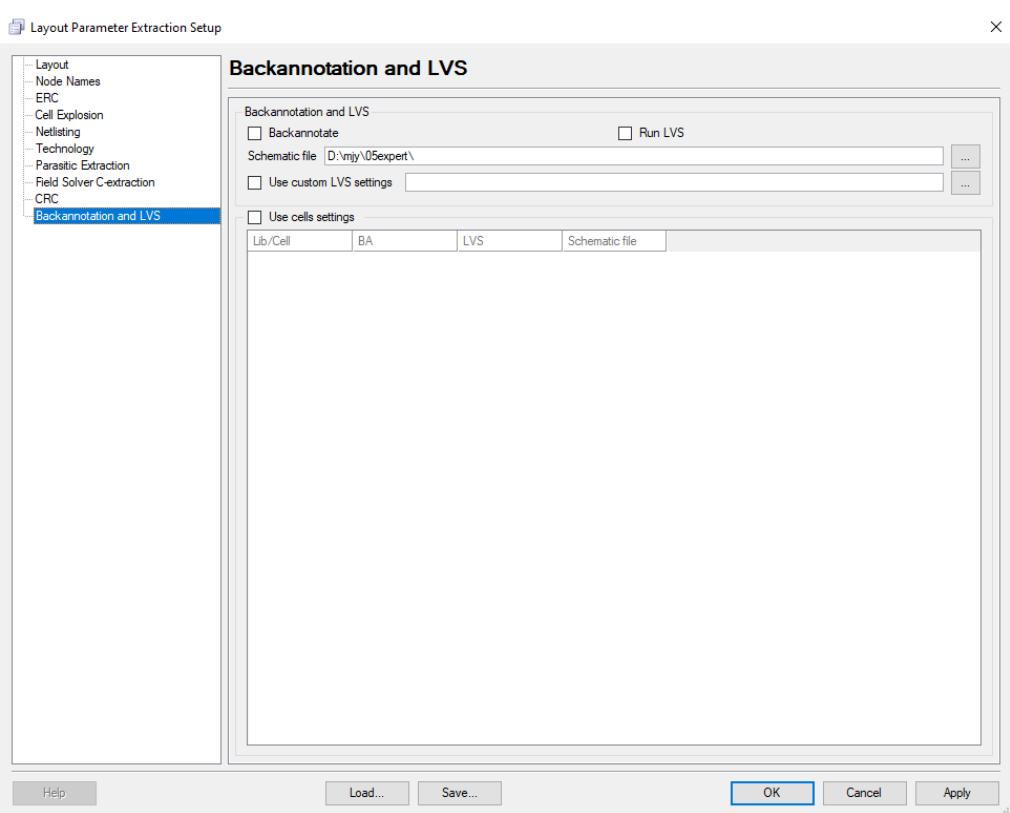
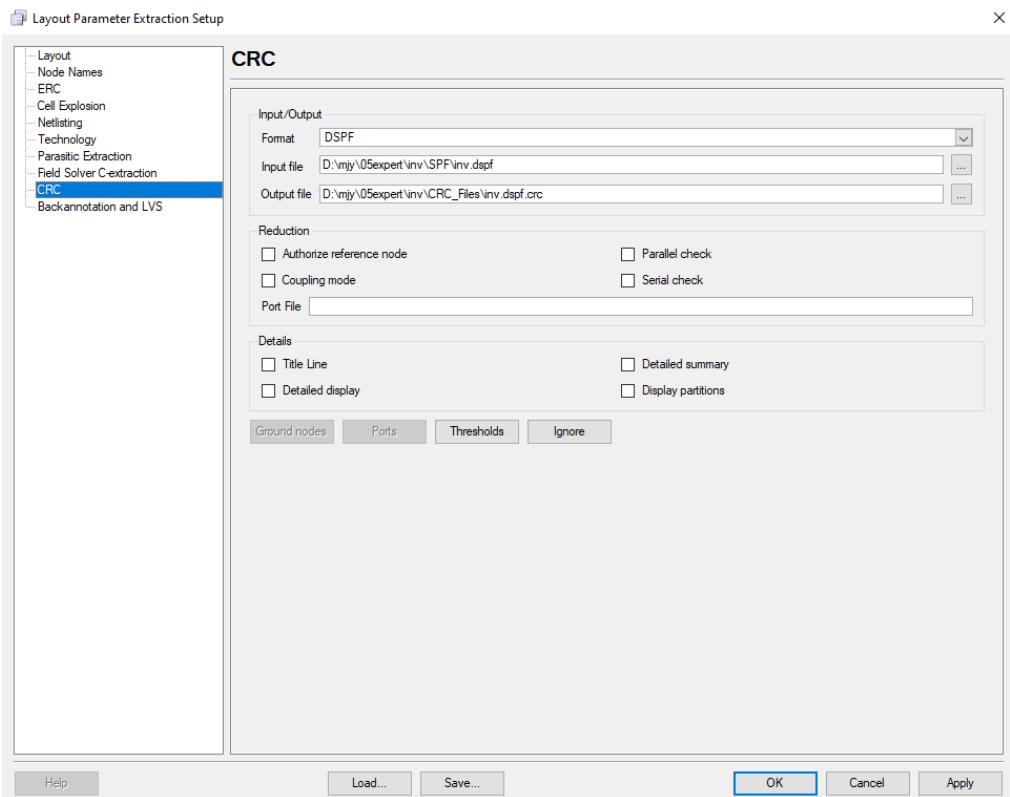




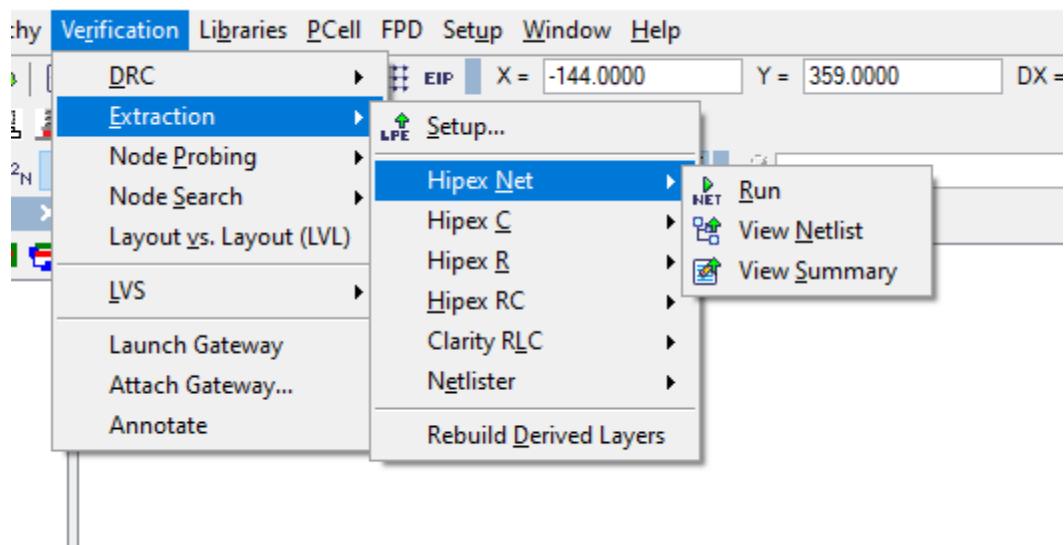
这个在寄生参数提取上很关键，后面会解释。



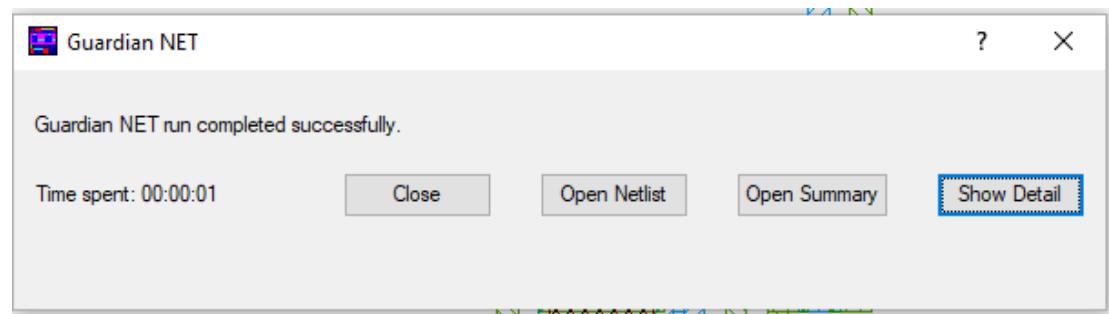




2) Verification -> extraction -> hipex net ->run

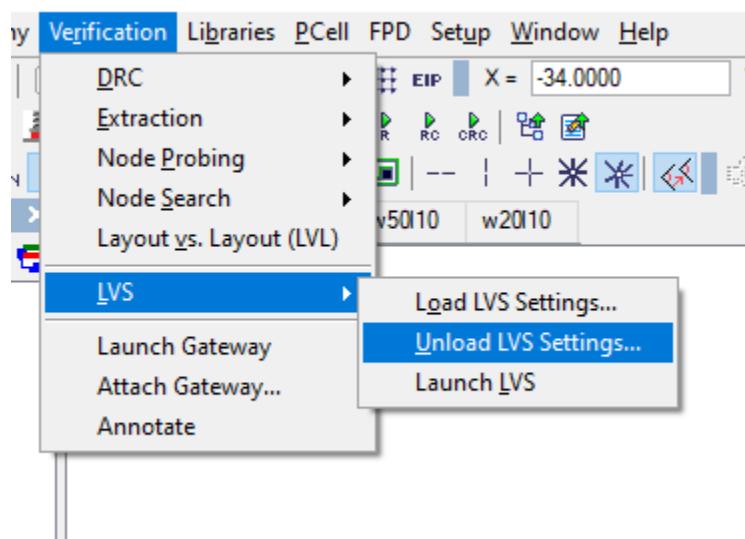


出现这个说明成功

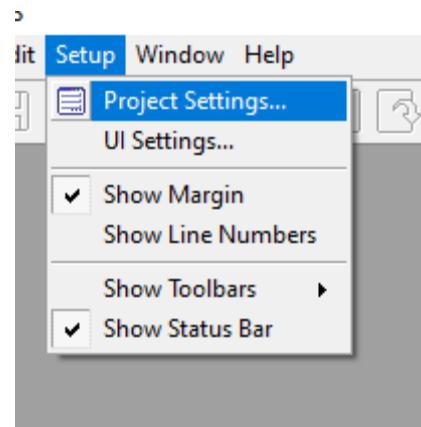


3) gateway 软件的电路图要求，需要去掉负载的电阻电容和电压源，输入输出端口用 pin 脚来表示，版图中没有对应的器件。可以在 Gateway 里面的 create netlist 中查看，是只读的，不能修改。

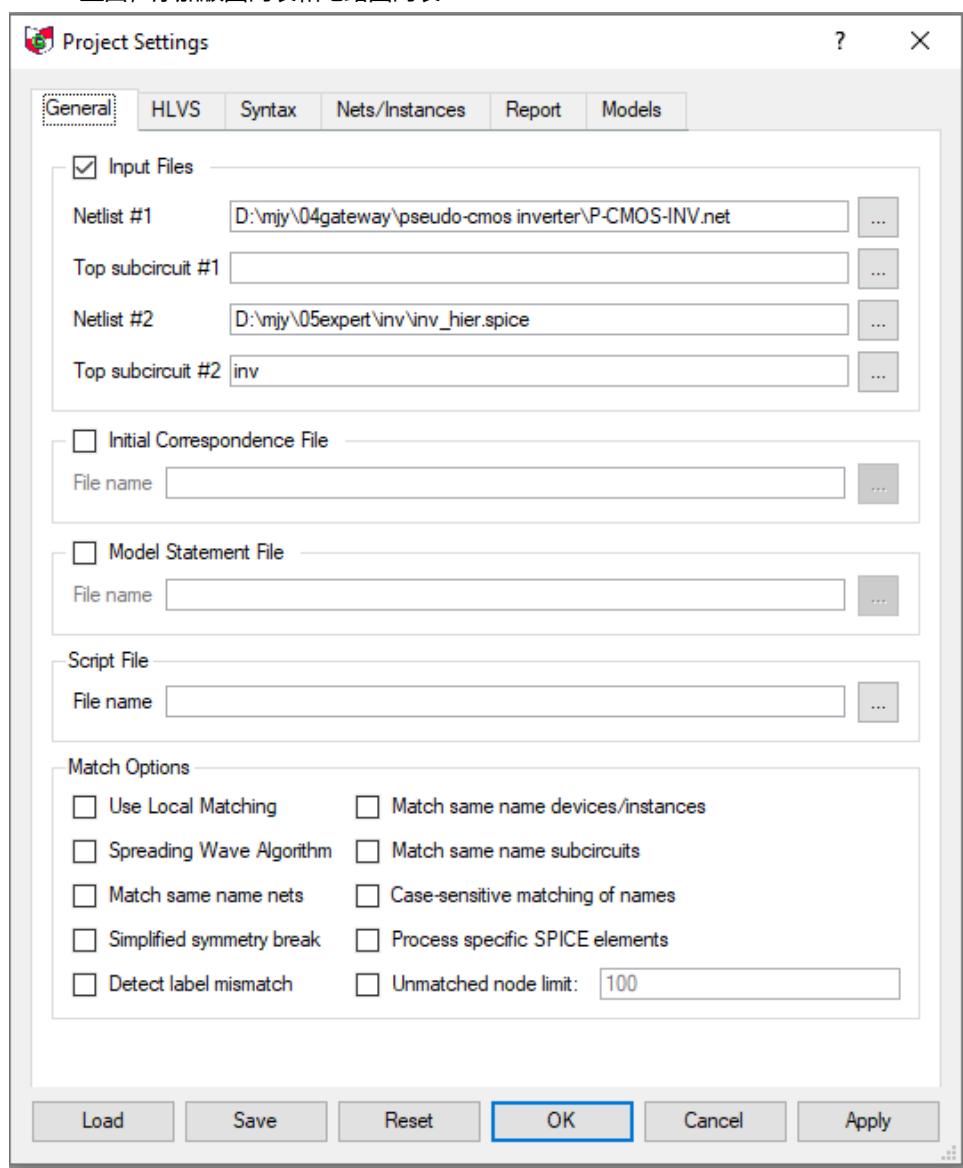
4) verification -> LVS -> Launch LVS



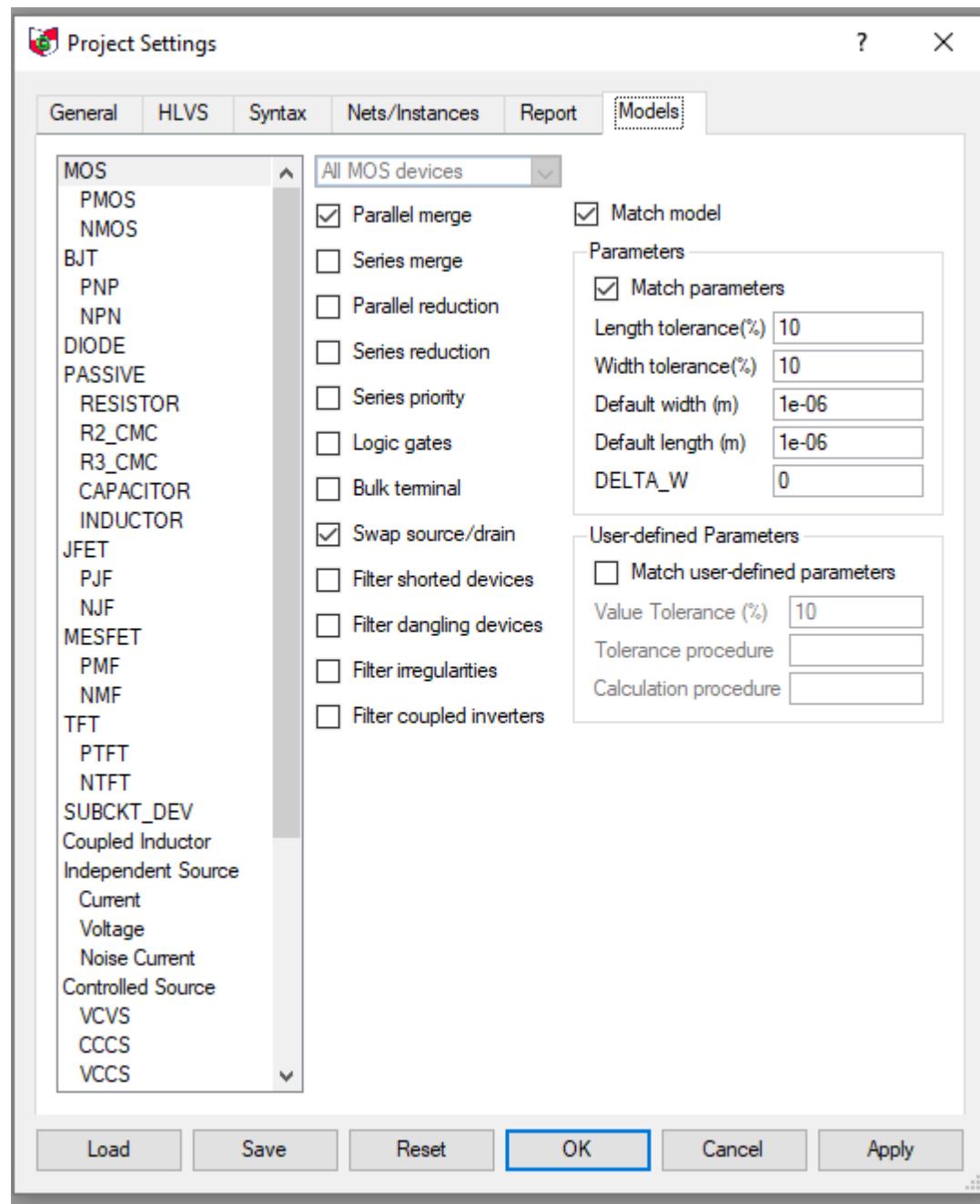
5) 进入 LVS 界面后, setup -> project settings



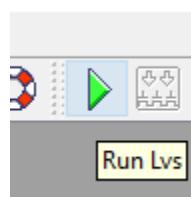
6) general 里面, 添加版图网表和电路图网表



6) models 里面, 勾上并联合并 (就是上述 200u/10u 的例子里画的 50u/10u), 勾上忽略 SD



7) 点击 run



D:\my\04gateway\pseudo-cmos inverter\P-CMOS-INV\vs\P-CMOS-INV.pms (Active Parameter Match File)

```

PARAMETER MATCHES

L0: M:  top_M1 . . . . . = (*) inv_X11_M13
    I=10u V=200u
L0: M:  top_M2 . . . . . = inv_X10_M10
    I=10u V=20u
L0: M:  top_M3 . . . . . = inv_X12_M10
    I=10u V=50u
L0: M:  top_M4 . . . . . = inv_X11_M10
    I=10u V=50u

(*) - indicates device instances formed by device merging, see merge file

```

D:\my\05expert\inv_hier.spice (Netlist #2)

```

*****
* Extracted SPICE netlist for top cell inv
* Created Fri Sep 13 21:53:43 2024 by hipex 3.6.10.R 64-bit (Wed Dec 05, 2018 9:00 PDT) versi
*****



GLOBAL D1AS GND DD
MODEL ttt NMOS
MODEL cap C

*****
* Sub-Circuit Netlist of : v20110
*****



.subckt v20110 #1 #2 #3
M10 #1 #2 ttt I=10U V=20U
.ends v20110

*****
* Sub-Circuit Netlist of : v50110
*****



.subckt v50110 #4 #5 #6
M10 #4 #5 ttt I=10U V=50U
.ends v50110

```

GUARDIAN MESSAGES

```

Reading netlists ...
First pass:
Spice file : D:\ajy\04gateway\pseudo-cmos inverter\P-CMOS-INV.net
Spice file : D:\ajy\05expert\inv\inv_hier.spice

Second pass:
Spice file : D:\ajy\04gateway\pseudo-cmos inverter\P-CMOS-INV.net
WARNING : No END statement. file D:\ajy\04gateway\pseudo-cmos inverter\P-CMOS-INV.net
Spice file : D:\ajy\05expert\inv\inv_hier.spice

Preprocessing data ...
Comparing netlists ...

Comparing subcircuits "top" and "inv" ...

```

LVS RESULTS

```

First netlist : D:\ajy\04gateway\pseudo-cmos inverter\P-CMOS-INV.net
Second netlist : D:\ajy\05expert\inv\inv_hier.spice

netlists are EQUIVALENT

COMPARISON SUMMARY
device device before after
type model preprocessing preprocessing unatched matched parameter
#1 #2 #1 #2 #1 #2 #1 #2 #1 #2
NMOS ttt 4 7 4 4 0 0 4 0
total devices 4 7 4 4 0 0 4 0
total nets 6 9 6 6 0 0 6 0

lvs time: 00:00:00.1
version: 4.10.16.R (build 1843) (64-bit) (IE 101205)
created: Fri Sep 13 21:57:09 2024

```

LVS SETTINGS

```

Guardian message file : D:\ajy\04gateway\pseudo-cmos inverter\P-CMOS-INV\lvs\P-CMOS
Guardian filtered nodes file : D:\ajy\04gateway\pseudo-cmos inverter\P-CMOS-INV\lvs\P-CMOS
Guardian unmatched nodes file : D:\ajy\04gateway\pseudo-cmos inverter\P-CMOS-INV\lvs\P-CMOS
Guardian parameter error file : D:\ajy\04gateway\pseudo-cmos inverter\P-CMOS-INV\lvs\P-CMOS
Guardian parse error batch file : D:\ajy\04gateway\pseudo-cmos inverter\P-CMOS-INV\lvs\P-CMOS
Guardian port swapability file : D:\ajy\04gateway\pseudo-cmos inverter\P-CMOS-INV\lvs\P-CMOS

General Settings:
Use Local Matching off

```

8) 查看错误