Implementation of Broadband and High Efficiency S-band Doherty Power Amplifier Based on GaN HEMTs

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Abstract: In this work, based on Gallium Nitride (GaN) high electron mobility transistors (HEMTs), a high performance Doherty power amplifier (DPA) has been implemented. Specifically, fractional bandwidth of 24% at center frequency of 2 GHz, saturation output power of 263.876 Watts (54.214 dBm), and power added efficiency (PAE) of 54.874% have been successfully demonstrated. GaN HEMT was selected in DPA topology due to its strengths in high power operations and high thermal conductivity. Wide bandwidth was achieved by employing short stub at output of power combiner and low load impedance (25 Ohm) as well. Additional matches for resonance at second and third harmonics were implemented at output of both carrier PA and peak PA to achieve a better PAE. The designed DPA exhibited outstanding linearity with large input power level and showed excellent third input intermodulation point of 49 dBm.

Keywords: broad band, Doherty power amplifier, GaN, harmonics resonance, low load impedance pull

Introduction and Designing Idea

In modern transmitter of base stations, power amplifiers (PAs) with large saturation output power and good linearity are highly demanded to transmit sufficient power for wireless communications. Compared to conventional technologies based on Si LDMOS or GaAs, GaN HEMTs have been regarded as promising candidates for high power and high frequency applications owing to the superior material properties, such as high electron mobility in 2 dimensional electron gas (2-DEG), wide band gap, and high thermal conductivity [1]. Thus, PAs based on GaN HEMTs are expected to achieve ultra-high output power in RF bands. Doherty PA (DPA), first proposed in 1936, has garnered considerable research and industry interests in amplifiers designing due to its enhanced efficiency at back-off power ranges and acceptable linearity [2]. In addition to large saturation power and good linearity, output efficiency (power added efficiency (PAE) and drain efficiency) and bandwidth are also crucial for a PA with good performances. Besides, to work with a full interoperability within the modern communication systems, PAs should also perform well in several RF bands, such as frequency range of 1800 MHz to 2200 MHz, which includes long-term evolution (LTE) band 1 to 4 of frequency division duplexing (FDD) mode, and LTE band 34 to 37 of time division duplexing (TDD) mode [3]. Hence, designing a Doherty PA, based on GaN HEMTs, with wide bandwidth and high efficiency at a frequency range of 1800 to 2200 MHz becomes the key topic of this work.

Theoretical Analysis and Solutions

A. Operation Principle of Conventional Doherty PA

Fig. 1 Shows the topology of conventional Doherty PA (DPA), which contains two ways of PA, named as carrier PA and peak PA, respectively. Carrier PA is typically biased in Class A/AB, while peak PA is biased in Class C. At low input power

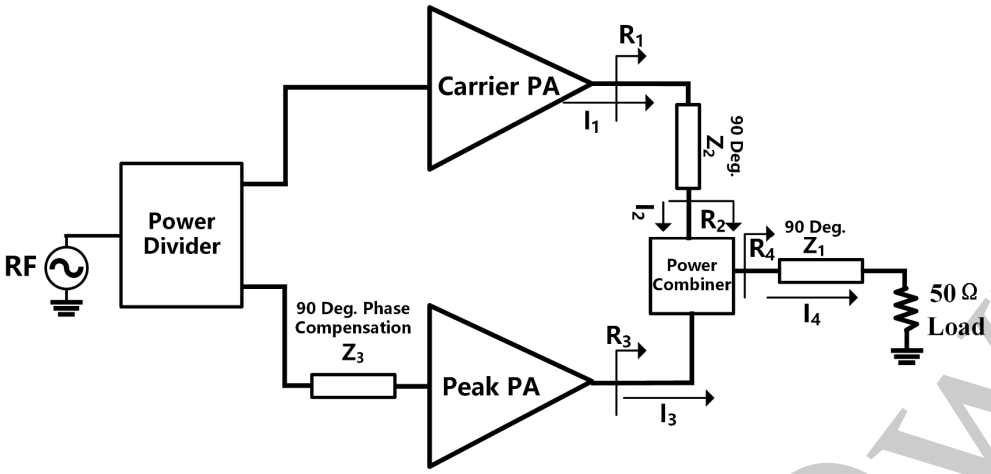


Fig.1. Conventional Doherty PA topology

level, carrier PA works in its active region, while peak PA is turned off because the instantaneous amplitude of the input signal is insufficient to overcome the negative class C bias and appears as open circuit. At medium input power levels, the carrier PA is saturated, whereas peak PA is turned on and operates in the active region. At high input power, both carrier amplifier and peak amplifier may reach their maximum efficiency. The 90 Degree transmission line with intrinsic impedance of Z_3 at the input of peak PA is used to compensate the phase difference between carrier way and peak way. The 90 Degree transmission line with intrinsic impedance of Z_2 at output of carrier PA is used to modulate the output impedance of carrier PA. And as a matter of fact, the modulation, also called as active load pull, represents a critical core part of DPA working principle and design. The specific operating principle of DPA comes as follows:

Consider the case that input power is divided equally into two ways of DPA using a power divider.

1. When working with large input power, the overall output power is the summation of power of peak PA and carrier PA, and they are equal to each other. Thus we have $I_1=I_3$. According to the theory of 90 Degree transformer of $Z_0=\sqrt{(Z_{in}Z_{out})}$ [4], The impedance seen in the input of power combiner can be written as:

$$R_2 = R_3 = \frac{I_2 + I_3}{I_2}\frac{{Z_1}^2}{50} = 2\frac{{Z_1}^2}{50}$$

Thus, load impedance of carrier PA can be derived as:

$$R_{1|high\_input} = \frac{50{Z_2}^2}{2{Z_1}^2}$$

2. When operating under low input power, peak PA is turned off, and all output power of DPA comes from carrier PA. In this case, $I_3=0$, and $R_2 = \frac{{Z_1}^2}{50}$. Thus, load impedance of carrier PA would be:

$$R_{1|low\_input} = \frac{50{Z_2}^2}{{Z_1}^2}$$

Which is twice times as that of large input case. Therefore, as input power increasing, load impedance of carrier PA would degrade from $R_{1|low\_input}$ to $R_{1|high\_input}$, and the load impedance of peak PA would degrade from infinity to $2\frac{{Z_1}^2}{50}$.

The higher load impedance under low power mode enables carrier PA to operate in pre-saturation region, where carrier PA has large efficiency. As increasing the input power, the degradation of load impedance would keep the operation state of carrier PA, while peak PA could work in linear region. Thus total efficiency of DPA would be typically larger than that of single stage PA biased in Class AB when operating in back-off power region.

B. Solutions for DPA with wide Bandwidth and High Efficiency

Usage of quarter-wavelength transformers would limit the output bandwidth. Typically, optimized output impedance (Z_{opt}) of a PA (without pre-match at output) has a relatively small real part, which means that there is a large mismatch between Z_{opt} and Z_{load} (50 Ohm). In this case, quarter-wavelength transformer (with intrinsic impedance of Z_0) used to match Z_{opt} and Z_{load} has small bandwidth. Fractional bandwidth of a quarter-wavelength transformer can be written as [4]:

$$\frac{\Delta f}{f_0} = 2 - \frac{4}{\pi}\cos^{-1}\left(\frac{\gamma_m}{\sqrt{1-\gamma_m{}^2}}\frac{2\sqrt{(Z_{in}Z_L)}}{|Z_L - Z_{in}|}\right)$$

Where γ_m is the acceptable reflection coefficient (typically -10 dB), Z_{in} the source impedance of transformer, Z_L the load impedance of transformer. Therefore, the smaller mismatch between Z_L and Z_{in} is, the wider bandwidth transformer will have. In this work, the carrier PA and peak PA of DPA were matched to 25 Ohm before the power combiner due to the optimized output impedance of carrier PA and peak PA were 6.995+j7.849 Ohm and 8.095+j2.999 Ohm, respectively. In addition, we employed a single short stub technology to improve the bandwidth further and obtain a flatter band behavior of DPA.

As for efficiency improvement, when matching output impedance of both PAs in DPA topology, we took harmonic into consideration. At the output of both PAs, second harmonic was shorted and third harmonic was opened. In this method, output signal would be much sharper, and PAs are more similar to working under Class F [5], which leads to a DPA with higher efficiency.

Fig. 2 illustrates the specific topology of our design for DPA with wide bandwidth and high efficiency. Z_{CL}, Z_{PL}, Z_{CS}, and Z_{PS} are the optimized load impedance and source impedance obtained from source and load pull respectively. Output of PAs are matched to 25 Ohm system. A shorted quarter-wavelength transmission line with intrinsic impedance of 12.5 Ohm is employed to expand bandwidth. The following 25 Ohm transformer transfers 25 Ohm system to 50 Ohm standard load. At output of peak PA, there is a 25 Ohm offset line to ensure the output impedance of peak PA is large enough (transfer output impedance to open point in Smith Chart) when operating in small input power [6]. Moreover, 25 Ohm offset line at output of carrier PA and 50 Ohm phase compensation line are used to align phases of two ways.

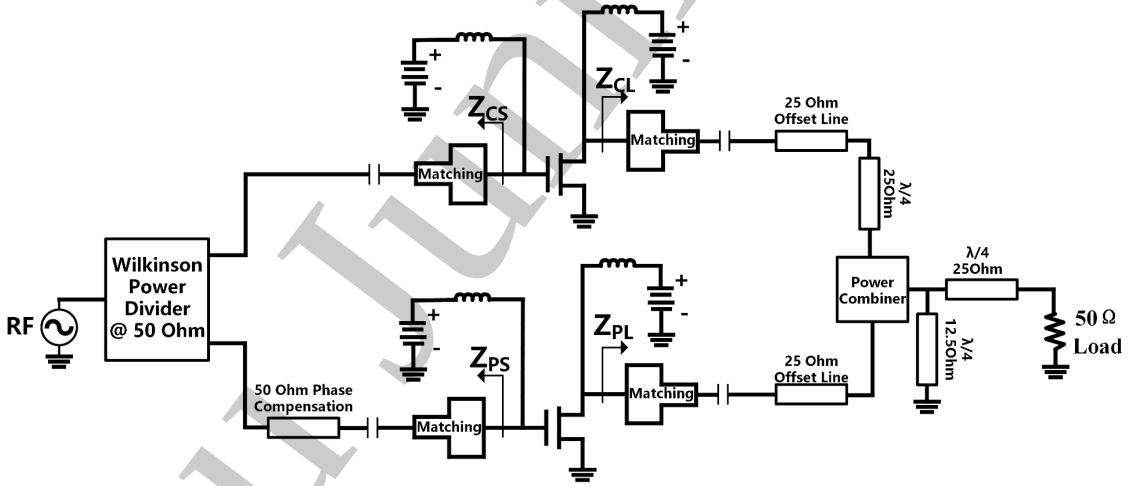


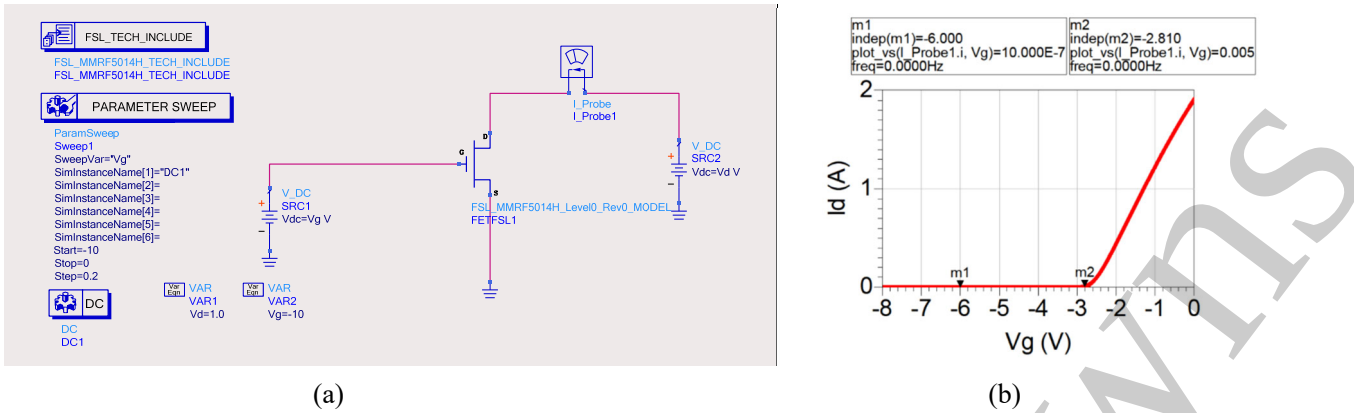
Fig.2. Our solution for DPA with wide bandwidth and high efficiency

Design Flow and Results

A. Selections of Quiescent DC Bias Point for Both Class AB and Class C PA

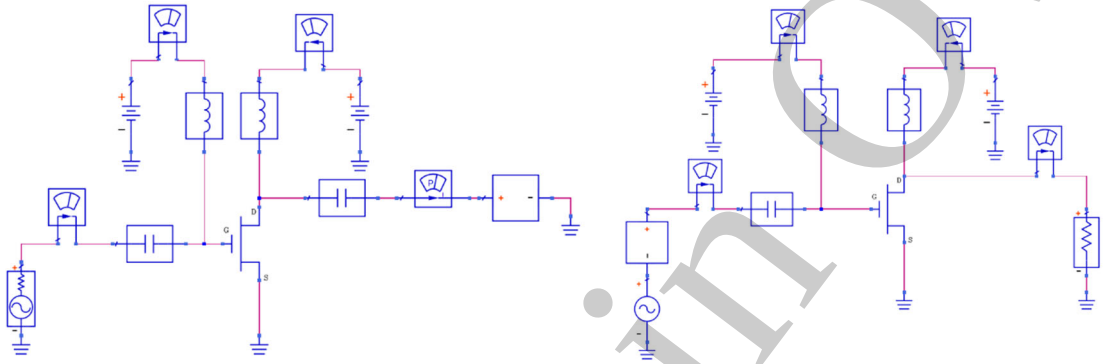
GaN based FSL_MMRF5014H HEMT model [7] was employed as both carrier PA and peak PA in Advanced Design System (ADS) simulation. The threshold voltage of the transistor was -3 V. **Fig. 3(a)** shows the DC simulation schematic and transfer characteristics of GaN HEMT. Quiescent DC Bias points on Gate terminals of carrier PA and peak PA were -2.75 V

and -6 V, respectively. Drain bias of both transistors were set as 55V.



(a) (b)

Fig.3. (a) DC simulation schematic, (b) transfer characteristics of GaN HEMT

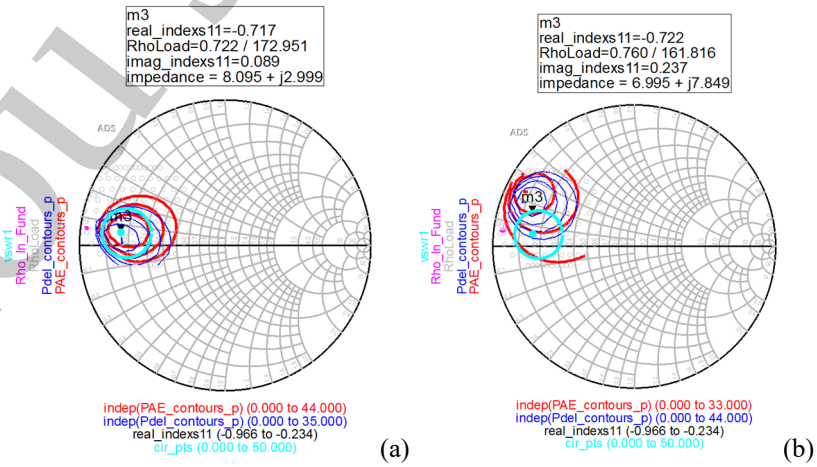


(a) (b)

Fig.4. (a) Schematic of load pull simulation, (b) schematic of source pull simulation.

B. Selections of Optimized Input and Output Impedance for Both PAs

When designing the PA, a question that no one could bypass is to locate the optimized load point in smith-chart. The optimized load impedance is not necessarily the point with maximum output power and maximum efficiency. The selection of load impedance must take efficiency, power and gain all into account. **Fig. 4** shows the schematic for source pull and load pull simulation. When the first load impedance point was determined, a suitable input impedance point should be chosen to get a better output performance. Several iterations of load pull and source pull have been carried out to obtain a best balance between output power gain and power added efficiency (PAE), defined as Gain = dB(P_{out}-P_{in}) and PAE = (P_{out}-P_{in})/P_{DC}*100%.



(a) (b)

Fig.5. (a) Load pull solution for peak PA, (b) load pull solution for carrier PA

Fig. 5 shows the results of load pull simulation for both carrier and peak PA. Optimized load impedance for peak PA and carrier PA were determined to be 6.995+j7.849 Ohm and 8.095+j2.999 Ohm, respectively. Optimized source impedance for peak PA and carrier PA were determined to be 2.6-j3.5 Ohm and 4.7-j9.6 Ohm, respectively.

C. Design of Matching Network for Both PAs

Micro-strip lines and capacitors with high Q were employed to match the input and output impedance. Here, Murata capacitor and inductor models are used to represent the non-ideal circuit with parasitics, and the layout design is completed through the built-in electromagnetic field simulation tool. S-parameters simulations were done to verify the matching networks. The simulation setup and results for input network of carrier PA are illustrated in **Fig. 6**. Other matching network designs are shown in the **Appendix II**. When matching the output impedance, second harmonic was matched to be short and third harmonic was matched to be open.

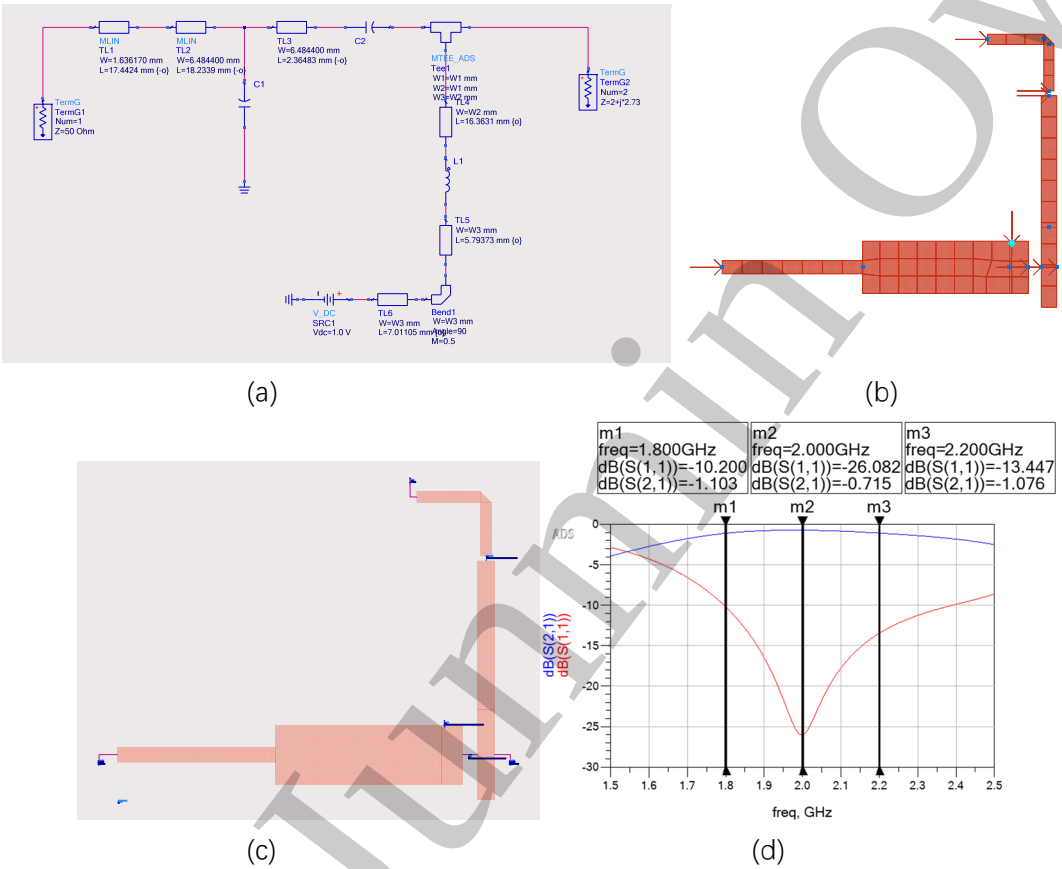


Fig.6. (a) Schematic of input matching network, (b) EM model for the schematic, (c) layout simulation, (d) S-parameters verification.

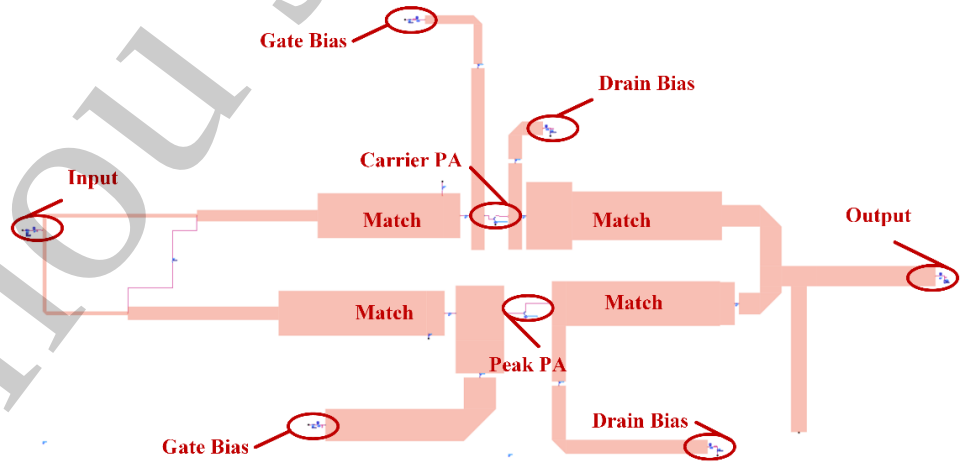


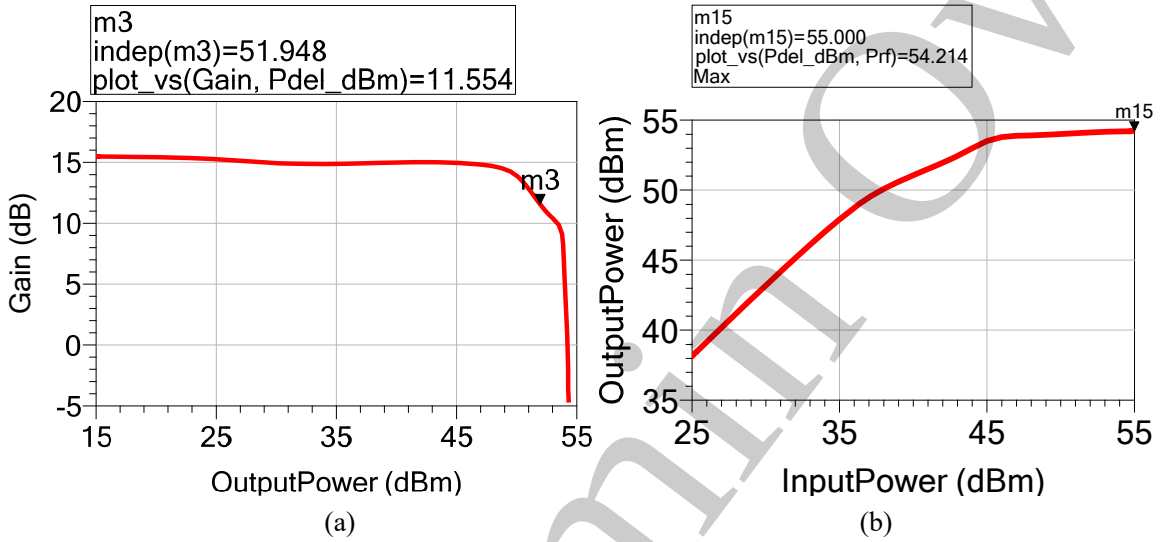
Fig.7. View of layout test bench for DPA

D. Design of Other Passive Networks in DPA

In this work, Wilkinson power divider, at 50 Ohm standard, was employed to divide the input signal equally into two ways of DPA for balancing and efficiency. Phase compensation transmission line was designed with 50 Ohm intrinsic impedance, while offset lines at output of two PAs were designed with 25 Ohm intrinsic impedance. In addition, the short stub at output was designed with 12.5 Ohm intrinsic impedance. **Fig. 7** shows the overall view of layout for the DPA.

E. DPA Performances

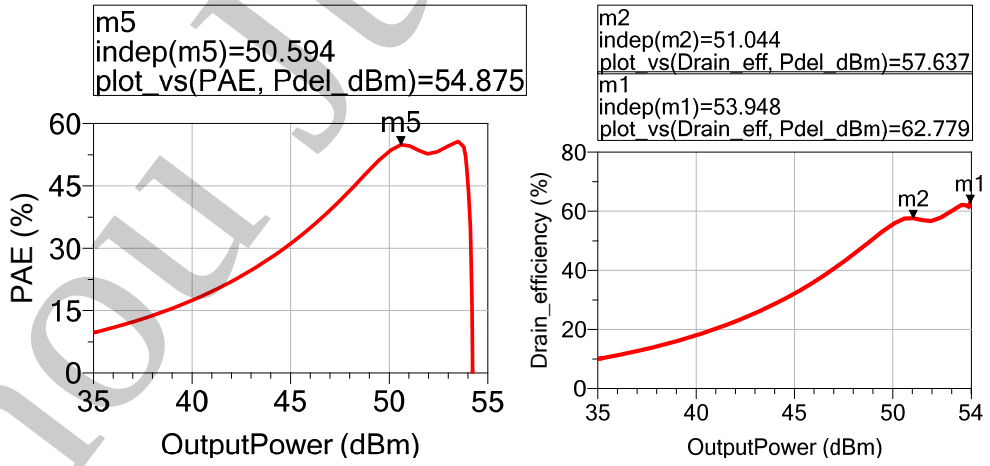
In this part, all the simulation results come from the layout simulation of DPA, which contain parasitics of the circuit. Peak PA was biased -6 V at gate and 55 V at drain, while carrier PA was biased -2.81 V at gate and 55 V at drain. Input power was divided equally into two ways of DPA.



(a) (b)

Fig.8. (a) Gain versus output power (b) output power versus input power

Fig. 8 shows the gain versus output power level in (a) and output power versus input power level in (b). The DPA achieved 3-dB power compression at output power level of **51.948 dBm** (**156.603 Watts**), and the saturation power can be derived as **54.214 dBm** (**263.876 Watts**) from **Fig. 8(b)**. In addition, uniform gain can be observed when output power is smaller than 45 dBm.



(a) (b)

Fig. 9. (a) PAE versus output power, (b) Drain efficiency versus output power

Fig. 9 shows the PAE and drain efficiency (P_{out}/P_{DC}*100%) with output power level. Back-off PAE is larger than 50% when output power level is larger than 49 dBm, and the maximum PAE reaches **54.875%**. The corresponding maximum drain

efficiency of DPA hits **62.779%**.

Fig. 10 shows the bandwidth of DPA with center frequency of 2 GHz. With low load impedance and shorted stub technology,

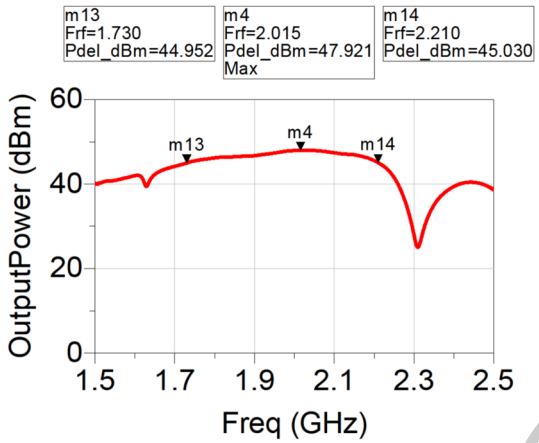


Fig. 10. Output power versus input frequency of DPA. This was simulated when input power level was 35 dBm, where DPA was operating in linear region.

3-dB bandwidth of DPA is over 480MHz. The corresponding fractional bandwidth ($BW_{frac}=(f_{MAX}-f_{MIN})/f_{center}*100\%$) is larger than **24%**.

Despite the fact that good linearity has been evidently observed in **Fig. 8(a)**, two tones nonlinear simulation was also done to get IMD3 of the DPA. The results are shown in **Fig. 11**. Two tones signal were fed into DPA with frequencies of 1895 MHz and 2005 MHz. The measured third order input intermodulation point (IIP3) was **49 dBm**, which shows exceptional and practically usable linearity of DPA.

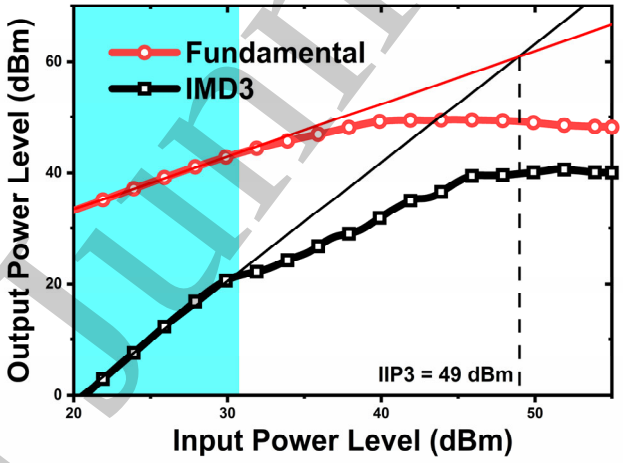


Fig. 11. Results of two tones nonlinear simulation.

Conclusion

We have implemented a DPA, based on GaN HEMTs, with fractional bandwidth of 24% at center frequency of 2 GHz, saturation output power of 263.876 Watts (54.214 dBm), and PAE of 54.874% in this work. Wide bandwidth was achieved by employing short stub at output of power combiner and lower load impedance (25 Ohm) as well. Additional matches for resonance at second and third harmonics were implemented at output of both carrier PA and peak PA to achieve a higher PAE. The designed DPA has great linearity in large input power level and it shows exceptional value of IIP3 at 49 dBm.

References

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Appendix I

Technical Data for DPA Implemented in This Work

Typical wide band Performance

Frequency (MHz)	Signal Type	P_{out} (dBm)	PAE	G_p (dB)	Drain eff.	Fractional BW
1800-2200	CW	50.5 (CW)	54.80%	15	62.78 %	24%

Nonlinear Performance

Frequency (MHz)	Test Method	$P_{3\text{-}dB}$ (dBm)	P_{sat} (dBm)	IIP3 (dBm)
2000	2 Tones Test	51.9	54.2	49

Schematic Parameters

Terminal	Bias Voltage (V)
Gate of carrier PA	-2.81
Drain of carrier PA	55
Gate of peak PA	-6
Drain of peak PA	55

Source/Load Pull Points

Source impedance of carrier PA	4.7-j9.6 Ohm
Load impedance of carrier PA	8.1+j3.0 Ohm
Source impedance of peak PA	2.6-j3.5 Ohm
Load impedance of peak PA	7.0+j7.8 Ohm

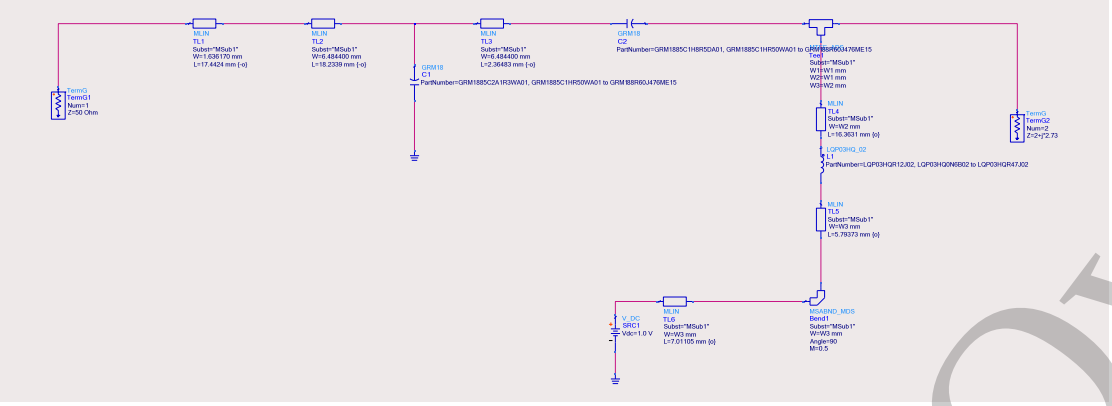
Appendix II

Content

Match Circuit

Carrier input match

Schematic:



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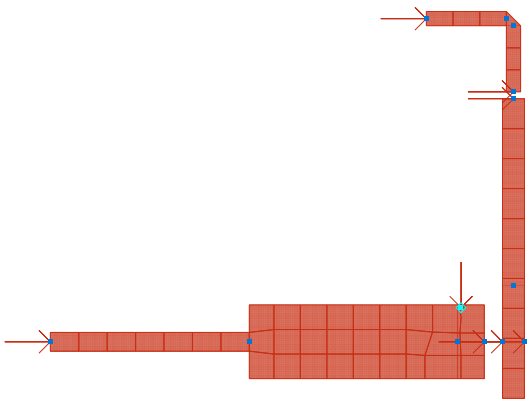

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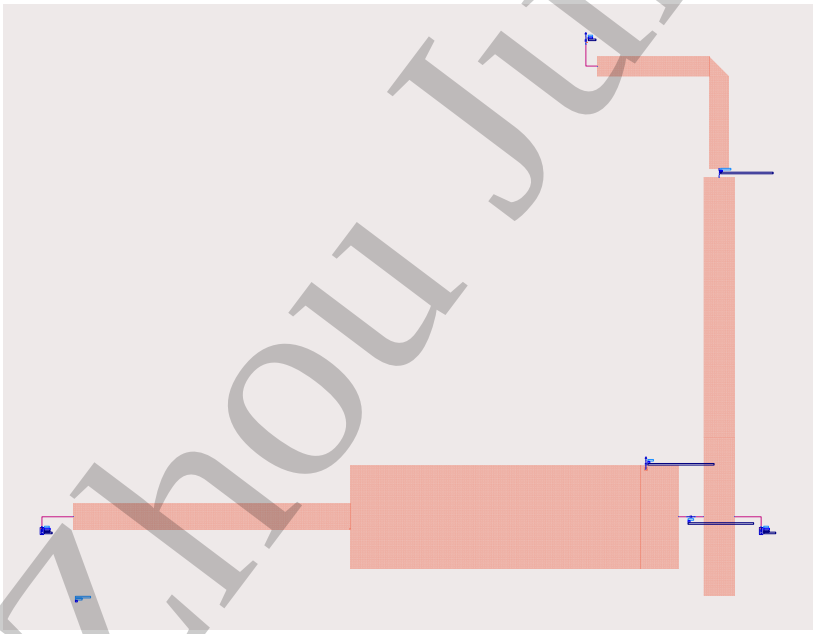

Carrier output match

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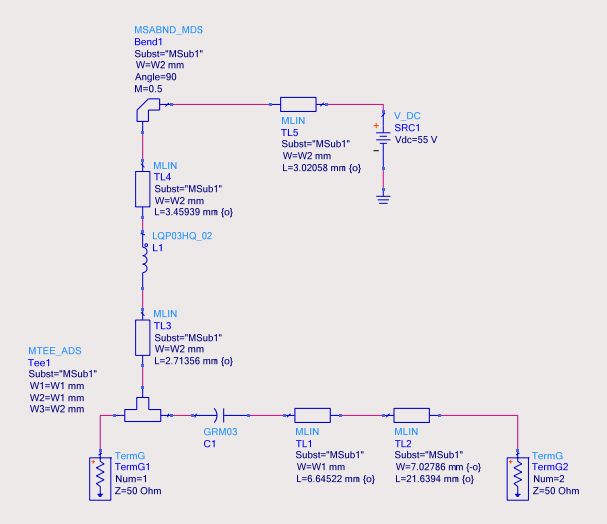

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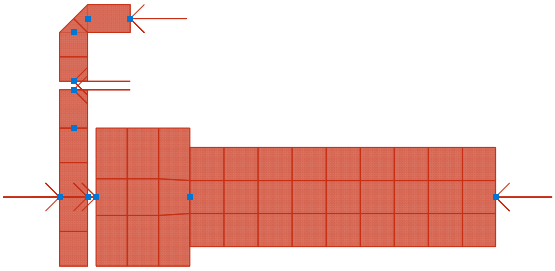

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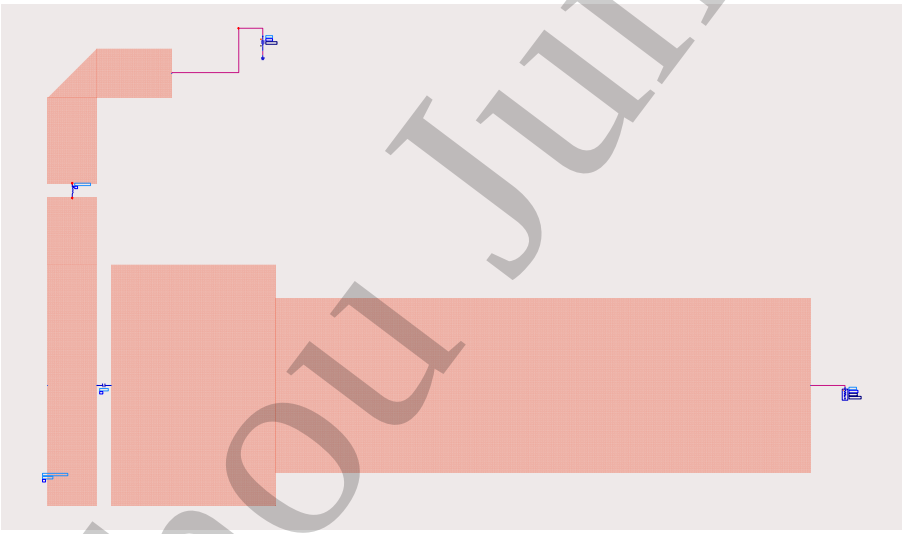

Peak input match

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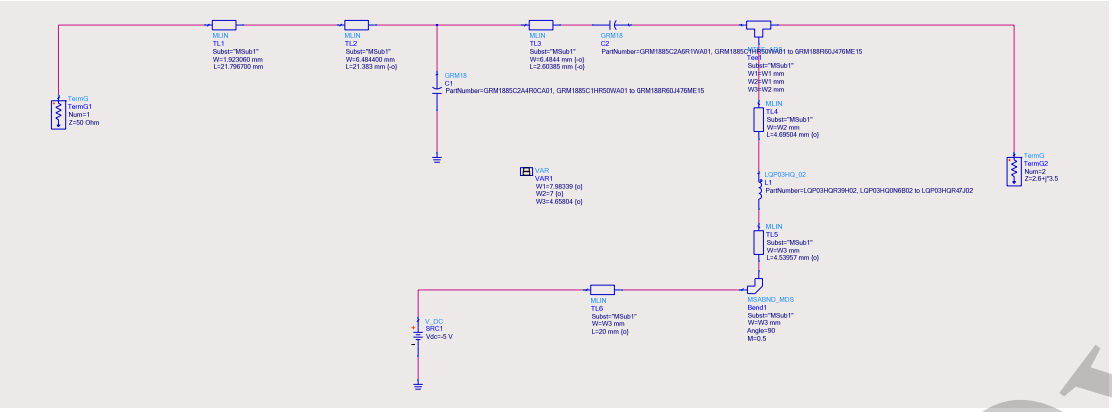

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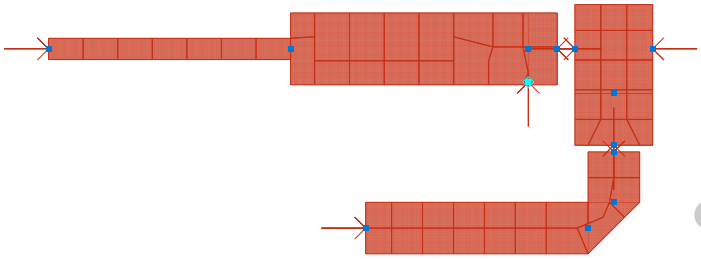

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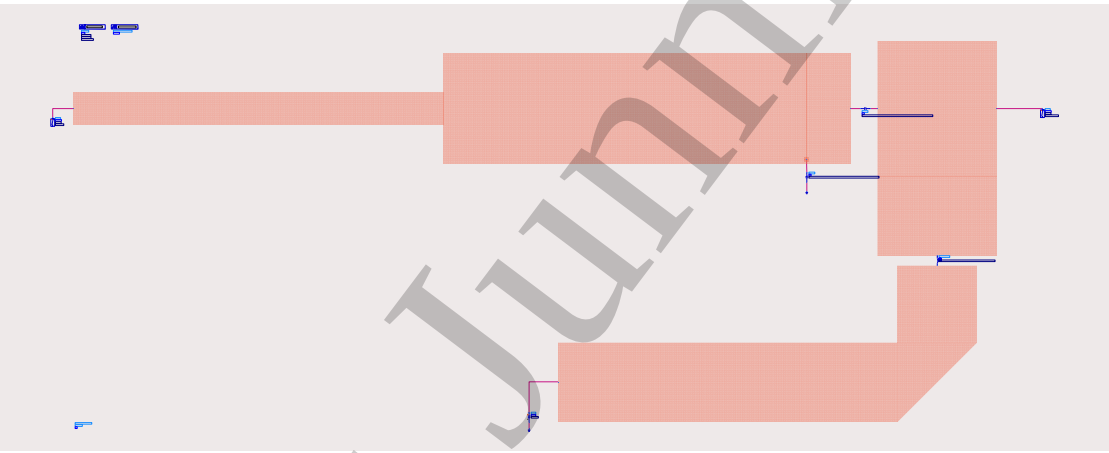

Peak output match

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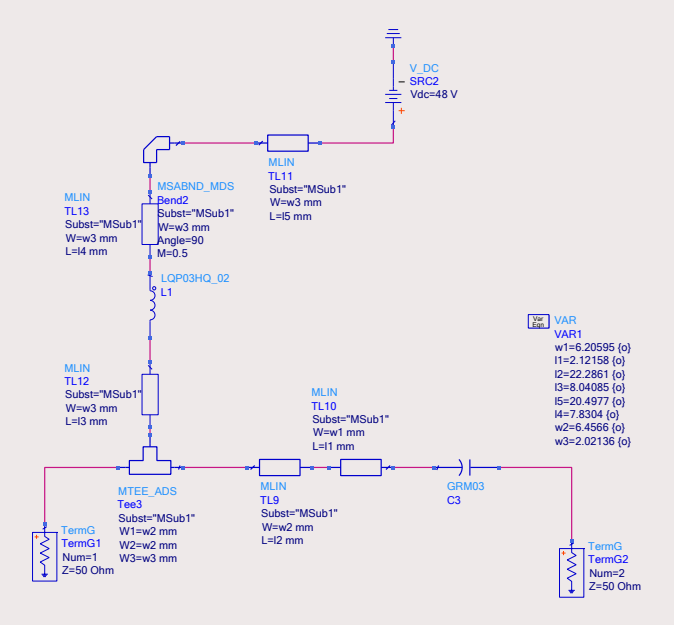

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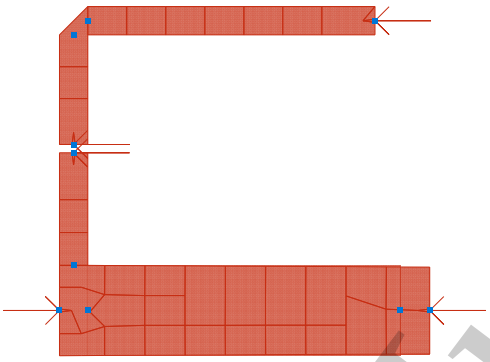
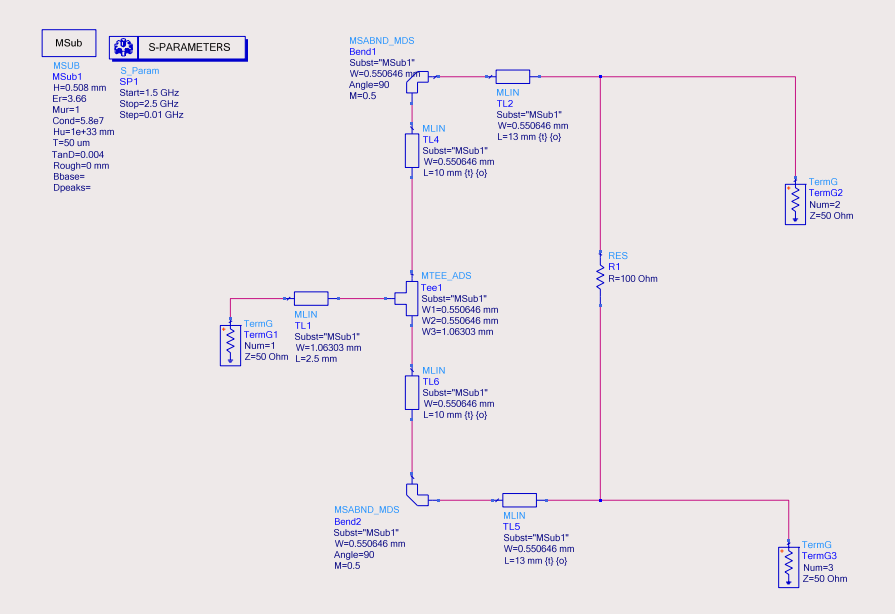


Power divider

Schematic:



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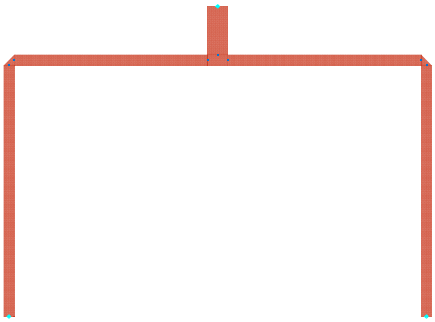

Combiner and Offset-line

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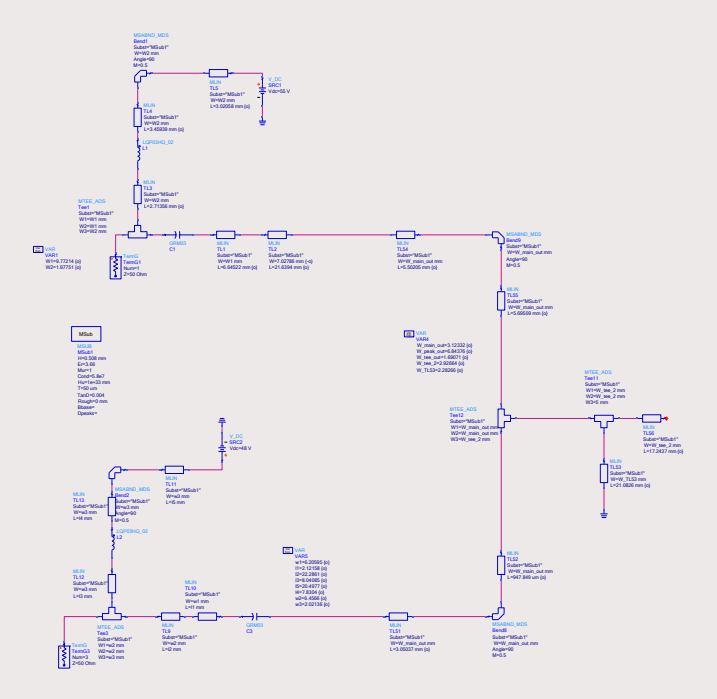

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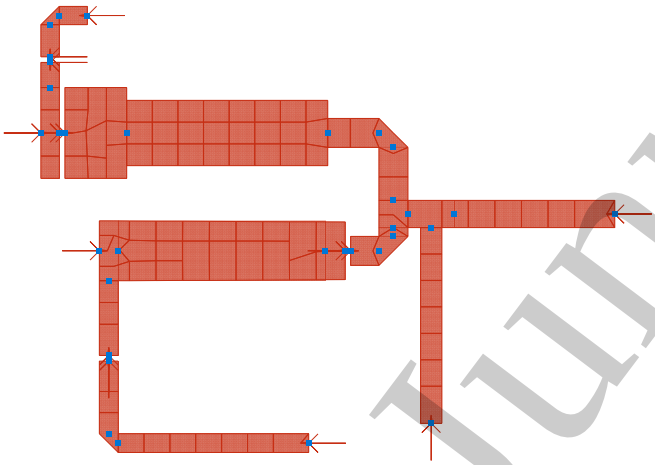
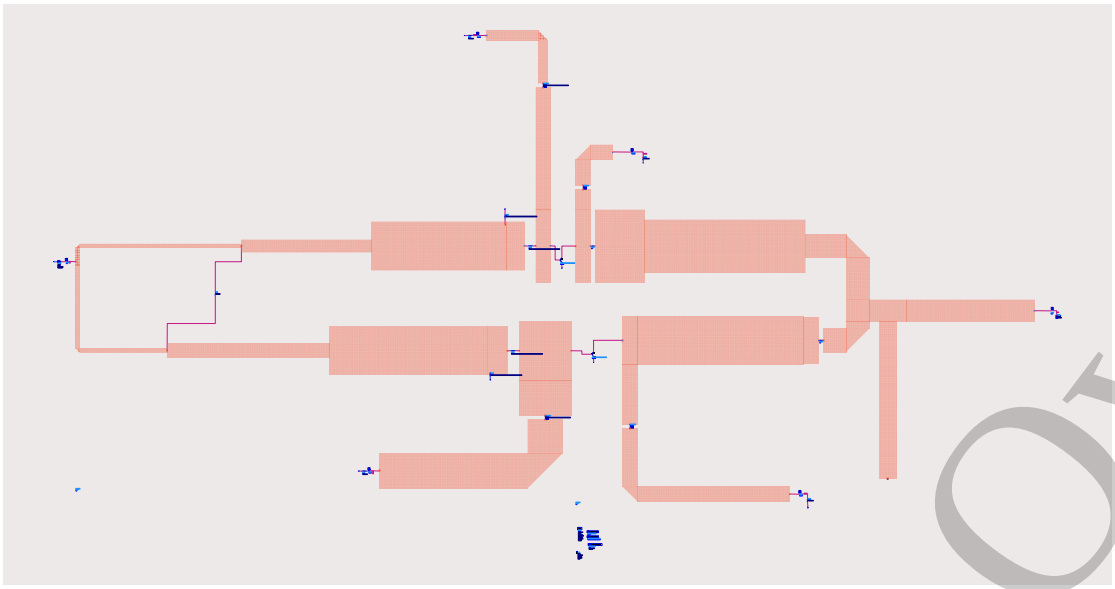


Overall Design:

Schematic:



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