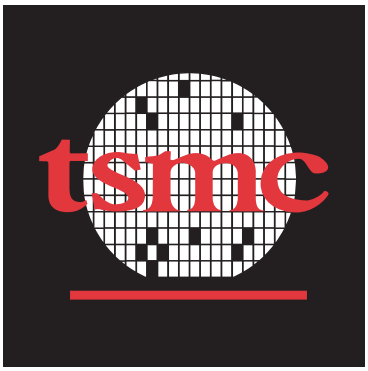

TPHN02P_075OD12GPIO
TSMC 2nm
Standard I/O Library

Databook

Version 100A
March 25, 2025

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Table of Contents

1 Introduction

This databook provides basic information about the *TPHN02P_075OD12GPIO Standard I/O* library.

The *TPHN02P_075OD12GPIO* library is designed to optimize I/O performance with core voltage of *0.75V* in typical case, and I/O voltage of *1.2V* in typical case in the *TSMC 2nm 0.75V/1.2V process*. Design engineers can refer to this document for DC characteristics, cell availability, cell descriptions, datasheets, and so on.

2 Electrical Characteristics

2.1 DC Characteristics

For section 2.1, refer to table 2.7 for the list of PVT conditions used to determine min and max values.

2.1.1 Recommended Operating Conditions

Warning: Permanent damage could occur if the operation exceeds the ranges listed in Table 2.1.

Table 2.1: Recommended Operating Conditions

Parameter		Min.	Nom.	Max.	Units
V_{DD}	Pre-Driver Voltage	*0.675*	*0.75*	*0.825*	V
V_{DDPST}	Post-Driver Voltage	*1.08*	*1.2*	*1.32*	V
T_J	Junction Temperature	*-40*	*25*	*125*	^{o}C
V_{IMAX}	Maximum Input Voltage			*VDDIO+0.3*	V
$VDD_{ramp-upslew}$	Ramp up slew for VDD			*0.018*	V/us
$VDDIO_{ramp-upslew}$	Ramp up slew for VDDIO			*0.018*	V/us

(*) The Vimax is not for DC signal level, but just for a reference of over-shoot/under-shoot, no guarantee of electrical spec and reliability.

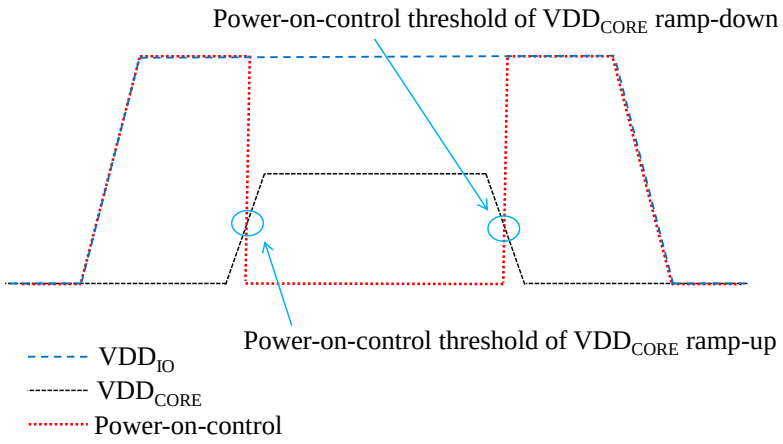


Figure 2.1: POC illustration

Table 2.2: Power-On-Control Threshold

(This_PVT: IDDQ_0P825V_0P880V_1P320V_0P360V_125C_TYPICAL)

Parameter	Min.	This_PVT	Max.	Units
Power-On-Control threshold of VDD ramp-up(pvdd12codpoc_v)	0.329	0.378	0.395	V
Power-On-Control threshold of VDD ramp-down(pvdd12codpoc_v)	0.311	0.356	0.378	V
Power-On-Control threshold of VDD ramp-up(pvdd12codpoc_h)	0.329	0.378	0.395	V
Power-On-Control threshold of VDD ramp-down(pvdd12codpoc_h)	0.311	0.356	0.378	V

Table 2.3: DC Characteristics for PRWDWUWSWEWCODCDGH

(This_PVT: IDDQ_0P825V_0P880V_1P320V_0P360V_125C_TYPICAL)

Parameter	Min.	This_PVT	Max.	Units	
VIL	*-0.3*		*0.35*VDDIO*	V	Input Low Voltage
VIH	*0.65*VDDIO*		*VDDIO+0.3*	V	Input High Voltage
VT	*0.53*	*0.66*	*0.66*	V	Threshold Point
VT+	*0.61*	*0.76*	*0.76*	V	Schmitt Trigger Low to High Threshold Point
VT-	*0.48*	*0.53*	*0.53*	V	Schmitt Trigger High to Low Threshold Point
VTPU	*0.53*	*0.66*	*0.66*	V	Threshold Point with Pull-up Resistor Enabled

VTPD	*0.53*	*0.66*	*0.66*	V	Threshold Point with Pull-down Resistor Enabled
VTPU+	*0.61*	*0.76*	*0.76*	V	Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled
VTPU-	*0.48*	*0.53*	*0.53*	V	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled
VTPD+	*0.61*	*0.76*	*0.76*	V	Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled
VTPD-	*0.48*	*0.53*	*0.53*	V	Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled
I			$\pm 10\mu$	A	Input Leakage Current @ V_I=*1.2V* or 0V
IOZ			$\pm 10\mu$	A	Tri-state Output Leakage Current @ V_O=*1.2V* or 0V
RPU	*19k*	*19k*	*28k*	Ω	Pull-up Resistor
RPD	*16k*	*16k*	*22k*	Ω	Pull-down Resistor
VOL			*0.25*VDDIO*	V	Output Low Voltage
VOH	*0.75*VDDIO*			V	Output High Voltage

(*) The max. VIH and min. VIL is not for DC signal level, but just for a reference of over-shoot/under-shoot, no guarantee of electrical spec and reliability.

IOL/IOH	**Min.**	**This_PVT**	**Max.**	**Units**
IOL Low Level Output Current @V_{OL}(max)				
(DS2,DS1,DS0) = '000'	*1.4*	*3.0*	*3.4*	mA
(DS2,DS1,DS0) = '001'	*2.8*	*5.9*	*6.7*	mA
(DS2,DS1,DS0) = '010'	*4.3*	*8.9*	*10.1*	mA
(DS2,DS1,DS0) = '011'	*5.7*	*11.7*	*13.4*	mA
(DS2,DS1,DS0) = '100'	*7.1*	*14.7*	*16.7*	mA
(DS2,DS1,DS0) = '101'	*8.5*	*17.5*	*19.9*	mA
(DS2,DS1,DS0) = '110'	*9.8*	*20.1*	*22.9*	mA
(DS2,DS1,DS0) = '111'	*11.2*	*22.8*	*26.1*	mA
IOH High Level Output Current @V_{OH}(min)				
(DS2,DS1,DS0) = '000'	*1.9*	*6.5*	*7.5*	mA

(DS2,DS1,DS0) = '001'	*3.7*	*12.9*	*15.0*	mA
(DS2,DS1,DS0) = '010'	*5.5*	*19.1*	*22.3*	mA
(DS2,DS1,DS0) = '011'	*7.3*	*25.2*	*29.5*	mA
(DS2,DS1,DS0) = '100'	*9.1*	*31.2*	*36.6*	mA
(DS2,DS1,DS0) = '101'	*10.9*	*37.3*	*43.7*	mA
(DS2,DS1,DS0) = '110'	*12.7*	*43.1*	*50.6*	mA
(DS2,DS1,DS0) = '111'	*14.5*	*48.8*	*57.5*	mA

Table 2.5: DC Characteristics for PRWDWUWSWEWCODCDGSH

(This_PVT: IDDQ_0P825V_0P880V_1P320V_0P360V_125C_TYPICAL)

Parameter	**Min.**	**This_PVT**	**Max.**	**Units**	
VIL	*-0.3*		*0.35*VDDIO*	V	Input Low Voltage
VIH	*0.65*VDDIO*		*VDDIO+0.3*	V	Input High Voltage
VT	*0.53*	*0.66*	*0.66*	V	Threshold Point
VT+	*0.61*	*0.76*	*0.76*	V	Schmitt Trigger Low to High Threshold Point
VT-	*0.48*	*0.53*	*0.53*	V	Schmitt Trigger High to Low Threshold Point
VTPU	*0.53*	*0.66*	*0.66*	V	Threshold Point with Pull-up Resistor Enabled
VTPD	*0.53*	*0.66*	*0.66*	V	Threshold Point with Pull-down Resistor Enabled
VTPU+	*0.61*	*0.76*	*0.76*	V	Schmitt Trigger Low to High Threshold Point with Pull-up Resistor Enabled
VTPU-	*0.48*	*0.53*	*0.53*	V	Schmitt Trigger High to Low Threshold Point with Pull-up Resistor Enabled
VTPD+	*0.61*	*0.76*	*0.76*	V	Schmitt Trigger Low to High Threshold Point with Pull-down Resistor Enabled
VTPD-	*0.48*	*0.53*	*0.53*	V	Schmitt Trigger High to Low Threshold Point with Pull-down Resistor Enabled

VTSPU	*0.53*	*0.66*	*0.66*	V	Threshold Point with Strong Pull-up Resistor Enabled
VTSPU+	*0.61*	*0.76*	*0.76*	V	Schmitt Trigger Low to High Threshold Point with Strong Pull-up Resistor Enabled
VTSPU-	*0.48*	*0.53*	*0.53*	V	Schmitt Trigger High to Low Threshold Point with Strong Pull-up Resistor Enabled
I			$\pm 10\mu$	A	Input Leakage Current @ V_I=*1.2V* or 0V
IOZ			$\pm 10\mu$	A	Tri-state Output Leakage Current @ V_O=*1.2V* or 0V
RSPU	*2.1k*	*2.2k*	*3.1k*	Ω	Strong Pull-up Resistor
RPU	*19k*	*19k*	*28k*	Ω	Pull-up Resistor
RPD	*16k*	*16k*	*23k*	Ω	Pull-down Resistor
VOL			*0.25*VDDIO*	V	Output Low Voltage
VOH	*0.75*VDDIO*			V	Output High Voltage

(*) The max. VIH and min. VIL is not for DC signal level, but just for a reference of over-shoot/under-shoot, no guarantee of electrical spec and reliability.

IOL/IOH	**Min.**	**This_PVT**	**Max.**	**Units**
IOL Low Level Output Current @V_{OL}(max)				
(DS3,DS2,DS1,DS0) = '0000'	*1.4*	*3.0*	*3.4*	mA
(DS3,DS2,DS1,DS0) = '0001'	*2.8*	*5.9*	*6.7*	mA
(DS3,DS2,DS1,DS0) = '0010'	*4.3*	*8.9*	*10.1*	mA
(DS3,DS2,DS1,DS0) = '0011'	*5.7*	*11.7*	*13.4*	mA
(DS3,DS2,DS1,DS0) = '0100'	*7.1*	*14.6*	*16.6*	mA
(DS3,DS2,DS1,DS0) = '0101'	*8.4*	*17.4*	*19.9*	mA
(DS3,DS2,DS1,DS0) = '0110'	*9.8*	*20.0*	*22.9*	mA
(DS3,DS2,DS1,DS0) = '0111'	*11.1*	*22.8*	*26.1*	mA
(DS3,DS2,DS1,DS0) = '1000'	*12.9*	*26.4*	*30.3*	mA
(DS3,DS2,DS1,DS0) = '1001'	*14.3*	*29.2*	*33.4*	mA
(DS3,DS2,DS1,DS0) = '1010'	*15.7*	*32.1*	*36.8*	mA
(DS3,DS2,DS1,DS0) = '1011'	*17.1*	*34.8*	*39.9*	mA
(DS3,DS2,DS1,DS0) = '1100'	*18.4*	*37.4*	*43.0*	mA
(DS3,DS2,DS1,DS0) = '1101'	*19.7*	*40.1*	*46.0*	mA
(DS3,DS2,DS1,DS0) = '1110'	*21.0*	*42.6*	*49.0*	mA
(DS3,DS2,DS1,DS0) = '1111'	*22.3*	*45.2*	*52.1*	mA

IOH High Level Output Current @V_{OH}(min)				
(DS3,DS2,DS1,DS0) = '0000'	*1.9*	*6.5*	*7.5*	mA
(DS3,DS2,DS1,DS0) = '0001'	*3.7*	*12.9*	*15.0*	mA
(DS3,DS2,DS1,DS0) = '0010'	*5.5*	*19.1*	*22.3*	mA
(DS3,DS2,DS1,DS0) = '0011'	*7.3*	*25.2*	*29.5*	mA
(DS3,DS2,DS1,DS0) = '0100'	*9.1*	*31.3*	*36.6*	mA
(DS3,DS2,DS1,DS0) = '0101'	*10.9*	*37.4*	*43.8*	mA
(DS3,DS2,DS1,DS0) = '0110'	*12.7*	*43.2*	*50.7*	mA
(DS3,DS2,DS1,DS0) = '0111'	*14.5*	*48.9*	*57.6*	mA
(DS3,DS2,DS1,DS0) = '1000'	*16.2*	*54.3*	*64.0*	mA
(DS3,DS2,DS1,DS0) = '1001'	*18.0*	*60.1*	*70.9*	mA
(DS3,DS2,DS1,DS0) = '1010'	*19.7*	*65.5*	*77.5*	mA
(DS3,DS2,DS1,DS0) = '1011'	*21.5*	*71.0*	*84.0*	mA
(DS3,DS2,DS1,DS0) = '1100'	*23.2*	*76.2*	*90.4*	mA
(DS3,DS2,DS1,DS0) = '1101'	*24.9*	*81.7*	*97.0*	mA
(DS3,DS2,DS1,DS0) = '1110'	*26.6*	*86.8*	*103.2*	mA
(DS3,DS2,DS1,DS0) = '1111'	*28.3*	*92.0*	*109.5*	mA

2.1.2 Characterization Conditions

Table 2.7: Characterization Conditions

Corner	Condition
TT_0P750V_0P800V_1P200V_0P400V_85C_TYPICAL	*VDD_{CORE} = 0.75V* *VDD_{IO} = 1.2V* *Temperature = 85°C* *Device Name = TTMacro_MOS_MOSCAP, TT_RES_DISRES, TT_BIP_DIO, TT_R_METAL, TYPICAL_MOM*
SSGNP_0P675V_0P720V_1P080V_0P440V_125C_CWORST_CCWORST_T	*VDD_{CORE} = 0.675V* *VDD_{IO} = 1.08V* *Temperature = 125°C* *Device Name = SSGNPGlobal-Corner_LocalMC_MOS_MOSCAP, SS_RES_DISRES, SS_BIP_DIO, SS_R_METAL, CWORST_MOM*

SSGNP_0P675V_0P720V_1P080V_0P440V_0C_CWORST_CCWORST_T	VDD_{CORE} = 0.675V VDD_{IO} = 1.08V Temperature = 0°C Device Name = SSGNPGlobal-Corner_LocalMC_MOS_MOSCAP, SS_RES_DISRES, SS_BIP_DIO, SS_R_METAL, CWORST_MOM
TT_0P750V_0P800V_1P200V_0P400V_25C_TYPICAL	VDD_{CORE} = 0.75V VDD_{IO} = 1.2V Temperature = 25°C Device Name = TTMacro_MOS_MOSCAP, TT_RES_DISRES, TT_BIP_DIO, TT_R_METAL, TYPICAL_MOM
SSGNP_0P675V_0P720V_1P080V_0P440V_M40C_CWORST_CCWORST_T	VDD_{CORE} = 0.675V VDD_{IO} = 1.08V Temperature = -40°C Device Name = SSGNPGlobal-Corner_LocalMC_MOS_MOSCAP, SS_RES_DISRES, SS_BIP_DIO, SS_R_METAL, CWORST_MOM
IDDQ_0P825V_0P880V_1P320V_0P360V_125C_TYPICAL	VDD_{CORE} = 0.825V VDD_{IO} = 1.32V Temperature = 125°C Device Name = IDDQ_MOS_MOSCAP, FF_RES_DISRES, FF_BIP_DIO, FF_R_METAL, CBEST_MOM
FFGNP_0P825V_0P880V_1P320V_0P360V_125C_CBEST_CCBEST_T	VDD_{CORE} = 0.825V VDD_{IO} = 1.32V Temperature = 125°C Device Name = FFGNPGlobal-Corner_LocalMC_MOS_MOSCAP, FF_RES_DISRES, FF_BIP_DIO, FF_R_METAL, CBEST_MOM
FFGNP_0P825V_0P880V_1P320V_0P360V_0C_CBEST_CCBEST_T	VDD_{CORE} = 0.825V VDD_{IO} = 1.32V Temperature = 0°C Device Name = FFGNPGlobal-Corner_LocalMC_MOS_MOSCAP, FF_RES_DISRES, FF_BIP_DIO, FF_R_METAL, CBEST_MOM
FFGNP_0P825V_0P880V_1P320V_0P360V_M40C_CBEST_CCBEST_T	VDD_{CORE} = 0.825V VDD_{IO} = 1.32V Temperature = -40°C Device Name = FFGNPGlobal-Corner_LocalMC_MOS_MOSCAP, FF_RES_DISRES, FF_BIP_DIO, FF_R_METAL, CBEST_MOM

2.2 Timing Information

2.2.1 Transition Time

Characterization is based on a "10-90" method; that is, the 10% and 90% points of the full output swing are used to define the rise and fall transition as illustrated in Figure 2.2. Please refer to the Synopsys *.lib* file for details.

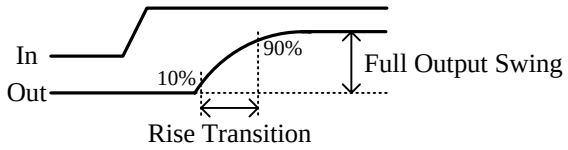


Figure 2.2: The Transition Time

2.2.2 Propagation Delay

Two different propagation delays, tp_{LH} and $tp_{HL,}$ represent the state change delay for low to high and from high to low transitions.

The propagation delay is measured from the 50% point of the input waveform to the 50% point of the output waveform as shown in Figure 2.3.

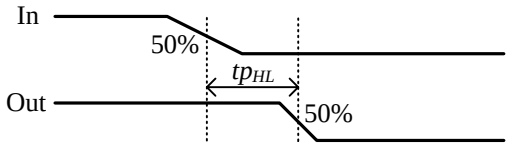


Figure 2.3: The Propagation Delay

3 Cell Descriptions

This chapter provides cell list along with cell descriptions for the TSMC *TPHN02P_075OD12GPIO* library.

Table 3.1: Cell Descriptions

Cell Name	Functional Description
PCLAMPCCOD_H	*Power clamp cell for core voltage*
PCLAMPCCOD_V	*Power clamp cell for core voltage*
PCLAMPCOD_V	*Power clamp cell for 1.2V*
PCORNERCOD_V	*Corner cell*
PDB2CODANA_H	*Analog signal cell, compatible to be used in digital IO domain*
PDB2CODANA_V	*Analog signal cell, compatible to be used in digital IO domain*
PDCAPR12COD06240_H	*Filler Cell with DECAP between VDDPST12 and VSS*
PDCAPR12COD06240_V	*Filler Cell with DECAP between VDDPST12 and VSS*
PENDCAPCOD_H	*Domain end enclosure cell*
PENDCAPCOD_V	*Domain end enclosure cell*
PFILLERCOD00048_V	*Digital Filler cell*
PFILLERCOD00130_H	*Digital Filler cell*
PFILLERCOD00624_V	*Digital Filler cell*
PFILLERCOD00650_H	*Digital Filler cell*
PFILLERROUTECOD06240_H	*Digital Filler cell*
PFILLERROUTECOD06240_V	*Digital Filler cell*
PFILLERROUTECOD53040_H	*Digital Filler cell*
PFILLERROUTECOD53040_V	*Digital Filler cell*
PFILLERSTRAPCOD06240_H	*Digital Filler cell*
PFILLERSTRAPCOD06240_V	*Digital Filler cell*
PRCUTCOD_H	*Power cut cell*
PRCUTCOD_V	*Power cut cell*
PRWDWUWSWEWCODCDGH_H	*8-Drive Regular Tri-State Output Pad with Input Enable, Programmable Slew-Rate Control, Bus Keeper Enable, Schmitt Trigger Enable, Retention Enable and Enable-Controlled Pull-Up/Pull-Down Resistors*
PRWDWUWSWEWCODCDGH_V	*8-Drive Regular Tri-State Output Pad with Input Enable, Programmable Slew-Rate Control, Bus Keeper Enable, Schmitt Trigger Enable, Retention Enable and Enable-Controlled Pull-Up/Pull-Down Resistors*
PRWDWUWSWEWCODCDGSH_H	*Core overdrive 1.2V, Regular I/O with POC. (When in POC mode, output = Z, pull resistors = disabled.)*

Continued...

Cell Name	Functional Description
PRWDWUWSWEWCODCDGSH_V	*Core overdrive 1.2V, Regular I/O with POC. (When in POC mode, output = Z, pull resistors = disabled.)*
PVDD08CODCDGM_H	*Digital VDDPST08 power and ground combo cell*
PVDD08CODCDGM_V	*Digital VDDPST08 power and ground combo cell*
PVDD1204CODCDGM_H	*Digital 1.2V power, VDDPST04 and ground combo cell*
PVDD1204CODCDGM_V	*Digital 1.2V power, VDDPST04 and ground combo cell*
PVDD12CODCDGM_H	*Digital 1.2V power and ground combo cell*
PVDD12CODCDGM_V	*Digital 1.2V power and ground combo cell*
PVDD12CODPOC_H	*Power-on-control cell*
PVDD12CODPOC_V	*Power-on-control cell*
PVDD1CODANAM_H	*Analog core power and ground combo cell, compatible to be used in digital IO domain*
PVDD1CODANAM_V	*Analog core power and ground combo cell, compatible to be used in digital IO domain*
PVDD1CODCDGM_H	*Digital core power VDD and ground combo cell*
PVDD1CODCDGM_V	*Digital core power VDD and ground combo cell*

4 Pin Descriptions

This chapter provides pin list along with pin descriptions for the TSMC *TPHN02P_075OD12GPIO* library.

Table 4.1: Pin Descriptions

Pin Name	Functional Description
AIO	*Analog signal*
AIO200	*Analog signal through 200 ohm resistor*
C	*Output signal to core*
DS0	*Driving selector*
DS1	*Driving selector*
DS2	*Driving selector*
DS3	*Driving selector*
ESD12	*ESD rail*
ESD12B	*ESD rail*
ESDB	*ESD rail*
I	*Input signal from core side*
IE	*Input enable*
IRTE	*Retention signal input*
OE	*Output enable*
PAD	*Signal pin on pad side*
PD	*Pull down enable*
POCCTRL	*POC horizontal bus, I/O voltage level*
POCCTRL12	*POC horizontal bus, I/O voltage level*
POCCTRLD	*POC horizontal bus, I/O voltage level*
PU	*Pull up enable*
RTE	*Retention signal bus*
SL	*Slew-rate-control enable. SL=1 enables Slew-rate-control function*
SPU	*Strong pull up enable*
ST	*Schmitt trigger enable. ST=1 enables Schmitt trigger input function*
TIEL	*Tie-low for disabling IRTE pin purpose*

5 Simultaneously Switching Output Driving Factors

This chapter provides information about simultaneously switching output driving factors of the TSMC *TPHN02P_075OD12GPIO* library.

5.1 Terminologies and Definitions

This section describes basic terminologies and definitions of simultaneously switching output driving factors.

5.1.1 Simultaneously Switching Output (SSO)

Simultaneously switching output (SSO) means that a certain number of I/O buffers switching at the same time with the same direction (H → L, HZ → L or L → H, LZ → H), which would result in noise on the power/ground lines because of the large dI/dt value and the parasitic inductance of the bonding wire on the I/O power/ground cells.

5.1.2 Simultaneously Switching Noise (SSN)

SSN means the noise produced by the simultaneously switching output buffers. It would change the voltage levels of power/ground nodes. It is tested at the device output by keeping one stable output at low "0" or high "1", while all other outputs of the device switching simultaneously. The noise occurred at the stable output node is called "Quiet Output Switching" (QOS). If the input low voltage is defined as Vil, the QOS of Vil is taken to be the maximum noise that the system can endure. If the input high voltage is defined as Vih, the QOS of Vih is taken to be the minimum noise that the system can endure.

5.1.3 Driving Index (DI)

DI is the maximum copies of the specific I/O cell switching from high to low simultaneously without making the voltage on the quiet output "0" higher than "V_{il}" or switching from low to high simultaneously without making the voltage on the quiet output "1" lower than "V_{ih}".

5.1.4 Driving Factor (DF)

DF is the amount of how the specific output buffer contributes to the SSN on the power/ground rail. The DF value of an output buffer is proportional to dI/dt, the derivative of the current on the output buffer. We can obtain DF as follows:

DF = 1/DI

5.2 DF Values

This section provides circuit model parameters and DF values of the *TPHN02P_075OD12GPIO* library. Illustration of simulation model and calcuation instruction can be referenced from the TSMC Standard I/O Library General Application Note, which provides general information and is available to download at TSMC Online.

Table 5.1 and Table 5.2 describe wire model and capacitive load of SSO simulations.

Table 5.1: R, L, C Wire Model

Model	R(ohm)	L(nH)	C(pF)
A	*0.3*	*1*	*4*
B	*0.3*	*2.1*	*4*
C			
D			

Table 5.2: Capacitive Load

Drive Select Pin Setting	C_{load}(pF)
(DS2,DS1,DS0) = '000'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '0000'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '0001'	*5 15 30 50*
(DS2,DS1,DS0) = '001'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '0010'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '0011'	*5 15 30 50*
(DS2,DS1,DS0) = '010'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '0100'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '0101'	*5 15 30 50*

Continued...

Drive Select Pin Setting	C_{load}**(pF)**
(DS2,DS1,DS0) = '011'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '0110'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '0111'	*5 15 30 50*
(DS2,DS1,DS0) = '100'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '1000'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '1001'	*5 15 30 50*
(DS2,DS1,DS0) = '101'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '1010'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '1011'	*5 15 30 50*
(DS2,DS1,DS0) = '110'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '1100'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '1101'	*5 15 30 50*
(DS2,DS1,DS0) = '111'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '1110'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '1111'	*5 15 30 50*
(DS2,DS1,DS0) = '000'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '0000'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '0001'	*5 15 30 50*
(DS2,DS1,DS0) = '001'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '0010'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '0011'	*5 15 30 50*
(DS2,DS1,DS0) = '010'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '0100'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '0101'	*5 15 30 50*
(DS2,DS1,DS0) = '011'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '0110'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '0111'	*5 15 30 50*
(DS2,DS1,DS0) = '100'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '1000'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '1001'	*5 15 30 50*
(DS2,DS1,DS0) = '101'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '1010'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '1011'	*5 15 30 50*
(DS2,DS1,DS0) = '110'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '1100'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '1101'	*5 15 30 50*
(DS2,DS1,DS0) = '111'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '1110'	*5 15 30 50*
(DS3,DS2,DS1,DS0) = '1111'	*5 15 30 50*

The following tables provide SSO DF value with respect to the bond wire inductance and the capacitive load.

Characterization Corner: *FFGNP_0P825V_0P880V_1P320V_0P360V_M40C_CBEST_CCBEST_T*

Table 5.3: DF Table for PRWDWUWSWEWCODCDGSH with output slew-rate control disable

I/O Type	C / Model	5pF	15pF	30pF	50pF
(DS3,DS2,DS1,DS0) = '0000'	**A**	*0.01*	*0.01*	*0.01*	*0.01*
	B	*0.014*	*0.01*	*0.01*	*0.01*
(DS3,DS2,DS1,DS0) = '0001'	**A**	*0.024*	*0.014*	*0.012*	*0.013*
	B	*0.052*	*0.027*	*0.019*	*0.015*
(DS3,DS2,DS1,DS0) = '0010'	**A**	*0.065*	*0.022*	*0.017*	*0.017*
	B	*0.124*	*0.040*	*0.028*	*0.029*
(DS3,DS2,DS1,DS0) = '0011'	**A**	*0.130*	*0.034*	*0.023*	*0.022*
	B	*0.212*	*0.055*	*0.036*	*0.036*
(DS3,DS2,DS1,DS0) = '0100'	**A**	*0.196*	*0.057*	*0.028*	*0.030*
	B	*0.300*	*0.086*	*0.042*	*0.038*
(DS3,DS2,DS1,DS0) = '0101'	**A**	*0.257*	*0.089*	*0.032*	*0.034*
	B	*0.381*	*0.127*	*0.052*	*0.043*
(DS3,DS2,DS1,DS0) = '0110'	**A**	*0.318*	*0.122*	*0.037*	*0.043*
	B	*0.458*	*0.168*	*0.065*	*0.065*
(DS3,DS2,DS1,DS0) = '0111'	**A**	*0.370*	*0.153*	*0.053*	*0.039*
	B	*0.527*	*0.208*	*0.105*	*0.068*
(DS3,DS2,DS1,DS0) = '1000'	**A**	*0.413*	*0.181*	*0.073*	*0.077*
	B	*0.578*	*0.245*	*0.117*	*0.136*
(DS3,DS2,DS1,DS0) = '1001'	**A**	*0.465*	*0.211*	*0.084*	*0.080*
	B	*0.631*	*0.283*	*0.127*	*0.140*
(DS3,DS2,DS1,DS0) = '1010'	**A**	*0.512*	*0.243*	*0.101*	*0.082*
	B	*0.688*	*0.324*	*0.143*	*0.141*
(DS3,DS2,DS1,DS0) = '1011'	**A**	*0.545*	*0.270*	*0.116*	*0.084*
	B	*0.746*	*0.359*	*0.162*	*0.142*
(DS3,DS2,DS1,DS0) = '1100'	**A**	*0.581*	*0.301*	*0.132*	*0.085*
	B	*0.805*	*0.397*	*0.182*	*0.160*
(DS3,DS2,DS1,DS0) = '1101'	**A**	*0.613*	*0.331*	*0.148*	*0.085*
	B	*0.859*	*0.438*	*0.193*	*0.178*
(DS3,DS2,DS1,DS0) = '1110'	**A**	*0.645*	*0.356*	*0.163*	*0.083*

Continued...

I/O Type	C / Model	5pF	15pF	30pF	50pF
	B	*0.902*	*0.482*	*0.206*	*0.194*
(DS3,DS2,DS1,DS0) = '1111'	**A**	*0.678*	*0.382*	*0.177*	*0.091*
	B	*0.942*	*0.518*	*0.221*	*0.206*

Table 5.4: DF Table for PRWDWUWSWEWCODCDGSH with output slew-rate control enable

I/O Type	C / Model	5pF	15pF	30pF	50pF
(DS3,DS2,DS1,DS0) = '0000'	**A**	*0.01*	*0.01*	*0.01*	*0.01*
	B	*0.01*	*0.01*	*0.01*	*0.01*
(DS3,DS2,DS1,DS0) = '0001'	**A**	*0.01*	*0.01*	*0.01*	*0.01*
	B	*0.016*	*0.015*	*0.013*	*0.012*
(DS3,DS2,DS1,DS0) = '0010'	**A**	*0.011*	*0.01*	*0.01*	*0.01*
	B	*0.024*	*0.020*	*0.019*	*0.017*
(DS3,DS2,DS1,DS0) = '0011'	**A**	*0.015*	*0.012*	*0.012*	*0.011*
	B	*0.033*	*0.025*	*0.023*	*0.021*
(DS3,DS2,DS1,DS0) = '0100'	**A**	*0.019*	*0.015*	*0.014*	*0.013*
	B	*0.042*	*0.030*	*0.027*	*0.024*
(DS3,DS2,DS1,DS0) = '0101'	**A**	*0.023*	*0.019*	*0.016*	*0.015*
	B	*0.049*	*0.034*	*0.030*	*0.027*
(DS3,DS2,DS1,DS0) = '0110'	**A**	*0.027*	*0.022*	*0.017*	*0.017*
	B	*0.055*	*0.042*	*0.033*	*0.030*
(DS3,DS2,DS1,DS0) = '0111'	**A**	*0.031*	*0.025*	*0.019*	*0.018*
	B	*0.060*	*0.048*	*0.038*	*0.033*
(DS3,DS2,DS1,DS0) = '1000'	**A**	*0.035*	*0.030*	*0.019*	*0.020*
	B	*0.071*	*0.057*	*0.041*	*0.037*
(DS3,DS2,DS1,DS0) = '1001'	**A**	*0.038*	*0.032*	*0.020*	*0.022*
	B	*0.078*	*0.061*	*0.047*	*0.041*
(DS3,DS2,DS1,DS0) = '1010'	**A**	*0.041*	*0.035*	*0.021*	*0.023*
	B	*0.085*	*0.065*	*0.052*	*0.045*
(DS3,DS2,DS1,DS0) = '1011'	**A**	*0.045*	*0.036*	*0.022*	*0.025*
	B	*0.093*	*0.068*	*0.057*	*0.049*
(DS3,DS2,DS1,DS0) = '1100'	**A**	*0.048*	*0.039*	*0.024*	*0.026*
	B	*0.100*	*0.072*	*0.062*	*0.053*
(DS3,DS2,DS1,DS0) = '1101'	**A**	*0.051*	*0.041*	*0.032*	*0.027*

Continued...

I/O Type	Model \ C	5pF	15pF	30pF	50pF
	B	*0.107*	*0.074*	*0.067*	*0.057*
(DS3,DS2,DS1,DS0) = '1110'	**A**	*0.053*	*0.042*	*0.033*	*0.029*
	B	*0.113*	*0.076*	*0.074*	*0.062*
(DS3,DS2,DS1,DS0) = '1111'	**A**	*0.056*	*0.044*	*0.034*	*0.030*
	B	*0.120*	*0.079*	*0.079*	*0.066*

Table 5.5: DF Table for PRWDWUWSWEWCODCDGH with output slew-rate control disable

I/O Type	Model \ C	5pF	15pF	30pF	50pF
(DS2,DS1,DS0) = '000'	**A**	*0.01*	*0.01*	*0.01*	*0.011*
	B	*0.022*	*0.016*	*0.023*	*0.016*
(DS2,DS1,DS0) = '001'	**A**	*0.029*	*0.019*	*0.020*	*0.025*
	B	*0.056*	*0.035*	*0.027*	*0.038*
(DS2,DS1,DS0) = '010'	**A**	*0.047*	*0.031*	*0.032*	*0.041*
	B	*0.084*	*0.051*	*0.045*	*0.050*
(DS2,DS1,DS0) = '011'	**A**	*0.100*	*0.040*	*0.039*	*0.042*
	B	*0.152*	*0.065*	*0.070*	*0.054*
(DS2,DS1,DS0) = '100'	**A**	*0.156*	*0.048*	*0.050*	*0.050*
	B	*0.226*	*0.086*	*0.072*	*0.073*
(DS2,DS1,DS0) = '101'	**A**	*0.219*	*0.054*	*0.050*	*0.055*
	B	*0.309*	*0.110*	*0.071*	*0.076*
(DS2,DS1,DS0) = '110'	**A**	*0.279*	*0.085*	*0.057*	*0.069*
	B	*0.386*	*0.135*	*0.097*	*0.075*
(DS2,DS1,DS0) = '111'	**A**	*0.341*	*0.116*	*0.074*	*0.077*
	B	*0.474*	*0.157*	*0.129*	*0.145*

Table 5.6: DF Table for PRWDWUWSWEWCODCDGH with output slew-rate control enable

I/O Type	Model \ C	5pF	15pF	30pF	50pF
(DS2,DS1,DS0) = '000'	**A**	*0.01*	*0.01*	*0.01*	*0.01*
	B	*0.015*	*0.013*	*0.015*	*0.013*

Continued...

I/O Type	C / Model	5pF	15pF	30pF	50pF
(DS2,DS1,DS0) = '001'	**A**	*0.017*	*0.014*	*0.014*	*0.014*
	B	*0.035*	*0.031*	*0.032*	*0.028*
(DS2,DS1,DS0) = '010'	**A**	*0.025*	*0.021*	*0.020*	*0.016*
	B	*0.050*	*0.042*	*0.038*	*0.033*
(DS2,DS1,DS0) = '011'	**A**	*0.032*	*0.027*	*0.024*	*0.022*
	B	*0.061*	*0.049*	*0.043*	*0.040*
(DS2,DS1,DS0) = '100'	**A**	*0.038*	*0.031*	*0.028*	*0.026*
	B	*0.069*	*0.055*	*0.048*	*0.042*
(DS2,DS1,DS0) = '101'	**A**	*0.044*	*0.034*	*0.031*	*0.030*
	B	*0.076*	*0.058*	*0.053*	*0.067*
(DS2,DS1,DS0) = '110'	**A**	*0.049*	*0.037*	*0.035*	*0.033*
	B	*0.084*	*0.059*	*0.055*	*0.061*
(DS2,DS1,DS0) = '111'	**A**	*0.054*	*0.040*	*0.038*	*0.036*
	B	*0.092*	*0.060*	*0.070*	*0.069*

6 Datasheet Contents

This chapter provides information about the contents of the TSMC Standard I/O library datasheet.

6.1 Truth Table

The truth table lists all possible combinations of input and output signals for a cell. Table 6.1 defines all the symbols used in the datasheet truth table.

Table 6.1: Truth Table Symbols

Symbol	Definition
0	Logic Low
1	Logic High
0/1	Don't care
-	Not Applicable
X	Unknown
Z	High Impedance
H	Pull-High
L	Pull-Low

The digital function I/O cells of this standard I/O library feature multi-drive, where the various drive strength can be achieved through different control pin settings. Please refer to the DC table(s) in chapter 2 for the output drive strength with respect to the drive control pin configuration(s).

6.2 Cell Information

The cell information section provides information about the number of pads required.

6.3 Leakage Power

The Leakage power section provides information about the standby leakage power from core power and I/O power respectively.

6.4 Pin Capacitance

The pin capacitance table describes the typical loading at each pin of the cell (pF), corresponding to each driving strength.

6.5 Propagation Delay

The propagation delay is a non-linear function of the loads. Using the 5 x 6 look-up table of the Synopsys *.lib* file, three piece-wise linear functions are created to calculate propagation delays for various load conditions. Each linear function has a dedicated linear equation, and three linear equations are provided to model the delay. Each group equation in the table of propagation delay is based on values extracted from the third row of the 5 x 6 look-up table for your reference. Three groups of linear equations are defined as follows:

Group 1: Based on the first and second points of the load index, if a cell has a load that is less than or equal to the second point of the load index, use the linear equation in Group 1 to calculate the propagation delay.

Group 2: Based on the third and fourth points of the load index, if a cell has a load that is more than the second point and less than the fifth point of the load index, use the linear equation in Group 2 to calculate the propagation delay.

Group 3: Based on the fifth and sixth points of the load index, if a cell has a load that is more than or equal to the fifth point of the load index, use the linear equation in Group 3 to calculate the propagation delay.

A linear equation is formed in the following format:

$$D = D_i + K * C_{load}$$

where

$D = propagationdelay(ns)$

$D_i = cellintrinsic(unloaded)delay(ns)$

$K = delayfactor(ns/pF)$

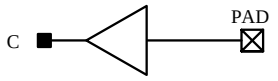
$C_{load} = valueofoutputload(pF)$

6.6 Example

The following is an example of datasheet.

PDIDGZ - (1)

Input Pad, High-Volt Tolerant - (2)



- (3)

Truth Table - (4)

INPUT	OUTPUT
PAD	C
0	0
1	1

Cell Information - (5)

	Value	Unit
Pad Number	1	-

Leakage Power - (6)

	Value	Unit
VDD	1.4944	nW
VDDPST	1.1191	nW

Pin Capacitance - (7)

	Value	Unit
PAD	3.4718	pF

Propagation Delay - (8)

	Group1	Group2	Group3
Timing Arc	**(< 0.0300)pf**	**(0.0300-0.3000)pf**	**(> 0.3000)pf**
PAD_C_T$_{PHL}$	1.0140+0.2000*Cload	1.0170+0.1400*Cload	1.0250+0.100*Cload
PAD_C_T$_{PLH}$	0.7023+0.2000*Cload	0.7034+0.1720*Cload	0.7065+0.1515*Cload

(1) Cell Name
(2) Cell Description
(3) Cell Schematic
(4) Truth Table
(5) Cell Information
(6) Leakage Power
(7) Pin Capacitance
(8) Propagation Delay

7 Design Kits Support

The following design kits/packages are delivered in a standard library release

Table 7.1: Deliverable Design Kits

Abbreviation	Description
rln	Release note
doc	Databook
nldm	Non-linear delay model
vlg	Verilog™ model
*vit	VHDL/Vital™ model
ctc	CeltIC cdB view
mdt	Mentor™ DFTAdvisor™ and Fastscan™ model
apf/apt	Astro/ICC frame view, layout view and runset files
sef	SoC Encounter™ frame view, layout view and runset files
gds	GDSII layout views
spi	LVS netlists in CDL™ format
lpe	Layout parasitic extracted spice netlist
ibs	IBIS model
cdk	Cell design kit
**vcn	Magma™ Volcano™ database

*vit kit is only provided in N20 and above technologies.
**vcn kits are only provided from N90 to N40 technologies.

8 Contact Us

The TSMC standard I/O libraries are released under the supervision of the TSMC standard quality assurance (QA) procedure. If you find any errors or encounter any problems with the *TPHN02P_075OD12GPIO* library, please contact your library distributor or TSMC regional application engineers for immediate assistance.

9 Datasheets

9.1 PCLAMPCCOD_H

Power clamp cell for core voltage

Cell Information

	Value	Unit
Cell Width	61.104	um
Cell Height	24.544	um

Leakage Power

	Value	Unit
VDDESD	2.593e+04	nW

9.2 PCLAMPCCOD_V

Power clamp cell for core voltage

Cell Information

	Value	Unit
Cell Width	26.448	um
Cell Height	55.536	um

Leakage Power

	Value	Unit
VDDESD	2.595e+04	nW

9.3 PCLAMPCOD_V

Power clamp cell for 1.2V

Cell Information		
	Value	**Unit**
Cell Width	57.792	um
Cell Height	59.904	um

Leakage Power		
	Value	**Unit**
VDDESD	8.437e+04	nW

9.4 PCORNERCOD_V

Corner cell

Cell Information

	Value	Unit
Cell Width	104.064	um
Cell Height	105.69	um

Leakage Power

	Value	Unit
VDDPST12	0	nW

Leakage Power

	Value	Unit
VDDPST08	1e-10	nW

Leakage Power

	Value	Unit
VDD	1e-10	nW

Leakage Power

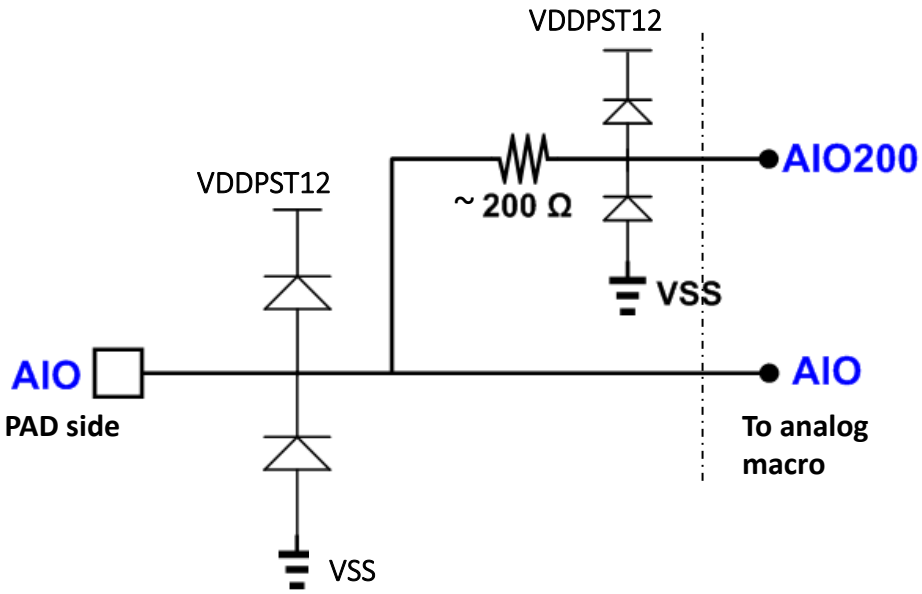
	Value	Unit
VDDPST04	1e-10	nW

Pin Capacitance

	Value	Unit
ESD12	0.01083	pF
ESD12B	0.01038	pF
ESDB	0.01061	pF
POCCTRL	0.009126	pF
POCCTRL12	0.01036	pF
POCCTRLD	0.0104	pF
RTE	0.009938	pF

9.5 PDB2CODANA_H

Analog signal cell, compatible to be used in digital IO domain



Truth Table

INPUT													OUTPUT	
VDDPST12	VDDPST08	VDDPST04	VDD	ESDB	ESD12	ESD12B	POCCTRL	POCCTRL12	POCCTRLD	RTE	AIO	AIO200	AIO	AIO200
1	-	-	-	-	-	-	-	-	-	-	0	0/Z	0	0
1	-	-	-	-	-	-	-	-	-	-	0/Z	0	0	0
1	-	-	-	-	-	-	-	-	-	-	1	1/Z	1	1
1	-	-	-	-	-	-	-	-	-	-	1/Z	1	1	1
0	-	-	-	-	-	-	-	-	-	-	0/Z	0/Z	X	X

*All undefined states in truth table are illegal operation

Cell Information

	Value	Unit
Cell Width	55.584	um
Cell Height	17.68	um
Pad Number	1	-

Leakage Power

	Value	Unit
VDDPST12	766.4	nW

Leakage Power

	Value	Unit
VDDPST08	0	nW

Leakage Power

	Value	Unit
VDD	0	nW

Leakage Power

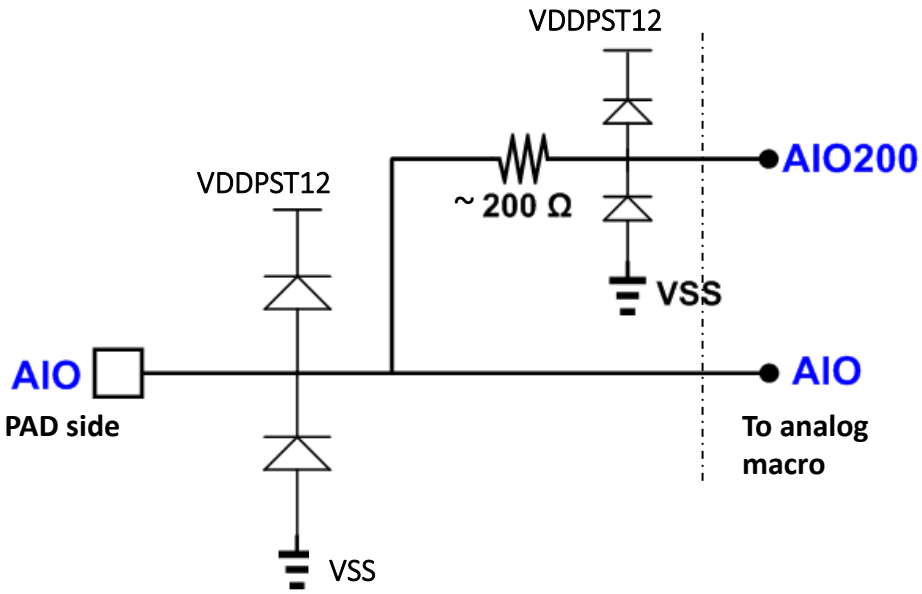
	Value	Unit
VDDPST04	0	nW

Pin Capacitance

	Value	Unit
AIO	0.7088	pF
AIO200	0.6952	pF
ESD12	0.004912	pF
ESD12B	0.005108	pF
ESDB	0.004934	pF
POCCTRL	0.004193	pF
POCCTRL12	0.004262	pF
POCCTRLD	0.004196	pF
RTE	0.004069	pF

9.6 PDB2CODANA_V

Analog signal cell, compatible to be used in digital IO domain



Truth Table

INPUT													OUTPUT	
VDDPST12	VDDPST08	VDDPST04	VDD	ESDB	ESD12	ESD12B	POCCTRL	POCCTRL12	POCCTRLD	RTE	AIO	AIO200	AIO	AIO200
1	-	-	-	-	-	-	-	-	-	-	0	0/Z	0	0
1	-	-	-	-	-	-	-	-	-	-	0/Z	0	0	0
1	-	-	-	-	-	-	-	-	-	-	1	1/Z	1	1
1	-	-	-	-	-	-	-	-	-	-	1/Z	1	1	1
0	-	-	-	-	-	-	-	-	-	-	0/Z	0/Z	X	X

*All undefined states in truth table are illegal operation

Cell Information

	Value	Unit
Cell Width	17.76	um
Cell Height	55.77	um
Pad Number	1	-

Leakage Power

	Value	Unit
VDDPST12	769.1	nW

Leakage Power

	Value	Unit
VDDPST08	0	nW

Leakage Power

	Value	Unit
VDD	0	nW

Leakage Power

	Value	Unit
VDDPST04	0	nW

Pin Capacitance

	Value	Unit
AIO	0.6961	pF
AIO200	0.6829	pF
ESD12	0.005168	pF
ESD12B	0.005312	pF
ESDB	0.005161	pF
POCCTRL	0.003726	pF
POCCTRL12	0.003571	pF
POCCTRLD	0.00402	pF
RTE	0.004282	pF

9.7 PDCAPR12COD06240_H

Filler Cell with DECAP between VDDPST12 and VSS

Cell Information

	Value	Unit
Cell Width	55.584	um
Cell Height	6.24	um

Leakage Power

	Value	Unit
VDDPST12	0	nW

Leakage Power

	Value	Unit
VDDPST08	0	nW

Leakage Power

	Value	Unit
VDD	0	nW

Leakage Power

	Value	Unit
VDDPST04	0	nW

Pin Capacitance

	Value	Unit
ESD12	0.001837	pF
ESD12B	0.001938	pF
ESDB	0.001826	pF
POCCTRL	0.00151	pF
POCCTRL12	0.001505	pF
POCCTRLD	0.001533	pF
RTE	0.001507	pF

9.8 PDCAPR12COD06240_V

Filler Cell with DECAP between VDDPST12 and VSS

Cell Information

	Value	Unit
Cell Width	6.24	um
Cell Height	55.77	um

Leakage Power

	Value	Unit
VDDPST12	1.465e-07	nW

Leakage Power

	Value	Unit
VDDPST08	0	nW

Leakage Power

	Value	Unit
VDD	0	nW

Leakage Power

	Value	Unit
VDDPST04	0	nW

Pin Capacitance

	Value	Unit
ESD12	0.001897	pF
ESD12B	0.001952	pF
ESDB	0.001891	pF
POCCTRL	0.001602	pF
POCCTRL12	0.001633	pF
POCCTRLD	0.001566	pF
RTE	0.001575	pF

9.9 PENDCAPCOD_H

Domain end enclosure cell

Cell Information

	Value	Unit
Cell Width	55.584	um
Cell Height	15.21	um

9.10 PENDCAPCOD_V

Domain end enclosure cell

Cell Information

	Value	Unit
Cell Width	15.072	um
Cell Height	55.77	um

9.11 PFILLERCOD00048_V

Digital Filler cell

Cell Information

	Value	Unit
Cell Width	0.048	um
Cell Height	55.77	um

Leakage Power

	Value	Unit
VDDPST12	0	nW

Leakage Power

	Value	Unit
VDDPST08	0	nW

Leakage Power

	Value	Unit
VDD	0	nW

Leakage Power

	Value	Unit
VDDPST04	0	nW

Pin Capacitance

	Value	Unit
ESD12	2.048e-05	pF
ESD12B	1.986e-05	pF
ESDB	2.01e-05	pF
POCCTRL	1.852e-05	pF
POCCTRL12	1.793e-05	pF
POCCTRLD	1.551e-05	pF
RTE	1.513e-05	pF

9.12 PFILLERCOD00130_H

Digital Filler cell

Cell Information

	Value	Unit
Cell Width	55.584	um
Cell Height	0.13	um

Leakage Power

	Value	Unit
VDDPST12	0	nW

Leakage Power

	Value	Unit
VDDPST08	0	nW

Leakage Power

	Value	Unit
VDD	0	nW

Leakage Power

	Value	Unit
VDDPST04	0	nW

Pin Capacitance

	Value	Unit
ESD12	2.871e-05	pF
ESD12B	2.723e-05	pF
ESDB	2.81e-05	pF
POCCTRL	2.536e-05	pF
POCCTRL12	2.567e-05	pF
POCCTRLD	2.31e-05	pF
RTE	2.239e-05	pF

9.13 PFILLERCOD00624_V

Digital Filler cell

Cell Information

	Value	Unit
Cell Width	0.624	um
Cell Height	55.77	um

Leakage Power

	Value	Unit
VDDPST12	0	nW

Leakage Power

	Value	Unit
VDDPST08	0	nW

Leakage Power

	Value	Unit
VDD	0	nW

Leakage Power

	Value	Unit
VDDPST04	0	nW

Pin Capacitance

	Value	Unit
ESD12	7.164e-05	pF
ESD12B	6.681e-05	pF
ESDB	7.209e-05	pF
POCCTRL	6.58e-05	pF
POCCTRL12	7.117e-05	pF
POCCTRLD	6.842e-05	pF
RTE	6.543e-05	pF

9.14 PFILLERCOD00650_H

Digital Filler cell

Cell Information

	Value	Unit
Cell Width	55.584	um
Cell Height	0.65	um

Leakage Power

	Value	Unit
VDDPST12	0	nW

Leakage Power

	Value	Unit
VDDPST08	0	nW

Leakage Power

	Value	Unit
VDD	0	nW

Leakage Power

	Value	Unit
VDDPST04	0	nW

Pin Capacitance

	Value	Unit
ESD12	7.388e-05	pF
ESD12B	6.897e-05	pF
ESDB	7.429e-05	pF
POCCTRL	6.781e-05	pF
POCCTRL12	7.356e-05	pF
POCCTRLD	7.077e-05	pF
RTE	6.762e-05	pF

9.15 PFILLERROUTECOD06240_H

Digital Filler cell

Cell Information

	Value	Unit
Cell Width	55.584	um
Cell Height	6.24	um

Leakage Power

	Value	Unit
VDDPST12	1e-10	nW

Leakage Power

	Value	Unit
VDDPST08	6.127e-06	nW

Leakage Power

	Value	Unit
VDD	7.874e-06	nW

Leakage Power

	Value	Unit
VDDPST04	0	nW

Pin Capacitance

	Value	Unit
ESD12	0.001739	pF
ESD12B	0.001705	pF
ESDB	0.001728	pF
POCCTRL	0.001286	pF
POCCTRL12	0.001363	pF
POCCTRLD	0.001363	pF
RTE	0.001331	pF

9.16 PFILLERROUTECOD06240_V

Digital Filler cell

Cell Information

	Value	Unit
Cell Width	6.24	um
Cell Height	55.77	um

Leakage Power

	Value	Unit
VDDPST12	1.496e-10	nW

Leakage Power

	Value	Unit
VDDPST08	6.127e-06	nW

Leakage Power

	Value	Unit
VDD	7.874e-06	nW

Leakage Power

	Value	Unit
VDDPST04	0	nW

Pin Capacitance

	Value	Unit
ESD12	0.001579	pF
ESD12B	0.001676	pF
ESDB	0.001596	pF
POCCTRL	0.001254	pF
POCCTRL12	0.001282	pF
POCCTRLD	0.001269	pF
RTE	0.001258	pF

9.17 PFILLERROUTECOD53040_H

Digital Filler cell

Cell Information

	Value	Unit
Cell Width	55.584	um
Cell Height	53.04	um

Leakage Power

	Value	Unit
VDDPST12	3.772e-08	nW

Leakage Power

	Value	Unit
VDDPST08	1e-10	nW

Leakage Power

	Value	Unit
VDD	1.398e-06	nW

Leakage Power

	Value	Unit
VDDPST04	0	nW

Pin Capacitance

	Value	Unit
ESD12	0.01562	pF
ESD12B	0.01545	pF
ESDB	0.01551	pF
POCCTRL	0.01136	pF
POCCTRL12	0.01209	pF
POCCTRLD	0.01213	pF
RTE	0.01196	pF

9.18 PFILLERROUTECOD53040_V

Digital Filler cell

Cell Information

	Value	Unit
Cell Width	53.04	um
Cell Height	55.77	um

Leakage Power

	Value	Unit
VDDPST12	1.539e-07	nW

Leakage Power

	Value	Unit
VDDPST08	4.084e-07	nW

Leakage Power

	Value	Unit
VDD	2.143e-07	nW

Leakage Power

	Value	Unit
VDDPST04	1e-10	nW

Pin Capacitance

	Value	Unit
ESD12	0.01199	pF
ESD12B	0.01278	pF
ESDB	0.01231	pF
POCCTRL	0.009663	pF
POCCTRL12	0.01003	pF
POCCTRLD	0.009984	pF
RTE	0.00988	pF

9.19 PFILLERSTRAPCOD06240_H

Digital Filler cell

Cell Information

	Value	Unit
Cell Width	55.584	um
Cell Height	6.24	um

Leakage Power

	Value	Unit
VDDPST12	1e-10	nW

Leakage Power

	Value	Unit
VDDPST08	1e-10	nW

Leakage Power

	Value	Unit
VDD	7.874e-06	nW

Leakage Power

	Value	Unit
VDDPST04	1e-10	nW

Pin Capacitance

	Value	Unit
ESD12	0.002096	pF
ESD12B	0.002037	pF
ESDB	0.002086	pF
POCCTRL	0.001569	pF
POCCTRL12	0.001607	pF
POCCTRLD	0.001609	pF
RTE	0.001564	pF

9.20 PFILLERSTRAPCOD06240_V

Digital Filler cell

Cell Information

	Value	Unit
Cell Width	6.24	um
Cell Height	55.77	um

Leakage Power

	Value	Unit
VDDPST12	0	nW

Leakage Power

	Value	Unit
VDDPST08	0	nW

Leakage Power

	Value	Unit
VDD	7.874e-06	nW

Leakage Power

	Value	Unit
VDDPST04	0	nW

Pin Capacitance

	Value	Unit
ESD12	0.0018	pF
ESD12B	0.00193	pF
ESDB	0.001814	pF
POCCTRL	0.001422	pF
POCCTRL12	0.001426	pF
POCCTRLD	0.001411	pF
RTE	0.001403	pF

9.21 PRCUTCOD_H

Power cut cell

Cell Information

	Value	Unit
Cell Width	55.584	um
Cell Height	19.76	um

9.22 PRCUTCOD_V

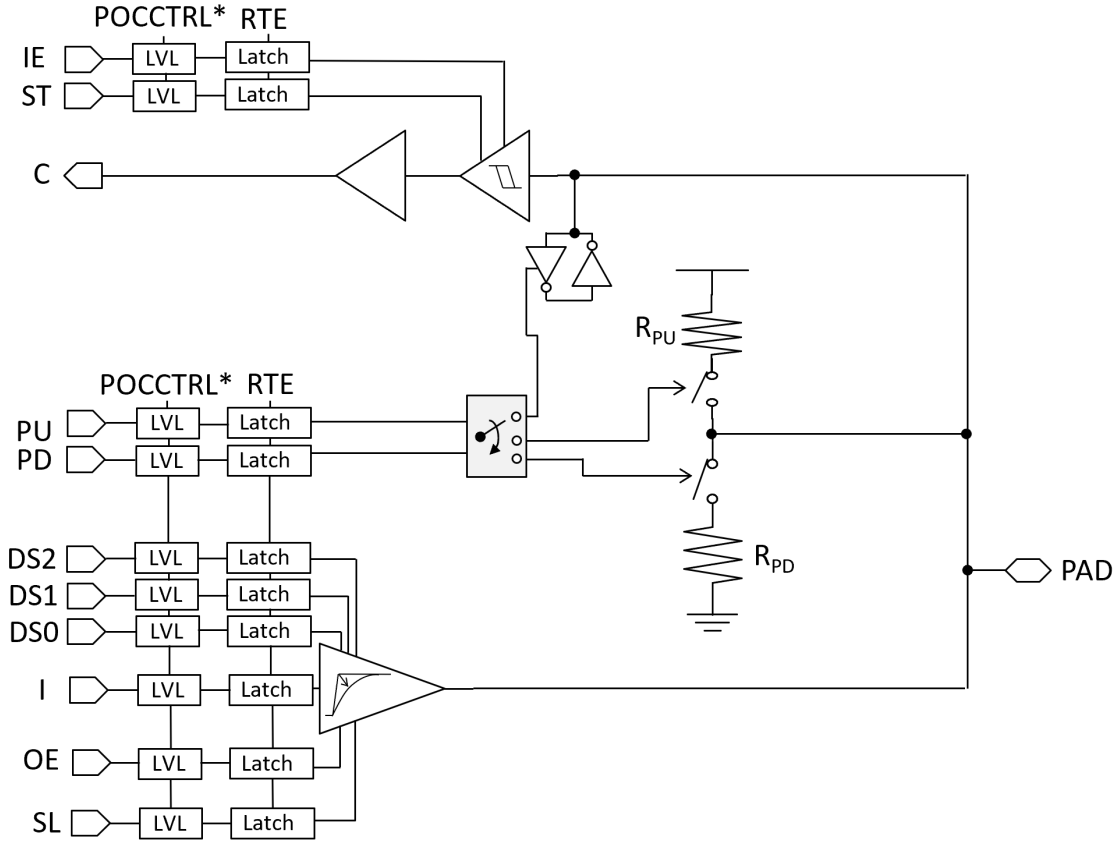
Power cut cell

Cell Information

	Value	Unit
Cell Width	19.776	um
Cell Height	55.77	um

9.23 PRWDWUWSWEWCODCDGH_H

8-Drive Regular Tri-State Output Pad with Input Enable, Programmable Slew-Rate Control, Bus Keeper Enable, Schmitt Trigger Enable, Retention Enable and Enable-Controlled Pull-Up/Pull-Down Resistors



Truth Table

INPUT																						OUTPUT	
VDD	VDDPST12	VDDPST08	VDDPST04	ESDB	ESD12	ESD12B	POCCTRL	POCCTRLD	POCCTRL12	RTE	DS2	DS1	DS0	SL	OE	I	PD	PU	PAD	ST	IE	PAD	C
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	1	0	0/1	0/1	-	0/1	0/1	0	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	1	1	0/1	0/1	-	0/1	1	1	1
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	1	1	0/1	0/1	-	0/1	0	1	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	0/1	0/1	0	0/1	0/1	-	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	0/1	0/1	1	0/1	0	-	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	0/1	0/1	1	0/1	1	-	1
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	0	0	Z	0/1	0	-	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	0	0	Z	0/1	1	-	X
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	1	0	Z	0/1	0	L	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	1	0	Z	0/1	1	L	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	0	1	Z	0/1	0	H	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	0	1	Z	0/1	1	H	1
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	1	1	Z	0/1	0	previous-state	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	1	1	Z	0/1	1	previous-state	previous-state
1	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	-	0/1	0/1	X	0
0	1	1	1	1	0	1	1	1	0	0	-	-	-	-	-	-	-	-	-	-	-	Z	X
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch1	Latch0	Latch	Latch	-	Latch	Latch	0	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch1	Latch1	Latch	Latch	-	Latch	Latch1	1	1
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch1	Latch1	Latch	Latch	-	Latch	Latch0	1	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	0	Latch	Latch	-	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	1	Latch	Latch0	-	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	1	Latch	Latch1	-	1
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch0	Z	Latch	Latch0	-	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch0	Z	Latch	Latch1	-	X
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch0	Z	Latch	Latch0	L	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch0	Z	Latch	Latch1	L	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch1	Z	Latch	Latch0	H	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch1	Z	Latch	Latch1	H	1
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch1	Z	Latch	Latch0	previous-state	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch1	Z	Latch	Latch1	previous-state	previous-state
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch1	Latch0	Latch	Latch	-	Latch	Latch	0	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch1	Latch1	Latch	Latch	-	Latch	Latch1	1	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch1	Latch1	Latch	Latch	-	Latch	Latch0	1	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	0	Latch	Latch	-	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	1	Latch	Latch0	-	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	1	Latch	Latch1	-	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch0	Z	Latch	Latch0	-	X

Continued. . .

VDD	VDDPST12	VDDPST08	VDDPST04	ESDB	ESD12	ESD12B	POCCTRL	POCCTRLD	POCCTRL12	RTE	DS2	DS1	DS0	SL	OE	I	PD	PU	PAD	ST	IE	PAD	C
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch0	Z	Latch	Latch1	-	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch0	Z	Latch	Latch0	L	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch0	Z	Latch	Latch1	L	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch1	Z	Latch	Latch0	H	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch1	Z	Latch	Latch1	H	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch1	Z	Latch	Latch0	previous-state	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch1	Z	Latch	Latch1	previous-state	X
1	0	1	1	1	0	0	1	1	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	-	0/1	0/1	X	0
0	0	1	1	1	0	0	1	1	0	0	-	-	-	-	-	-	-	-	-	-	-	X	X
1	0	1	0	1	0	0	1	1	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	-	0/1	0/1	X	0
0	0	1	0	1	0	0	1	1	0	0	-	-	-	-	-	-	-	-	-	-	-	X	X
1	0	0	1	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	-	0/1	0/1	X	0
0	0	0	1	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	X	X
0	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	Z	-	-	X	X

*All undefined states in truth table are illegal operation

Cell Information

	Value	Unit
Cell Width	55.584	um
Cell Height	17.68	um
Pad Number	1	-

Leakage Power

	Value	Unit
VDDPST12	1.087e+04	nW

Leakage Power

	Value	Unit
VDDPST08	4583	nW

Leakage Power

	Value	Unit
VDD	4490	nW

Leakage Power

	Value	Unit
VDDPST04	1e-10	nW

Pin Capacitance

	Value	Unit
DS0	0.00561	pF
DS1	0.005363	pF
DS2	0.005518	pF
ESD12	0.008281	pF
ESD12B	0.009654	pF
ESDB	0.008907	pF
I	0.005227	pF
IE	0.005157	pF
OE	0.004835	pF
PAD	1.165	pF
PD	0.003974	pF
POCCTRL	0.007021	pF
POCCTRL12	0.009329	pF

Continued...

	Value	Unit
POCCTRLD	0.006771	pF
PU	0.004956	pF
RTE	0.006322	pF
SL	0.004781	pF
ST	0.004962	pF

Propagation Delay

	Group1	Group2	Group3
Timing Arc	**(< 0.03)pf**	**(0.03-0.3)pf**	**(> 0.3)pf**
IE_C_T$_{PHL}${!ST}	0.1222+0.3000*Cload	0.1224+0.2960*Cload	0.1222+0.2975*Cload
IE_C_T$_{PHL}${ST}	0.1222+0.3000*Cload	0.1224+0.2960*Cload	0.1222+0.2975*Cload
IE_C_T$_{PLH}${!ST}	0.3326+0.2650*Cload	0.3328+0.2600*Cload	0.3327+0.2610*Cload
IE_C_T$_{PLH}${ST}	0.3621+0.2650*Cload	0.3621+0.2620*Cload	0.3617+0.2625*Cload
Timing Arc	**(< 10)pf**	**(10-70)pf**	**(> 70)pf**
I_PAD_T$_{PHL}${!DS0&!DS1&!DS2&!SL}	0.5670+0.1612*Cload	0.5795+0.1603*Cload	0.6000+0.1600*Cload
I_PAD_T$_{PHL}${!DS0&!DS1&!DS2&SL}	1.0200+0.1634*Cload	1.0560+0.1606*Cload	1.0410+0.1607*Cload
I_PAD_T$_{PHL}${!DS0&!DS1&DS2&!SL}	0.3963+0.0338*Cload	0.4130+0.0326*Cload	0.4190+0.0325*Cload
I_PAD_T$_{PHL}${!DS0&!DS1&DS2&SL}	0.7838+0.0412*Cload	0.8920+0.0336*Cload	0.9410+0.0326*Cload
I_PAD_T$_{PHL}${!DS0&DS1&!DS2&!SL}	0.4193+0.0549*Cload	0.4285+0.0541*Cload	0.4360+0.0539*Cload
I_PAD_T$_{PHL}${!DS0&DS1&!DS2&SL}	0.8300+0.0608*Cload	0.9155+0.0545*Cload	0.9390+0.0540*Cload
I_PAD_T$_{PHL}${!DS0&DS1&DS2&!SL}	0.3862+0.0248*Cload	0.4037+0.0235*Cload	0.4080+0.0234*Cload
I_PAD_T$_{PHL}${!DS0&DS1&DS2&SL}	0.7660+0.0328*Cload	0.8815+0.0249*Cload	0.9450+0.0236*Cload
I_PAD_T$_{PHL}${DS0&!DS1&!DS2&!SL}	0.4538+0.0817*Cload	0.4655+0.0809*Cload	0.4690+0.0808*Cload
I_PAD_T$_{PHL}${DS0&!DS1&!DS2&SL}	0.8850+0.0860*Cload	0.9465+0.0813*Cload	0.9650+0.0809*Cload
I_PAD_T$_{PHL}${DS0&!DS1&DS2&!SL}	0.3897+0.0285*Cload	0.4055+0.0273*Cload	0.4090+0.0272*Cload
I_PAD_T$_{PHL}${DS0&!DS1&DS2&SL}	0.7732+0.0362*Cload	0.8845+0.0285*Cload	0.9430+0.0273*Cload
I_PAD_T$_{PHL}${DS0&DS1&!DS2&!SL}	0.4019+0.0418*Cload	0.4135+0.0409*Cload	0.4230+0.0407*Cload
I_PAD_T$_{PHL}${DS0&DS1&!DS2&SL}	0.8030+0.0484*Cload	0.9015+0.0415*Cload	0.9370+0.0408*Cload
I_PAD_T$_{PHL}${DS0&DS1&DS2&!SL}	0.3835+0.0221*Cload	0.4016+0.0207*Cload	0.4110+0.0205*Cload
I_PAD_T$_{PHL}${DS0&DS1&DS2&SL}	0.7609+0.0304*Cload	0.8785+0.0223*Cload	0.9510+0.0208*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&!DS2&!SL}	0.3659+0.0712*Cload	0.3775+0.0703*Cload	0.3770+0.0703*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&!DS2&SL}	1.0230+0.0802*Cload	1.1485+0.0711*Cload	1.1780+0.0705*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&DS2&!SL}	0.3057+0.0150*Cload	0.3160+0.0143*Cload	0.3230+0.0142*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&DS2&SL}	0.8170+0.0292*Cload	0.9915+0.0175*Cload	1.1180+0.0150*Cload
I_PAD_T$_{PLH}${!DS0&DS1&!DS2&!SL}	0.3112+0.0242*Cload	0.3207+0.0236*Cload	0.3270+0.0235*Cload
I_PAD_T$_{PLH}${!DS0&DS1&!DS2&SL}	0.8610+0.0378*Cload	1.0320+0.0260*Cload	1.1290+0.0240*Cload
I_PAD_T$_{PLH}${!DS0&DS1&DS2&!SL}	0.3029+0.0112*Cload	0.3127+0.0104*Cload	0.3160+0.0103*Cload
I_PAD_T$_{PLH}${!DS0&DS1&DS2&SL}	0.8029+0.0252*Cload	0.9705+0.0141*Cload	1.1120+0.0113*Cload
I_PAD_T$_{PLH}${DS0&!DS1&!DS2&!SL}	0.3231+0.0361*Cload	0.3355+0.0353*Cload	0.3370+0.0353*Cload
I_PAD_T$_{PLH}${DS0&!DS1&!DS2&SL}	0.9110+0.0484*Cload	1.0740+0.0370*Cload	1.1420+0.0356*Cload
I_PAD_T$_{PLH}${DS0&!DS1&DS2&!SL}	0.3039+0.0127*Cload	0.3136+0.0120*Cload	0.3180+0.0119*Cload
I_PAD_T$_{PLH}${DS0&!DS1&DS2&SL}	0.8088+0.0267*Cload	0.9785+0.0155*Cload	1.1150+0.0128*Cload
I_PAD_T$_{PLH}${DS0&DS1&!DS2&!SL}	0.3055+0.0185*Cload	0.3136+0.0179*Cload	0.3180+0.0178*Cload
I_PAD_T$_{PLH}${DS0&DS1&!DS2&SL}	0.8340+0.0325*Cload	1.0085+0.0207*Cload	1.1220+0.0184*Cload
I_PAD_T$_{PLH}${DS0&DS1&DS2&!SL}	0.3027+0.0100*Cload	0.3144+0.0091*Cload	0.3195+0.0090*Cload
I_PAD_T$_{PLH}${DS0&DS1&DS2&SL}	0.8008+0.0238*Cload	0.9635+0.0131*Cload	1.1090+0.0102*Cload
Timing Arc	**(< 10)pf**	**(10-70)pf**	**(> 70)pf**
OE_PAD_T$_{PHZ}${!DS0&!DS1&!DS2&!SL}	0.1933	0.1935	0.1937
OE_PAD_T$_{PHZ}${!DS0&!DS1&!DS2&SL}	0.1932	0.1934	0.1936
OE_PAD_T$_{PHZ}${!DS0&!DS1&DS2&!SL}	0.1948	0.1950	0.1952
OE_PAD_T$_{PHZ}${!DS0&!DS1&DS2&SL}	0.1947	0.1949	0.1951
OE_PAD_T$_{PHZ}${!DS0&DS1&!DS2&!SL}	0.1980	0.1982	0.1984
OE_PAD_T$_{PHZ}${!DS0&DS1&!DS2&SL}	0.1978	0.1980	0.1982
OE_PAD_T$_{PHZ}${!DS0&DS1&DS2&!SL}	0.1983	0.1985	0.1987

Continued...

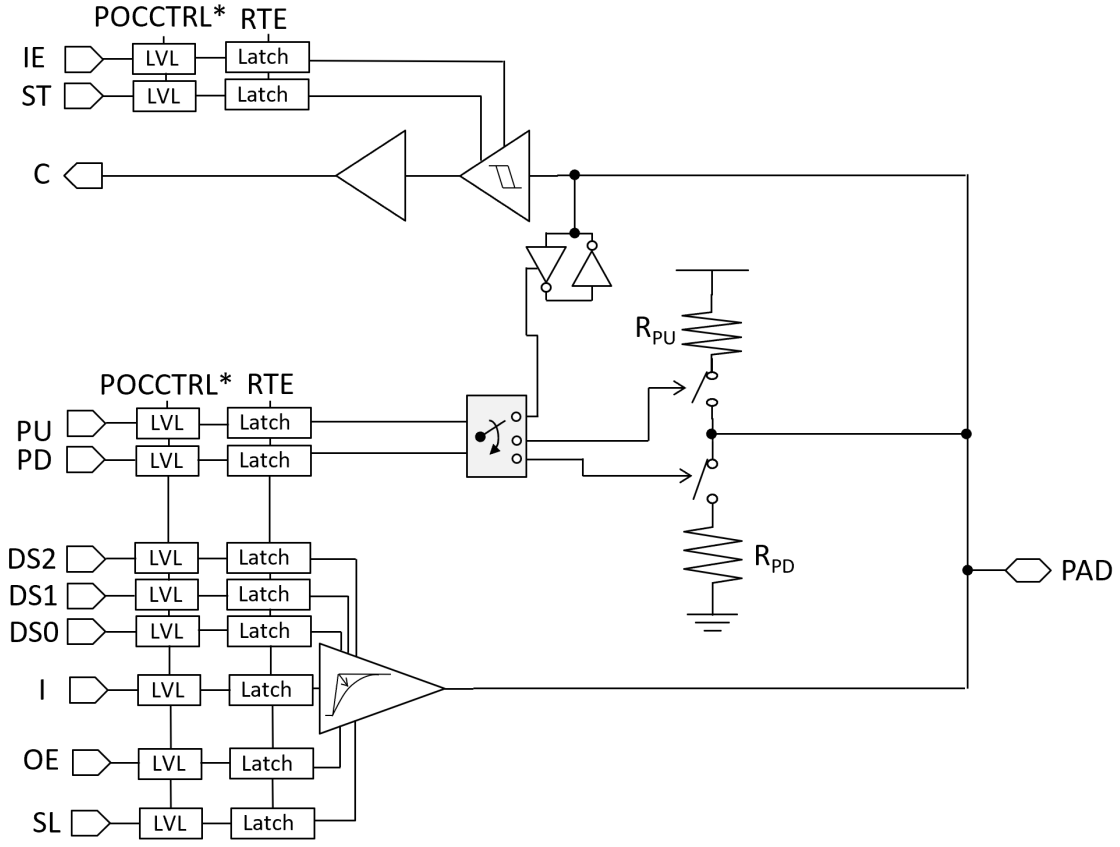
	Group1	Group2	Group3
OE_PAD_T$_{PHZ}${!DS0&DS1&DS2&SL}	0.1981	0.1983	0.1985
OE_PAD_T$_{PHZ}${DS0&!DS1&!DS2&!SL}	0.1979	0.1981	0.1983
OE_PAD_T$_{PHZ}${DS0&!DS1&!DS2&SL}	0.1976	0.1978	0.1980
OE_PAD_T$_{PHZ}${DS0&!DS1&DS2&!SL}	0.1967	0.1969	0.1971
OE_PAD_T$_{PHZ}${DS0&!DS1&DS2&SL}	0.1966	0.1968	0.1970
OE_PAD_T$_{PHZ}${DS0&DS1&!DS2&!SL}	0.2005	0.2007	0.2009
OE_PAD_T$_{PHZ}${DS0&DS1&!DS2&SL}	0.2002	0.2004	0.2006
OE_PAD_T$_{PHZ}${DS0&DS1&DS2&!SL}	0.2007	0.2009	0.2011
OE_PAD_T$_{PHZ}${DS0&DS1&DS2&SL}	0.2005	0.2007	0.2009
OE_PAD_T$_{PLZ}${!DS0&!DS1&!DS2&!SL}	0.2279	0.2281	0.2283
OE_PAD_T$_{PLZ}${!DS0&!DS1&!DS2&SL}	0.2275	0.2277	0.2279
OE_PAD_T$_{PLZ}${!DS0&!DS1&DS2&!SL}	0.2110	0.2112	0.2114
OE_PAD_T$_{PLZ}${!DS0&!DS1&DS2&SL}	0.2105	0.2107	0.2109
OE_PAD_T$_{PLZ}${!DS0&DS1&!DS2&!SL}	0.2216	0.2218	0.2220
OE_PAD_T$_{PLZ}${!DS0&DS1&!DS2&SL}	0.2211	0.2213	0.2215
OE_PAD_T$_{PLZ}${!DS0&DS1&DS2&!SL}	0.2100	0.2102	0.2104
OE_PAD_T$_{PLZ}${!DS0&DS1&DS2&SL}	0.2096	0.2098	0.2100
OE_PAD_T$_{PLZ}${DS0&!DS1&!DS2&!SL}	0.2334	0.2336	0.2338
OE_PAD_T$_{PLZ}${DS0&!DS1&!DS2&SL}	0.2330	0.2332	0.2334
OE_PAD_T$_{PLZ}${DS0&!DS1&DS2&!SL}	0.2107	0.2109	0.2111
OE_PAD_T$_{PLZ}${DS0&!DS1&DS2&SL}	0.2103	0.2105	0.2107
OE_PAD_T$_{PLZ}${DS0&DS1&!DS2&!SL}	0.2209	0.2211	0.2213
OE_PAD_T$_{PLZ}${DS0&DS1&!DS2&SL}	0.2204	0.2206	0.2208
OE_PAD_T$_{PLZ}${DS0&DS1&DS2&!SL}	0.2099	0.2101	0.2103
OE_PAD_T$_{PLZ}${DS0&DS1&DS2&SL}	0.2094	0.2096	0.2098
OE_PAD_T$_{PZH}${!DS0&!DS1&!DS2&!SL}	0.3531+0.0712*Cload	0.3645+0.0703*Cload	0.3650+0.0703*Cload
OE_PAD_T$_{PZH}${!DS0&!DS1&!DS2&SL}	0.9970+0.0804*Cload	1.1210+0.0712*Cload	1.1540+0.0705*Cload
OE_PAD_T$_{PZH}${!DS0&!DS1&DS2&!SL}	0.2966+0.0150*Cload	0.3070+0.0143*Cload	0.3140+0.0142*Cload
OE_PAD_T$_{PZH}${!DS0&!DS1&DS2&SL}	0.7950+0.0293*Cload	0.9705+0.0175*Cload	1.0970+0.0150*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&!DS2&!SL}	0.3012+0.0243*Cload	0.3110+0.0236*Cload	0.3170+0.0235*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&!DS2&SL}	0.8370+0.0382*Cload	1.0145+0.0259*Cload	1.1080+0.0240*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&DS2&!SL}	0.2940+0.0112*Cload	0.3064+0.0103*Cload	0.3070+0.0103*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&DS2&SL}	0.7801+0.0253*Cload	0.9495+0.0141*Cload	1.0910+0.0113*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&!DS2&!SL}	0.3134+0.0360*Cload	0.3220+0.0354*Cload	0.3260+0.0353*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&!DS2&SL}	0.8880+0.0486*Cload	1.0520+0.0370*Cload	1.1190+0.0356*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&DS2&!SL}	0.2944+0.0128*Cload	0.3046+0.0120*Cload	0.3090+0.0119*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&DS2&SL}	0.7858+0.0269*Cload	0.9575+0.0155*Cload	1.0940+0.0128*Cload
OE_PAD_T$_{PZH}${DS0&DS1&!DS2&!SL}	0.2963+0.0185*Cload	0.3043+0.0179*Cload	0.3080+0.0178*Cload
OE_PAD_T$_{PZH}${DS0&DS1&!DS2&SL}	0.8111+0.0328*Cload	0.9875+0.0207*Cload	1.1010+0.0184*Cload
OE_PAD_T$_{PZH}${DS0&DS1&DS2&!SL}	0.2938+0.0100*Cload	0.3056+0.0091*Cload	0.3107+0.0090*Cload
OE_PAD_T$_{PZH}${DS0&DS1&DS2&SL}	0.7771+0.0240*Cload	0.9415+0.0131*Cload	1.0880+0.0102*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&!DS2&!SL}	0.5100+0.1614*Cload	0.5245+0.1603*Cload	0.5190+0.1603*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&!DS2&SL}	0.9610+0.1638*Cload	1.0005+0.1607*Cload	1.0190+0.1603*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&DS2&!SL}	0.3884+0.0338*Cload	0.4025+0.0327*Cload	0.4120+0.0325*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&DS2&SL}	0.7712+0.0417*Cload	0.8860+0.0336*Cload	0.9280+0.0327*Cload
OE_PAD_T$_{PZL}${!DS0&DS1&!DS2&!SL}	0.4018+0.0550*Cload	0.4125+0.0541*Cload	0.4210+0.0539*Cload
OE_PAD_T$_{PZL}${!DS0&DS1&!DS2&SL}	0.8090+0.0612*Cload	0.9005+0.0545*Cload	0.9250+0.0540*Cload
OE_PAD_T$_{PZL}${!DS0&DS1&DS2&!SL}	0.3810+0.0249*Cload	0.3995+0.0235*Cload	0.4040+0.0234*Cload
OE_PAD_T$_{PZL}${!DS0&DS1&DS2&SL}	0.7568+0.0332*Cload	0.8760+0.0250*Cload	0.9430+0.0236*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&!DS2&!SL}	0.4270+0.0817*Cload	0.4395+0.0809*Cload	0.4440+0.0808*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&!DS2&SL}	0.8530+0.0866*Cload	0.9225+0.0813*Cload	0.9410+0.0809*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&DS2&!SL}	0.3832+0.0286*Cload	0.4005+0.0273*Cload	0.4040+0.0272*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&DS2&SL}	0.7629+0.0366*Cload	0.8805+0.0285*Cload	0.9390+0.0273*Cload
OE_PAD_T$_{PZL}${DS0&DS1&!DS2&!SL}	0.3893+0.0419*Cload	0.4025+0.0409*Cload	0.4120+0.0407*Cload
OE_PAD_T$_{PZL}${DS0&DS1&!DS2&SL}	0.7850+0.0490*Cload	0.8890+0.0416*Cload	0.9280+0.0408*Cload
OE_PAD_T$_{PZL}${DS0&DS1&DS2&!SL}	0.3798+0.0221*Cload	0.3983+0.0207*Cload	0.4070+0.0205*Cload
OE_PAD_T$_{PZL}${DS0&DS1&DS2&SL}	0.7529+0.0307*Cload	0.8765+0.0223*Cload	0.9500+0.0208*Cload

Continued...

	Group1	**Group2**	**Group3**
Timing Arc	**(< 0.03)pf**	**(0.03-0.3)pf**	**(> 0.3)pf**
PAD_C_T$_{PHL}${!ST}	0.2703+0.3000*Cload	0.2705+0.2960*Cload	0.2702+0.2990*Cload
PAD_C_T$_{PHL}${ST}	0.5454+0.3050*Cload	0.5456+0.2980*Cload	0.5464+0.2960*Cload
PAD_C_T$_{PLH}${!ST}	0.3530+0.2700*Cload	0.3532+0.2620*Cload	0.3530+0.2615*Cload
PAD_C_T$_{PLH}${ST}	0.5960+0.2650*Cload	0.5963+0.2600*Cload	0.5957+0.2625*Cload

9.24 PRWDWUWSWEWCODCDGH_V

8-Drive Regular Tri-State Output Pad with Input Enable, Programmable Slew-Rate Control, Bus Keeper Enable, Schmitt Trigger Enable, Retention Enable and Enable-Controlled Pull-Up/Pull-Down Resistors



Truth Table

INPUT																						OUTPUT	
VDD	VDDPST12	VDDPST08	VDDPST04	ESDB	ESD12	ESD12B	POCCTRL	POCCTRLD	POCCTRL12	RTE	DS2	DS1	DS0	SL	OE	I	PD	PU	PAD	ST	IE	PAD	C
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	1	0	0/1	0/1	-	0/1	0/1	0	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	1	1	0/1	0/1	-	0/1	1	1	1
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	1	1	0/1	0/1	-	0/1	0	1	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	0/1	0/1	0	0/1	0/1	-	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	0/1	0/1	1	0/1	0	-	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	0/1	0/1	1	0/1	1	-	1
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	0	0	Z	0/1	0	-	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	0	0	Z	0/1	1	-	X
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	1	0	Z	0/1	0	L	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	1	0	Z	0/1	1	L	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	0	1	Z	0/1	0	H	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	0	1	Z	0/1	1	H	1
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	1	1	Z	0/1	0	previous-state	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0	0/1	1	1	Z	0/1	1	previous-state	previous-state
1	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	-	0/1	0/1	X	0
0	1	1	1	1	0	1	1	1	0	0	-	-	-	-	-	-	-	-	-	-	-	Z	X
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch1	Latch0	Latch	Latch	-	Latch	Latch	0	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch1	Latch1	Latch	Latch	-	Latch	Latch1	1	1
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch1	Latch1	Latch	Latch	-	Latch	Latch0	1	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	0	Latch	Latch	-	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	1	Latch	Latch0	-	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	1	Latch	Latch1	-	1
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch0	Z	Latch	Latch0	-	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch0	Z	Latch	Latch1	-	X
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch0	Z	Latch	Latch0	L	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch0	Z	Latch	Latch1	L	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch1	Z	Latch	Latch0	H	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch1	Z	Latch	Latch1	H	1
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch1	Z	Latch	Latch0	previous-state	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch1	Z	Latch	Latch1	previous-state	previous-state
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch1	Latch0	Latch	Latch	-	Latch	Latch	0	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch1	Latch1	Latch	Latch	-	Latch	Latch1	1	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch1	Latch1	Latch	Latch	-	Latch	Latch0	1	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	0	Latch	Latch	-	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	1	Latch	Latch0	-	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	1	Latch	Latch1	-	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch0	Z	Latch	Latch0	-	X

Continued. . .

VDD	VDDPST12	VDDPST08	VDDPST04	ESDB	ESD12	ESD12B	POCCTRL	POCCTRLD	POCCTRL12	RTE	DS2	DS1	DS0	SL	OE	I	PD	PU	PAD	ST	IE	PAD	C
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch0	Z	Latch	Latch1	-	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch0	Z	Latch	Latch0	L	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch0	Z	Latch	Latch1	L	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch1	Z	Latch	Latch0	H	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch1	Z	Latch	Latch1	H	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch1	Z	Latch	Latch0	previous-state	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch1	Z	Latch	Latch1	previous-state	X
1	0	1	1	1	0	0	1	1	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	-	0/1	0/1	X	0
0	0	1	1	1	0	0	1	1	0	0	-	-	-	-	-	-	-	-	-	-	-	X	X
1	0	1	0	1	0	0	1	1	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	-	0/1	0/1	X	0
0	0	1	0	1	0	0	1	1	0	0	-	-	-	-	-	-	-	-	-	-	-	X	X
1	0	0	1	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	-	0/1	0/1	X	0
0	0	0	1	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	X	X
0	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	Z	-	-	X	X

*All undefined states in truth table are illegal operation

Cell Information

	Value	Unit
Cell Width	17.76	um
Cell Height	55.77	um
Pad Number	1	-

Leakage Power

	Value	Unit
VDDPST12	1.087e+04	nW

Pin Capacitance

	Value	Unit
DS0	0.003132	pF
DS1	0.002989	pF
DS2	0.002497	pF
ESD12	0.00922	pF
ESD12B	0.01189	pF
ESDB	0.009866	pF
I	0.002866	pF
IE	0.002243	pF
OE	0.002654	pF
PAD	1.131	pF
PD	0.00254	pF
POCCTRL	0.006748	pF
POCCTRL12	0.008543	pF
POCCTRLD	0.006838	pF
PU	0.002645	pF
RTE	0.007941	pF
SL	0.002182	pF
ST	0.002457	pF

Propagation Delay

	Group1	Group2	Group3
Timing Arc	**(< 0.03)pf**	**(0.03-0.3)pf**	**(> 0.3)pf**
IE_C_T$_{PHL}${!ST}	0.1202+0.4850*Cload	0.1201+0.4880*Cload	0.1201+0.4895*Cload
IE_C_T$_{PHL}${ST}	0.1202+0.4850*Cload	0.1201+0.4880*Cload	0.1201+0.4895*Cload
IE_C_T$_{PLH}${!ST}	0.3301+0.4650*Cload	0.3301+0.4640*Cload	0.3298+0.4645*Cload
IE_C_T$_{PLH}${ST}	0.3596+0.4600*Cload	0.3596+0.4620*Cload	0.3588+0.4665*Cload
Timing Arc	**(< 10)pf**	**(10-70)pf**	**(> 70)pf**
I_PAD_T$_{PHL}${!DS0&!DS1&!DS2&!SL}	0.5760+0.1646*Cload	0.5900+0.1636*Cload	0.5810+0.1637*Cload
I_PAD_T$_{PHL}${!DS0&!DS1&!DS2&SL}	0.9650+0.1664*Cload	0.9995+0.1639*Cload	1.0110+0.1637*Cload
I_PAD_T$_{PHL}${!DS0&!DS1&DS2&!SL}	0.3981+0.0349*Cload	0.4195+0.0333*Cload	0.4310+0.0331*Cload

Continued...

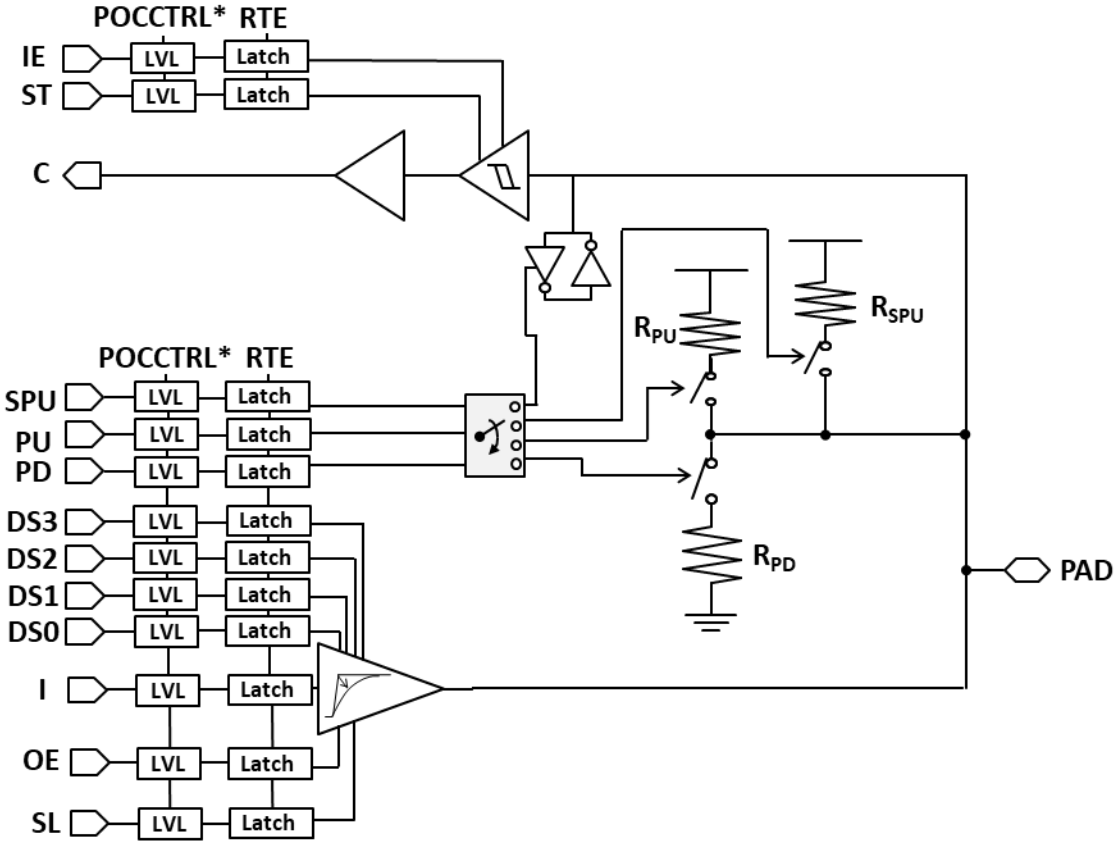
	Group1	Group2	Group3
I_PAD_T$_{PHL}${!DS0&!DS1&DS2&SL}	0.7239+0.0413*Cload	0.8275+0.0341*Cload	0.8650+0.0333*Cload
I_PAD_T$_{PHL}${!DS0&DS1&!DS2&!SL}	0.4235+0.0563*Cload	0.4395+0.0551*Cload	0.4450+0.0550*Cload
I_PAD_T$_{PHL}${!DS0&DS1&!DS2&SL}	0.7650+0.0614*Cload	0.8430+0.0556*Cload	0.8660+0.0551*Cload
I_PAD_T$_{PHL}${!DS0&DS1&DS2&!SL}	0.3845+0.0260*Cload	0.4090+0.0242*Cload	0.4130+0.0241*Cload
I_PAD_T$_{PHL}${!DS0&DS1&DS2&SL}	0.6942+0.0330*Cload	0.8060+0.0254*Cload	0.8650+0.0242*Cload
I_PAD_T$_{PHL}${DS0&!DS1&!DS2&!SL}	0.4622+0.0833*Cload	0.4740+0.0824*Cload	0.4840+0.0822*Cload
I_PAD_T$_{PHL}${DS0&!DS1&!DS2&SL}	0.8280+0.0874*Cload	0.8875+0.0827*Cload	0.9010+0.0824*Cload
I_PAD_T$_{PHL}${DS0&!DS1&DS2&!SL}	0.3904+0.0296*Cload	0.4135+0.0279*Cload	0.4230+0.0277*Cload
I_PAD_T$_{PHL}${DS0&!DS1&DS2&SL}	0.7120+0.0364*Cload	0.8205+0.0289*Cload	0.8680+0.0279*Cload
I_PAD_T$_{PHL}${DS0&DS1&!DS2&!SL}	0.4041+0.0429*Cload	0.4225+0.0415*Cload	0.4290+0.0414*Cload
I_PAD_T$_{PHL}${DS0&DS1&!DS2&SL}	0.7340+0.0489*Cload	0.8295+0.0421*Cload	0.8590+0.0415*Cload
I_PAD_T$_{PHL}${DS0&DS1&DS2&!SL}	0.3806+0.0232*Cload	0.4086+0.0212*Cload	0.4150+0.0211*Cload
I_PAD_T$_{PHL}${DS0&DS1&DS2&SL}	0.6888+0.0303*Cload	0.8005+0.0227*Cload	0.8680+0.0213*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&!DS2&!SL}	0.3601+0.0697*Cload	0.3725+0.0687*Cload	0.3720+0.0687*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&!DS2&SL}	0.9120+0.0766*Cload	1.0090+0.0694*Cload	1.0320+0.0689*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&DS2&!SL}	0.3036+0.0148*Cload	0.3132+0.0141*Cload	0.3190+0.0140*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&DS2&SL}	0.7330+0.0271*Cload	0.8875+0.0167*Cload	0.9930+0.0146*Cload
I_PAD_T$_{PLH}${!DS0&DS1&!DS2&!SL}	0.3086+0.0239*Cload	0.3185+0.0232*Cload	0.3240+0.0231*Cload
I_PAD_T$_{PLH}${!DS0&DS1&!DS2&SL}	0.7698+0.0353*Cload	0.9165+0.0251*Cload	1.0000+0.0234*Cload
I_PAD_T$_{PLH}${!DS0&DS1&DS2&!SL}	0.3013+0.0110*Cload	0.3119+0.0102*Cload	0.3160+0.0101*Cload
I_PAD_T$_{PLH}${!DS0&DS1&DS2&SL}	0.7198+0.0233*Cload	0.8705+0.0133*Cload	0.9860+0.0110*Cload
I_PAD_T$_{PLH}${DS0&!DS1&!DS2&!SL}	0.3202+0.0352*Cload	0.3305+0.0345*Cload	0.3350+0.0344*Cload
I_PAD_T$_{PLH}${DS0&!DS1&!DS2&SL}	0.8140+0.0454*Cload	0.9490+0.0358*Cload	1.0070+0.0346*Cload
I_PAD_T$_{PLH}${DS0&!DS1&DS2&!SL}	0.3019+0.0126*Cload	0.3123+0.0118*Cload	0.3180+0.0117*Cload
I_PAD_T$_{PLH}${DS0&!DS1&DS2&SL}	0.7263+0.0248*Cload	0.8775+0.0147*Cload	0.9950+0.0124*Cload
I_PAD_T$_{PLH}${DS0&DS1&!DS2&!SL}	0.3041+0.0182*Cload	0.3122+0.0176*Cload	0.3150+0.0175*Cload
I_PAD_T$_{PLH}${DS0&DS1&!DS2&SL}	0.7471+0.0302*Cload	0.8975+0.0199*Cload	0.9960+0.0179*Cload
I_PAD_T$_{PLH}${DS0&DS1&DS2&!SL}	0.3010+0.0099*Cload	0.3150+0.0089*Cload	0.3157+0.0089*Cload
I_PAD_T$_{PLH}${DS0&DS1&DS2&SL}	0.7183+0.0221*Cload	0.8665+0.0123*Cload	0.9860+0.0099*Cload
Timing Arc	**(< 10)pf**	**(10-70)pf**	**(> 70)pf**
OE_PAD_T$_{PHZ}${!DS0&!DS1&!DS2&!SL}	0.1928	0.1930	0.1932
OE_PAD_T$_{PHZ}${!DS0&!DS1&!DS2&SL}	0.1928	0.1930	0.1932
OE_PAD_T$_{PHZ}${!DS0&!DS1&DS2&!SL}	0.1898	0.1900	0.1902
OE_PAD_T$_{PHZ}${!DS0&!DS1&DS2&SL}	0.1898	0.1900	0.1902
OE_PAD_T$_{PHZ}${!DS0&DS1&!DS2&!SL}	0.1934	0.1936	0.1938
OE_PAD_T$_{PHZ}${!DS0&DS1&!DS2&SL}	0.1934	0.1936	0.1938
OE_PAD_T$_{PHZ}${!DS0&DS1&DS2&!SL}	0.1912	0.1914	0.1916
OE_PAD_T$_{PHZ}${!DS0&DS1&DS2&SL}	0.1911	0.1913	0.1915
OE_PAD_T$_{PHZ}${DS0&!DS1&!DS2&!SL}	0.1954	0.1956	0.1958
OE_PAD_T$_{PHZ}${DS0&!DS1&!DS2&SL}	0.1954	0.1956	0.1958
OE_PAD_T$_{PHZ}${DS0&!DS1&DS2&!SL}	0.1907	0.1909	0.1911
OE_PAD_T$_{PHZ}${DS0&!DS1&DS2&SL}	0.1907	0.1909	0.1911
OE_PAD_T$_{PHZ}${DS0&DS1&!DS2&!SL}	0.1947	0.1949	0.1951
OE_PAD_T$_{PHZ}${DS0&DS1&!DS2&SL}	0.1946	0.1948	0.1950
OE_PAD_T$_{PHZ}${DS0&DS1&DS2&!SL}	0.1923	0.1925	0.1927
OE_PAD_T$_{PHZ}${DS0&DS1&DS2&SL}	0.1923	0.1925	0.1927
OE_PAD_T$_{PLZ}${!DS0&!DS1&!DS2&!SL}	0.2272	0.2274	0.2276
OE_PAD_T$_{PLZ}${!DS0&!DS1&!DS2&SL}	0.2268	0.2270	0.2272
OE_PAD_T$_{PLZ}${!DS0&!DS1&DS2&!SL}	0.2108	0.2110	0.2112
OE_PAD_T$_{PLZ}${!DS0&!DS1&DS2&SL}	0.2102	0.2104	0.2106
OE_PAD_T$_{PLZ}${!DS0&DS1&!DS2&!SL}	0.2303	0.2305	0.2307
OE_PAD_T$_{PLZ}${!DS0&DS1&!DS2&SL}	0.2298	0.2300	0.2302
OE_PAD_T$_{PLZ}${!DS0&DS1&DS2&!SL}	0.2118	0.2120	0.2122
OE_PAD_T$_{PLZ}${!DS0&DS1&DS2&SL}	0.2112	0.2114	0.2116
OE_PAD_T$_{PLZ}${DS0&!DS1&!DS2&!SL}	0.2295	0.2297	0.2299
OE_PAD_T$_{PLZ}${DS0&!DS1&!DS2&SL}	0.2291	0.2293	0.2295
OE_PAD_T$_{PLZ}${DS0&!DS1&DS2&!SL}	0.2108	0.2110	0.2112

Continued...

	Group1	**Group2**	**Group3**
OE_PAD_T$_{PLZ}${DS0&!DS1&DS2&SL}	0.2102	0.2104	0.2106
OE_PAD_T$_{PLZ}${DS0&DS1&!DS2&!SL}	0.2284	0.2286	0.2288
OE_PAD_T$_{PLZ}${DS0&DS1&!DS2&SL}	0.2279	0.2281	0.2283
OE_PAD_T$_{PLZ}${DS0&DS1&DS2&!SL}	0.2118	0.2120	0.2122
OE_PAD_T$_{PLZ}${DS0&DS1&DS2&SL}	0.2111	0.2113	0.2115
OE_PAD_T$_{PZH}${!DS0&!DS1&!DS2&!SL}	0.3481+0.0696*Cload	0.3595+0.0687*Cload	0.3610+0.0687*Cload
OE_PAD_T$_{PZH}${!DS0&!DS1&!DS2&SL}	0.8910+0.0766*Cload	0.9880+0.0694*Cload	1.0120+0.0689*Cload
OE_PAD_T$_{PZH}${!DS0&!DS1&DS2&!SL}	0.2946+0.0148*Cload	0.3042+0.0141*Cload	0.3100+0.0140*Cload
OE_PAD_T$_{PZH}${!DS0&!DS1&DS2&SL}	0.7161+0.0271*Cload	0.8705+0.0167*Cload	0.9760+0.0146*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&!DS2&!SL}	0.2999+0.0238*Cload	0.3090+0.0232*Cload	0.3140+0.0231*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&!DS2&SL}	0.7511+0.0355*Cload	0.9020+0.0250*Cload	0.9810+0.0234*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&DS2&!SL}	0.2919+0.0111*Cload	0.3032+0.0102*Cload	0.3070+0.0101*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&DS2&SL}	0.7024+0.0233*Cload	0.8535+0.0133*Cload	0.9690+0.0110*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&!DS2&!SL}	0.3103+0.0352*Cload	0.3205+0.0345*Cload	0.3250+0.0344*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&!DS2&SL}	0.7960+0.0454*Cload	0.9300+0.0358*Cload	0.9880+0.0346*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&DS2&!SL}	0.2930+0.0126*Cload	0.3036+0.0118*Cload	0.3090+0.0117*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&DS2&SL}	0.7086+0.0249*Cload	0.8615+0.0147*Cload	0.9710+0.0125*Cload
OE_PAD_T$_{PZH}${DS0&DS1&!DS2&!SL}	0.2951+0.0182*Cload	0.3056+0.0175*Cload	0.3060+0.0175*Cload
OE_PAD_T$_{PZH}${DS0&DS1&!DS2&SL}	0.7288+0.0303*Cload	0.8830+0.0198*Cload	0.9780+0.0179*Cload
OE_PAD_T$_{PZH}${DS0&DS1&DS2&!SL}	0.2922+0.0099*Cload	0.3038+0.0090*Cload	0.3071+0.0089*Cload
OE_PAD_T$_{PZH}${DS0&DS1&DS2&SL}	0.7000+0.0222*Cload	0.8495+0.0123*Cload	0.9770+0.0098*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&!DS2&!SL}	0.5180+0.1648*Cload	0.5315+0.1637*Cload	0.5590+0.1633*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&!DS2&SL}	0.9030+0.1670*Cload	0.9410+0.1640*Cload	0.9300+0.1640*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&DS2&!SL}	0.3913+0.0349*Cload	0.4125+0.0333*Cload	0.4170+0.0332*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&DS2&SL}	0.7119+0.0417*Cload	0.8205+0.0341*Cload	0.8590+0.0333*Cload
OE_PAD_T$_{PZL}${!DS0&DS1&!DS2&!SL}	0.4063+0.0564*Cload	0.4245+0.0551*Cload	0.4300+0.0550*Cload
OE_PAD_T$_{PZL}${!DS0&DS1&!DS2&SL}	0.7410+0.0620*Cload	0.8305+0.0555*Cload	0.8510+0.0551*Cload
OE_PAD_T$_{PZL}${!DS0&DS1&DS2&!SL}	0.3801+0.0261*Cload	0.4060+0.0242*Cload	0.4170+0.0240*Cload
OE_PAD_T$_{PZL}${!DS0&DS1&DS2&SL}	0.6851+0.0334*Cload	0.7995+0.0255*Cload	0.8620+0.0242*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&!DS2&!SL}	0.4341+0.0835*Cload	0.4515+0.0823*Cload	0.4580+0.0822*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&!DS2&SL}	0.7960+0.0878*Cload	0.8625+0.0827*Cload	0.8760+0.0824*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&DS2&!SL}	0.3848+0.0297*Cload	0.4085+0.0279*Cload	0.4190+0.0277*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&DS2&SL}	0.7011+0.0368*Cload	0.8155+0.0289*Cload	0.8640+0.0279*Cload
OE_PAD_T$_{PZL}${DS0&DS1&!DS2&!SL}	0.3917+0.0430*Cload	0.4090+0.0416*Cload	0.4180+0.0414*Cload
OE_PAD_T$_{PZL}${DS0&DS1&!DS2&SL}	0.7159+0.0494*Cload	0.8185+0.0421*Cload	0.8490+0.0415*Cload
OE_PAD_T$_{PZL}${DS0&DS1&DS2&!SL}	0.3771+0.0233*Cload	0.4035+0.0213*Cload	0.4120+0.0211*Cload
OE_PAD_T$_{PZL}${DS0&DS1&DS2&SL}	0.6798+0.0308*Cload	0.7975+0.0227*Cload	0.8660+0.0213*Cload
Timing Arc	**(< 0.03)pf**	**(0.03-0.3)pf**	**(> 0.3)pf**
PAD_C_T$_{PHL}${!ST}	0.2496+0.4850*Cload	0.2493+0.4920*Cload	0.2500+0.4900*Cload
PAD_C_T$_{PHL}${ST}	0.5344+0.4650*Cload	0.5337+0.4900*Cload	0.5342+0.4890*Cload
PAD_C_T$_{PLH}${!ST}	0.3352+0.4650*Cload	0.3352+0.4620*Cload	0.3354+0.4625*Cload
PAD_C_T$_{PLH}${ST}	0.5689+0.4650*Cload	0.5690+0.4620*Cload	0.5683+0.4650*Cload

9.25 PRWDWUWSWEWCODCDGSH_H

Core overdrive 1.2V, Regular I/O with POC. (When in POC mode, output = Z, pull resistors = disabled.)



Truth Table

INPUT																							OUTPUT	
VDD	VDDPST12	VDDPST08	VDDPST04	ESDB	ESD12	ESD12B	POCCTRL	POCCTRLD	POCCTRL12	RTE	DS3	DS2	DS1	DS0	SL	OE	I	PD	PU	SPU	PAD	ST	IE	PAD	C
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	1	0	0/1	0/1	0/1	-	0/1	0/1	0	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	1	1	0/1	0/1	0/1	-	0/1	1	1	1
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	1	1	0/1	0/1	0/1	-	0/1	0	1	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	0/1	0/1	0/1	0	0/1	0/1	-	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	0/1	0/1	0/1	1	0/1	0	-	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	0/1	0/1	0/1	1	0/1	1	-	1
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	0	0	0	Z	0/1	0	-	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	0	0	0	Z	0/1	1	-	X
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	1	0	0	Z	0/1	0	L	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	1	0	0	Z	0/1	1	L	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	0	1	0	Z	0/1	0	H	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	0	1	0	Z	0/1	1	H	1
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	1	1	0	Z	0/1	0	previous-state	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	1	1	0	Z	0/1	1	previous-state	previous-state
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	0/1	0/1	1	Z	0/1	0	Strong-H	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	0/1	0/1	1	Z	0/1	1	Strong-H	1
1	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	-	0/1	0/1	X	0
0	1	1	1	1	0	1	1	1	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	Z	X
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch1	Latch0	Latch	Latch	Latch	-	Latch	Latch	0	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch1	Latch1	Latch	Latch	Latch	-	Latch	Latch1	1	1
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch1	Latch1	Latch	Latch	Latch	-	Latch	Latch0	1	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	Latch	0	Latch	Latch	-	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	Latch	1	Latch	Latch0	-	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	Latch	1	Latch	Latch1	-	1
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch0	Latch0	Z	Latch	Latch0	-	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch0	Latch0	Z	Latch	Latch1	-	X
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch0	Latch0	Z	Latch	Latch0	L	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch0	Latch0	Z	Latch	Latch1	L	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch1	Latch0	Z	Latch	Latch0	H	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch1	Latch0	Z	Latch	Latch1	H	1
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch1	Latch0	Z	Latch	Latch0	previous-state	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch1	Latch0	Z	Latch	Latch1	previous-state	previous-state
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	Latch1	Z	Latch	Latch0	Strong-H	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	Latch1	Z	Latch	Latch1	Strong-H	1
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch1	Latch0	Latch	Latch	Latch	-	Latch	Latch	0	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch1	Latch1	Latch	Latch	Latch	-	Latch	Latch1	1	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch1	Latch1	Latch	Latch	Latch	-	Latch	Latch0	1	X

Continued...

VDD	VDDPST12	VDDPST08	VDDPST04	ESDB	ESD12	ESD12B	POCCTRL	POCCTRLD	POCCTRL12	RTE	DS3	DS2	DS1	DS0	SL	OE	I	PD	PU	SPU	PAD	ST	IE	PAD	C
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	Latch	0	Latch	Latch	-	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	Latch	1	Latch	Latch0	-	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	Latch	1	Latch	Latch1	-	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch0	Latch0	Z	Latch	Latch0	-	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch0	Latch0	Z	Latch	Latch1	-	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch0	Latch0	Z	Latch	Latch0	L	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch0	Latch0	Z	Latch	Latch1	L	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch1	Latch0	Z	Latch	Latch0	H	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch1	Latch0	Z	Latch	Latch1	H	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch1	Latch0	Z	Latch	Latch0	previous-state	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch1	Latch0	Z	Latch	Latch1	previous-state	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	Latch1	Z	Latch	Latch0	Strong-H	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	Latch1	Z	Latch	Latch1	Strong-H	X
1	0	1	1	1	0	0	1	1	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	-	0/1	0/1	X	0
0	0	1	1	1	0	0	1	1	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X
1	0	1	0	1	0	0	1	1	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	-	0/1	0/1	X	0
0	0	1	0	1	0	0	1	1	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X
1	0	0	1	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	-	0/1	0/1	X	0
0	0	0	1	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X
0	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X

*All undefined states in truth table are illegal operation

Cell Information

	Value	Unit
Cell Width	55.584	um
Cell Height	17.68	um
Pad Number	1	-

Leakage Power

	Value	Unit
VDDPST12	2.134e+04	nW

Pin Capacitance

	Value	Unit
DS0	0.00573	pF
DS1	0.005433	pF
DS2	0.005422	pF
DS3	0.005231	pF
ESD12	0.008586	pF
ESD12B	0.01011	pF
ESDB	0.00939	pF
I	0.005334	pF
IE	0.005278	pF
OE	0.004978	pF
PAD	1.309	pF
PD	0.004188	pF
POCCTRL	0.007209	pF
POCCTRL12	0.009582	pF
POCCTRLD	0.007136	pF
PU	0.005058	pF
RTE	0.006737	pF
SL	0.00515	pF
SPU	0.004734	pF
ST	0.005062	pF

Propagation Delay

	Group1	Group2	Group3
Timing Arc	**(< 0.03)pf**	**(0.03-0.3)pf**	**(> 0.3)pf**
IE_C_T$_{PHL}${!ST}	0.1117+0.3100*Cload	0.1118+0.3080*Cload	0.1117+0.3090*Cload
IE_C_T$_{PHL}${ST}	0.1117+0.3100*Cload	0.1118+0.3080*Cload	0.1115+0.3095*Cload
IE_C_T$_{PLH}${!ST}	0.3050+0.2850*Cload	0.3053+0.2760*Cload	0.3047+0.2785*Cload
IE_C_T$_{PLH}${ST}	0.3347+0.2850*Cload	0.3349+0.2760*Cload	0.3348+0.2770*Cload
Timing Arc	**(< 10)pf**	**(10-70)pf**	**(> 70)pf**

Continued...

	Group1	Group2	Group3
I_PAD_T$_{PHL}${!DS0&!DS1&!DS2&!DS3&!SL}	0.6380+0.1638*Cload	0.6585+0.1623*Cload	0.6490+0.1623*Cload
I_PAD_T$_{PHL}${!DS0&!DS1&!DS2&!DS3&SL}	1.2770+0.1680*Cload	1.3410+0.1630*Cload	1.3510+0.1627*Cload
I_PAD_T$_{PHL}${!DS0&!DS1&!DS2&DS3&!SL}	0.3868+0.0206*Cload	0.4126+0.0187*Cload	0.4220+0.0185*Cload
I_PAD_T$_{PHL}${!DS0&!DS1&!DS2&DS3&SL}	0.8690+0.0316*Cload	1.0200+0.0214*Cload	1.1340+0.0191*Cload
I_PAD_T$_{PHL}${!DS0&!DS1&DS2&!DS3&!SL}	0.4064+0.0344*Cload	0.4260+0.0330*Cload	0.4370+0.0328*Cload
I_PAD_T$_{PHL}${!DS0&!DS1&DS2&!DS3&SL}	0.9260+0.0448*Cload	1.0710+0.0348*Cload	1.1540+0.0331*Cload
I_PAD_T$_{PHL}${!DS0&!DS1&DS2&DS3&!SL}	0.3839+0.0154*Cload	0.4147+0.0132*Cload	0.4240+0.0130*Cload
I_PAD_T$_{PHL}${!DS0&!DS1&DS2&DS3&SL}	0.8590+0.0266*Cload	1.0110+0.0164*Cload	1.1380+0.0139*Cload
I_PAD_T$_{PHL}${!DS0&DS1&!DS2&!DS3&!SL}	0.4406+0.0558*Cload	0.4580+0.0546*Cload	0.4680+0.0544*Cload
I_PAD_T$_{PHL}${!DS0&DS1&!DS2&!DS3&SL}	1.0000+0.0646*Cload	1.1300+0.0556*Cload	1.1720+0.0547*Cload
I_PAD_T$_{PHL}${!DS0&DS1&!DS2&DS3&!SL}	0.3834+0.0175*Cload	0.4107+0.0155*Cload	0.4260+0.0152*Cload
I_PAD_T$_{PHL}${!DS0&DS1&!DS2&DS3&SL}	0.8630+0.0284*Cload	1.0115+0.0185*Cload	1.1360+0.0160*Cload
I_PAD_T$_{PHL}${!DS0&DS1&DS2&!DS3&!SL}	0.3917+0.0253*Cload	0.4145+0.0237*Cload	0.4200+0.0236*Cload
I_PAD_T$_{PHL}${!DS0&DS1&DS2&!DS3&SL}	0.8940+0.0360*Cload	1.0405+0.0261*Cload	1.1440+0.0240*Cload
I_PAD_T$_{PHL}${!DS0&DS1&DS2&DS3&!SL}	0.3834+0.0139*Cload	0.4155+0.0116*Cload	0.4300+0.0113*Cload
I_PAD_T$_{PHL}${!DS0&DS1&DS2&DS3&SL}	0.8589+0.0250*Cload	1.0080+0.0150*Cload	1.1380+0.0124*Cload
I_PAD_T$_{PHL}${DS0&!DS1&!DS2&!DS3&!SL}	0.4881+0.0831*Cload	0.5070+0.0818*Cload	0.5180+0.0816*Cload
I_PAD_T$_{PHL}${DS0&!DS1&!DS2&!DS3&SL}	1.0780+0.0906*Cload	1.1885+0.0825*Cload	1.2190+0.0819*Cload
I_PAD_T$_{PHL}${DS0&!DS1&!DS2&DS3&!SL}	0.3844+0.0189*Cload	0.4121+0.0169*Cload	0.4230+0.0167*Cload
I_PAD_T$_{PHL}${DS0&!DS1&!DS2&DS3&SL}	0.8640+0.0300*Cload	1.0150+0.0198*Cload	1.1350+0.0174*Cload
I_PAD_T$_{PHL}${DS0&!DS1&DS2&!DS3&!SL}	0.3969+0.0291*Cload	0.4170+0.0276*Cload	0.4270+0.0274*Cload
I_PAD_T$_{PHL}${DS0&!DS1&DS2&!DS3&SL}	0.9070+0.0396*Cload	1.0535+0.0297*Cload	1.1450+0.0278*Cload
I_PAD_T$_{PHL}${DS0&!DS1&DS2&DS3&!SL}	0.3832+0.0146*Cload	0.4157+0.0123*Cload	0.4260+0.0121*Cload
I_PAD_T$_{PHL}${DS0&!DS1&DS2&DS3&SL}	0.8589+0.0257*Cload	1.0110+0.0156*Cload	1.1370+0.0131*Cload
I_PAD_T$_{PHL}${DS0&DS1&!DS2&!DS3&!SL}	0.4170+0.0425*Cload	0.4335+0.0413*Cload	0.4430+0.0411*Cload
I_PAD_T$_{PHL}${DS0&DS1&!DS2&!DS3&SL}	0.9540+0.0524*Cload	1.0935+0.0427*Cload	1.1540+0.0414*Cload
I_PAD_T$_{PHL}${DS0&DS1&!DS2&DS3&!SL}	0.3821+0.0164*Cload	0.4107+0.0143*Cload	0.4260+0.0140*Cload
I_PAD_T$_{PHL}${DS0&DS1&!DS2&DS3&SL}	0.8601+0.0274*Cload	1.0125+0.0173*Cload	1.1340+0.0149*Cload
I_PAD_T$_{PHL}${DS0&DS1&DS2&!DS3&!SL}	0.3878+0.0225*Cload	0.4093+0.0209*Cload	0.4180+0.0207*Cload
I_PAD_T$_{PHL}${DS0&DS1&DS2&!DS3&SL}	0.8830+0.0334*Cload	1.0320+0.0234*Cload	1.1410+0.0212*Cload
I_PAD_T$_{PHL}${DS0&DS1&DS2&DS3&!SL}	0.3835+0.0133*Cload	0.4174+0.0109*Cload	0.4260+0.0107*Cload
I_PAD_T$_{PHL}${DS0&DS1&DS2&DS3&SL}	0.8598+0.0243*Cload	1.0090+0.0144*Cload	1.1390+0.0118*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&!DS2&!DS3&!SL}	0.3910+0.0713*Cload	0.4115+0.0697*Cload	0.4140+0.0696*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&!DS2&!DS3&SL}	1.4620+0.0910*Cload	1.7260+0.0724*Cload	1.8320+0.0702*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&!DS2&DS3&!SL}	0.3098+0.0096*Cload	0.3293+0.0083*Cload	0.3406+0.0081*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&!DS2&DS3&SL}	1.0460+0.0300*Cload	1.2715+0.0151*Cload	1.5070+0.0105*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&DS2&!DS3&!SL}	0.3126+0.0156*Cload	0.3284+0.0145*Cload	0.3390+0.0143*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&DS2&!DS3&SL}	1.1060+0.0376*Cload	1.3660+0.0206*Cload	1.5930+0.0161*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&DS2&DS3&!SL}	0.3097+0.0074*Cload	0.3299+0.0060*Cload	0.3384+0.0058*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&DS2&DS3&SL}	1.0290+0.0268*Cload	1.2410+0.0128*Cload	1.4630+0.0085*Cload
I_PAD_T$_{PLH}${!DS0&DS1&!DS2&!DS3&!SL}	0.3225+0.0248*Cload	0.3392+0.0237*Cload	0.3490+0.0235*Cload
I_PAD_T$_{PLH}${!DS0&DS1&!DS2&!DS3&SL}	1.1850+0.0480*Cload	1.4730+0.0288*Cload	1.6730+0.0248*Cload
I_PAD_T$_{PLH}${!DS0&DS1&!DS2&DS3&!SL}	0.3088+0.0083*Cload	0.3272+0.0070*Cload	0.3415+0.0067*Cload
I_PAD_T$_{PLH}${!DS0&DS1&!DS2&DS3&SL}	1.0360+0.0280*Cload	1.2545+0.0137*Cload	1.4830+0.0093*Cload
I_PAD_T$_{PLH}${!DS0&DS1&DS2&!DS3&!SL}	0.3087+0.0116*Cload	0.3254+0.0105*Cload	0.3370+0.0103*Cload
I_PAD_T$_{PLH}${!DS0&DS1&DS2&!DS3&SL}	1.0680+0.0328*Cload	1.3075+0.0171*Cload	1.5400+0.0125*Cload
I_PAD_T$_{PLH}${!DS0&DS1&DS2&DS3&!SL}	0.3107+0.0067*Cload	0.3316+0.0053*Cload	0.3469+0.0050*Cload
I_PAD_T$_{PLH}${!DS0&DS1&DS2&DS3&SL}	1.0270+0.0258*Cload	1.2345+0.0121*Cload	1.4520+0.0079*Cload
I_PAD_T$_{PLH}${DS0&!DS1&!DS2&!DS3&!SL}	0.3391+0.0364*Cload	0.3580+0.0352*Cload	0.3680+0.0350*Cload
I_PAD_T$_{PLH}${DS0&!DS1&!DS2&!DS3&SL}	1.2710+0.0594*Cload	1.5615+0.0395*Cload	1.7330+0.0360*Cload
I_PAD_T$_{PLH}${DS0&!DS1&!DS2&DS3&!SL}	0.3093+0.0089*Cload	0.3279+0.0076*Cload	0.3370+0.0074*Cload
I_PAD_T$_{PLH}${DS0&!DS1&!DS2&DS3&SL}	1.0400+0.0290*Cload	1.2610+0.0144*Cload	1.4910+0.0099*Cload
I_PAD_T$_{PLH}${DS0&!DS1&DS2&!DS3&!SL}	0.3100+0.0132*Cload	0.3242+0.0122*Cload	0.3390+0.0119*Cload
I_PAD_T$_{PLH}${DS0&!DS1&DS2&!DS3&SL}	1.0830+0.0348*Cload	1.3325+0.0185*Cload	1.5670+0.0139*Cload
I_PAD_T$_{PLH}${DS0&!DS1&DS2&DS3&!SL}	0.3103+0.0070*Cload	0.3313+0.0056*Cload	0.3408+0.0054*Cload
I_PAD_T$_{PLH}${DS0&!DS1&DS2&DS3&SL}	1.0270+0.0264*Cload	1.2380+0.0124*Cload	1.4550+0.0082*Cload
I_PAD_T$_{PLH}${DS0&DS1&!DS2&!DS3&!SL}	0.3151+0.0190*Cload	0.3297+0.0180*Cload	0.3380+0.0178*Cload
I_PAD_T$_{PLH}${DS0&DS1&!DS2&!DS3&SL}	1.1370+0.0418*Cload	1.4105+0.0237*Cload	1.6310+0.0193*Cload

Continued...

	Group1	Group2	Group3
I_PAD_T$_{PLH}${DS0&DS1&!DS2&DS3&!SL}	0.3091+0.0078*Cload	0.3300+0.0064*Cload	0.3413+0.0062*Cload
I_PAD_T$_{PLH}${DS0&DS1&!DS2&DS3&SL}	1.0320+0.0274*Cload	1.2455+0.0133*Cload	1.4720+0.0089*Cload
I_PAD_T$_{PLH}${DS0&DS1&DS2&!DS3&!SL}	0.3077+0.0104*Cload	0.3234+0.0093*Cload	0.3324+0.0091*Cload
I_PAD_T$_{PLH}${DS0&DS1&DS2&!DS3&SL}	1.0560+0.0312*Cload	1.2895+0.0159*Cload	1.5200+0.0114*Cload
I_PAD_T$_{PLH}${DS0&DS1&DS2&DS3&!SL}	0.3111+0.0065*Cload	0.3331+0.0050*Cload	0.3492+0.0047*Cload
I_PAD_T$_{PLH}${DS0&DS1&DS2&DS3&SL}	1.0260+0.0256*Cload	1.2330+0.0118*Cload	1.4450+0.0077*Cload
Timing Arc	**(< 10)pf**	**(10-70)pf**	**(> 70)pf**
OE_PAD_T$_{PHZ}${!DS0&!DS1&!DS2&!DS3&!SL}	0.1795	0.1797	0.1799
OE_PAD_T$_{PHZ}${!DS0&!DS1&!DS2&!DS3&SL}	0.1797	0.1799	0.1801
OE_PAD_T$_{PHZ}${!DS0&!DS1&!DS2&DS3&!SL}	0.1889	0.1891	0.1893
OE_PAD_T$_{PHZ}${!DS0&!DS1&!DS2&DS3&SL}	0.1888	0.1890	0.1892
OE_PAD_T$_{PHZ}${!DS0&!DS1&DS2&!DS3&!SL}	0.1814	0.1816	0.1818
OE_PAD_T$_{PHZ}${!DS0&!DS1&DS2&!DS3&SL}	0.1814	0.1816	0.1818
OE_PAD_T$_{PHZ}${!DS0&!DS1&DS2&DS3&!SL}	0.1952	0.1954	0.1956
OE_PAD_T$_{PHZ}${!DS0&!DS1&DS2&DS3&SL}	0.1946	0.1948	0.1950
OE_PAD_T$_{PHZ}${!DS0&DS1&!DS2&!DS3&!SL}	0.1846	0.1848	0.1850
OE_PAD_T$_{PHZ}${!DS0&DS1&!DS2&!DS3&SL}	0.1846	0.1848	0.1850
OE_PAD_T$_{PHZ}${!DS0&DS1&!DS2&DS3&!SL}	0.1926	0.1928	0.1930
OE_PAD_T$_{PHZ}${!DS0&DS1&!DS2&DS3&SL}	0.1923	0.1925	0.1927
OE_PAD_T$_{PHZ}${!DS0&DS1&DS2&!DS3&!SL}	0.1852	0.1854	0.1856
OE_PAD_T$_{PHZ}${!DS0&DS1&DS2&!DS3&SL}	0.1852	0.1854	0.1856
OE_PAD_T$_{PHZ}${!DS0&DS1&DS2&DS3&!SL}	0.1998	0.2000	0.2002
OE_PAD_T$_{PHZ}${!DS0&DS1&DS2&DS3&SL}	0.1989	0.1991	0.1993
OE_PAD_T$_{PHZ}${DS0&!DS1&!DS2&!DS3&!SL}	0.1845	0.1847	0.1849
OE_PAD_T$_{PHZ}${DS0&!DS1&!DS2&!DS3&SL}	0.1845	0.1847	0.1849
OE_PAD_T$_{PHZ}${DS0&!DS1&!DS2&DS3&!SL}	0.1911	0.1913	0.1915
OE_PAD_T$_{PHZ}${DS0&!DS1&!DS2&DS3&SL}	0.1908	0.1910	0.1912
OE_PAD_T$_{PHZ}${DS0&!DS1&DS2&!DS3&!SL}	0.1835	0.1837	0.1839
OE_PAD_T$_{PHZ}${DS0&!DS1&DS2&!DS3&SL}	0.1835	0.1837	0.1839
OE_PAD_T$_{PHZ}${DS0&!DS1&DS2&DS3&!SL}	0.1979	0.1981	0.1983
OE_PAD_T$_{PHZ}${DS0&!DS1&DS2&DS3&SL}	0.1971	0.1973	0.1975
OE_PAD_T$_{PHZ}${DS0&DS1&!DS2&!DS3&!SL}	0.1873	0.1875	0.1877
OE_PAD_T$_{PHZ}${DS0&DS1&!DS2&!DS3&SL}	0.1872	0.1874	0.1876
OE_PAD_T$_{PHZ}${DS0&DS1&!DS2&DS3&!SL}	0.1951	0.1953	0.1955
OE_PAD_T$_{PHZ}${DS0&DS1&!DS2&DS3&SL}	0.1946	0.1948	0.1950
OE_PAD_T$_{PHZ}${DS0&DS1&DS2&!DS3&!SL}	0.1879	0.1881	0.1883
OE_PAD_T$_{PHZ}${DS0&DS1&DS2&!DS3&SL}	0.1878	0.1880	0.1882
OE_PAD_T$_{PHZ}${DS0&DS1&DS2&DS3&!SL}	0.2024	0.2026	0.2028
OE_PAD_T$_{PHZ}${DS0&DS1&DS2&DS3&SL}	0.2014	0.2016	0.2018
OE_PAD_T$_{PLZ}${!DS0&!DS1&!DS2&!DS3&!SL}	0.2046	0.2048	0.2050
OE_PAD_T$_{PLZ}${!DS0&!DS1&!DS2&!DS3&SL}	0.2040	0.2042	0.2044
OE_PAD_T$_{PLZ}${!DS0&!DS1&!DS2&DS3&!SL}	0.1935	0.1937	0.1939
OE_PAD_T$_{PLZ}${!DS0&!DS1&!DS2&DS3&SL}	0.1927	0.1929	0.1931
OE_PAD_T$_{PLZ}${!DS0&!DS1&DS2&!DS3&!SL}	0.1895	0.1897	0.1899
OE_PAD_T$_{PLZ}${!DS0&!DS1&DS2&!DS3&SL}	0.1890	0.1892	0.1894
OE_PAD_T$_{PLZ}${!DS0&!DS1&DS2&DS3&!SL}	0.1939	0.1941	0.1943
OE_PAD_T$_{PLZ}${!DS0&!DS1&DS2&DS3&SL}	0.1931	0.1933	0.1935
OE_PAD_T$_{PLZ}${!DS0&DS1&!DS2&!DS3&!SL}	0.1969	0.1971	0.1973
OE_PAD_T$_{PLZ}${!DS0&DS1&!DS2&!DS3&SL}	0.1963	0.1965	0.1967
OE_PAD_T$_{PLZ}${!DS0&DS1&!DS2&DS3&!SL}	0.1937	0.1939	0.1941
OE_PAD_T$_{PLZ}${!DS0&DS1&!DS2&DS3&SL}	0.1929	0.1931	0.1933
OE_PAD_T$_{PLZ}${!DS0&DS1&DS2&!DS3&!SL}	0.1889	0.1891	0.1893
OE_PAD_T$_{PLZ}${!DS0&DS1&DS2&!DS3&SL}	0.1884	0.1886	0.1888
OE_PAD_T$_{PLZ}${!DS0&DS1&DS2&DS3&!SL}	0.1941	0.1943	0.1945
OE_PAD_T$_{PLZ}${!DS0&DS1&DS2&DS3&SL}	0.1933	0.1935	0.1937
OE_PAD_T$_{PLZ}${DS0&!DS1&!DS2&!DS3&!SL}	0.2104	0.2106	0.2108
OE_PAD_T$_{PLZ}${DS0&!DS1&!DS2&!DS3&SL}	0.2096	0.2098	0.2100

Continued...

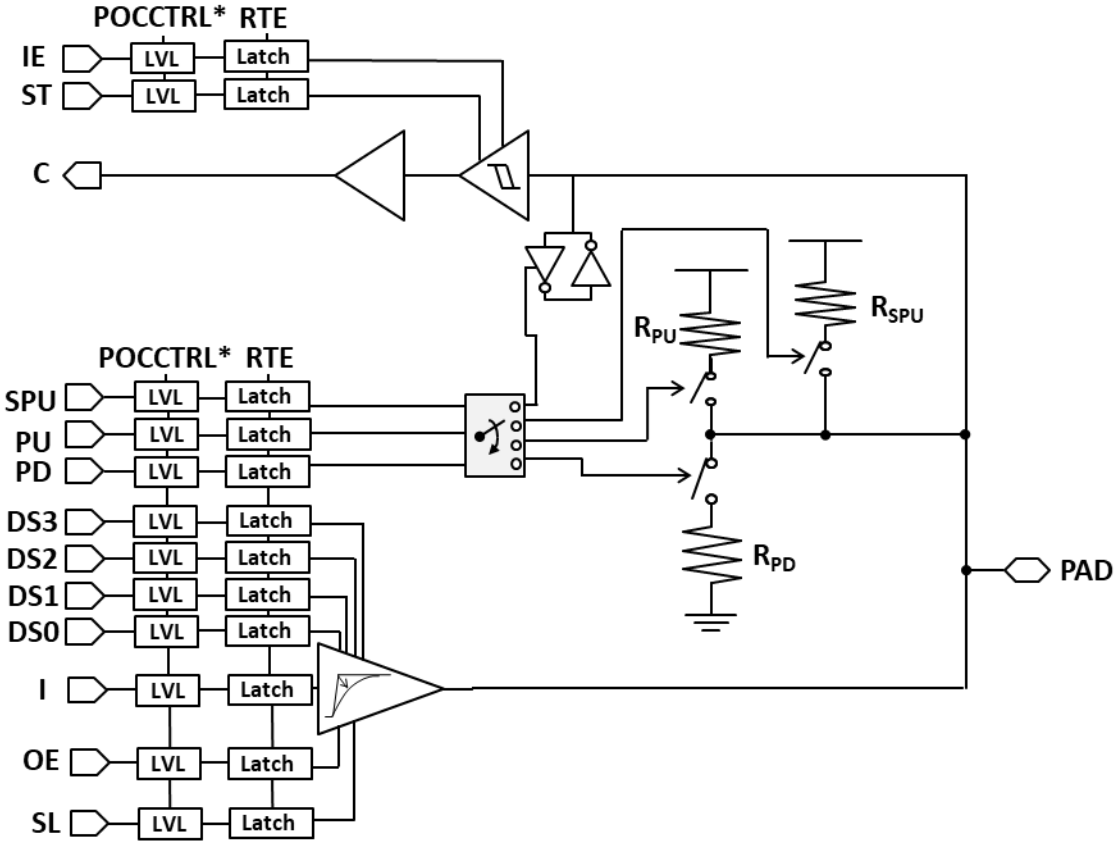
	Group1	Group2	Group3
OE_PAD_T$_{PLZ}${DS0&!DS1&!DS2&DS3&!SL}	0.1939	0.1941	0.1943
OE_PAD_T$_{PLZ}${DS0&!DS1&!DS2&DS3&SL}	0.1932	0.1934	0.1936
OE_PAD_T$_{PLZ}${DS0&!DS1&DS2&!DS3&!SL}	0.1893	0.1895	0.1897
OE_PAD_T$_{PLZ}${DS0&!DS1&DS2&!DS3&SL}	0.1889	0.1891	0.1893
OE_PAD_T$_{PLZ}${DS0&!DS1&DS2&DS3&!SL}	0.1943	0.1945	0.1947
OE_PAD_T$_{PLZ}${DS0&!DS1&DS2&DS3&SL}	0.1936	0.1938	0.1940
OE_PAD_T$_{PLZ}${DS0&DS1&!DS2&!DS3&!SL}	0.1964	0.1966	0.1968
OE_PAD_T$_{PLZ}${DS0&DS1&!DS2&!DS3&SL}	0.1960	0.1962	0.1964
OE_PAD_T$_{PLZ}${DS0&DS1&!DS2&DS3&!SL}	0.1942	0.1944	0.1946
OE_PAD_T$_{PLZ}${DS0&DS1&!DS2&DS3&SL}	0.1935	0.1937	0.1939
OE_PAD_T$_{PLZ}${DS0&DS1&DS2&!DS3&!SL}	0.1888	0.1890	0.1892
OE_PAD_T$_{PLZ}${DS0&DS1&DS2&!DS3&SL}	0.1883	0.1885	0.1887
OE_PAD_T$_{PLZ}${DS0&DS1&DS2&DS3&!SL}	0.1946	0.1948	0.1950
OE_PAD_T$_{PLZ}${DS0&DS1&DS2&DS3&SL}	0.1939	0.1941	0.1943
OE_PAD_T$_{PZH}${!DS0&!DS1&!DS2&!DS3&!SL}	0.3759+0.0714*Cload	0.3975+0.0697*Cload	0.4020+0.0696*Cload
OE_PAD_T$_{PZH}${!DS0&!DS1&!DS2&!DS3&SL}	1.4270+0.0914*Cload	1.6935+0.0725*Cload	1.8030+0.0702*Cload
OE_PAD_T$_{PZH}${!DS0&!DS1&!DS2&DS3&!SL}	0.3011+0.0098*Cload	0.3227+0.0083*Cload	0.3340+0.0081*Cload
OE_PAD_T$_{PZH}${!DS0&!DS1&!DS2&DS3&SL}	1.0210+0.0302*Cload	1.2495+0.0151*Cload	1.4850+0.0105*Cload
OE_PAD_T$_{PZH}${!DS0&!DS1&DS2&!DS3&!SL}	0.3044+0.0157*Cload	0.3213+0.0145*Cload	0.3310+0.0143*Cload
OE_PAD_T$_{PZH}${!DS0&!DS1&DS2&!DS3&SL}	1.0780+0.0380*Cload	1.3430+0.0206*Cload	1.5700+0.0161*Cload
OE_PAD_T$_{PZH}${!DS0&!DS1&DS2&DS3&!SL}	0.3017+0.0075*Cload	0.3235+0.0060*Cload	0.3391+0.0057*Cload
OE_PAD_T$_{PZH}${!DS0&!DS1&DS2&DS3&SL}	1.0030+0.0270*Cload	1.2180+0.0128*Cload	1.4400+0.0085*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&!DS2&!DS3&!SL}	0.3134+0.0249*Cload	0.3308+0.0237*Cload	0.3400+0.0235*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&!DS2&!DS3&SL}	1.1560+0.0484*Cload	1.4490+0.0288*Cload	1.6490+0.0248*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&!DS2&DS3&!SL}	0.3008+0.0084*Cload	0.3207+0.0070*Cload	0.3351+0.0067*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&!DS2&DS3&SL}	1.0100+0.0282*Cload	1.2315+0.0137*Cload	1.4530+0.0094*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&DS2&!DS3&!SL}	0.3009+0.0117*Cload	0.3187+0.0105*Cload	0.3300+0.0103*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&DS2&!DS3&SL}	1.0400+0.0332*Cload	1.2845+0.0171*Cload	1.5180+0.0125*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&DS2&DS3&!SL}	0.3029+0.0068*Cload	0.3253+0.0053*Cload	0.3407+0.0050*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&DS2&DS3&SL}	1.0010+0.0260*Cload	1.2080+0.0122*Cload	1.4220+0.0080*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&!DS2&!DS3&!SL}	0.3283+0.0365*Cload	0.3480+0.0352*Cload	0.3580+0.0350*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&!DS2&!DS3&SL}	1.2390+0.0600*Cload	1.5365+0.0395*Cload	1.7150+0.0359*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&!DS2&DS3&!SL}	0.3011+0.0090*Cload	0.3215+0.0076*Cload	0.3375+0.0073*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&!DS2&DS3&SL}	1.0130+0.0294*Cload	1.2380+0.0144*Cload	1.4680+0.0099*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&DS2&!DS3&!SL}	0.3020+0.0133*Cload	0.3173+0.0122*Cload	0.3320+0.0119*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&DS2&!DS3&SL}	1.0560+0.0352*Cload	1.3095+0.0185*Cload	1.5450+0.0139*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&DS2&DS3&!SL}	0.3024+0.0071*Cload	0.3249+0.0056*Cload	0.3345+0.0054*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&DS2&DS3&SL}	1.0010+0.0266*Cload	1.2115+0.0125*Cload	1.4330+0.0082*Cload
OE_PAD_T$_{PZH}${DS0&DS1&!DS2&!DS3&!SL}	0.3065+0.0191*Cload	0.3221+0.0180*Cload	0.3300+0.0178*Cload
OE_PAD_T$_{PZH}${DS0&DS1&!DS2&!DS3&SL}	1.1080+0.0422*Cload	1.3865+0.0237*Cload	1.6080+0.0193*Cload
OE_PAD_T$_{PZH}${DS0&DS1&!DS2&DS3&!SL}	0.3011+0.0079*Cload	0.3211+0.0065*Cload	0.3350+0.0062*Cload
OE_PAD_T$_{PZH}${DS0&DS1&!DS2&DS3&SL}	1.0070+0.0276*Cload	1.2225+0.0133*Cload	1.4490+0.0089*Cload
OE_PAD_T$_{PZH}${DS0&DS1&DS2&!DS3&!SL}	0.2998+0.0105*Cload	0.3169+0.0093*Cload	0.3257+0.0091*Cload
OE_PAD_T$_{PZH}${DS0&DS1&DS2&!DS3&SL}	1.0300+0.0314*Cload	1.2665+0.0159*Cload	1.4980+0.0114*Cload
OE_PAD_T$_{PZH}${DS0&DS1&DS2&DS3&!SL}	0.3038+0.0065*Cload	0.3268+0.0050*Cload	0.3429+0.0047*Cload
OE_PAD_T$_{PZH}${DS0&DS1&DS2&DS3&SL}	1.0010+0.0256*Cload	1.2100+0.0118*Cload	1.4220+0.0077*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&!DS2&!DS3&!SL}	0.5190+0.1638*Cload	0.5405+0.1623*Cload	0.5600+0.1620*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&!DS2&!DS3&SL}	1.1470+0.1690*Cload	1.2225+0.1631*Cload	1.2410+0.1627*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&!DS2&DS3&!SL}	0.3764+0.0206*Cload	0.4018+0.0187*Cload	0.4110+0.0185*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&!DS2&DS3&SL}	0.8450+0.0324*Cload	1.0055+0.0215*Cload	1.1250+0.0191*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&DS2&!DS3&!SL}	0.3828+0.0345*Cload	0.4005+0.0331*Cload	0.4150+0.0328*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&DS2&!DS3&SL}	0.8860+0.0460*Cload	1.0455+0.0349*Cload	1.1330+0.0331*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&DS2&DS3&!SL}	0.3768+0.0154*Cload	0.4078+0.0132*Cload	0.4180+0.0130*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&DS2&DS3&SL}	0.8391+0.0273*Cload	1.0005+0.0165*Cload	1.1320+0.0139*Cload
OE_PAD_T$_{PZL}${!DS0&DS1&!DS2&!DS3&!SL}	0.3995+0.0560*Cload	0.4190+0.0546*Cload	0.4300+0.0544*Cload
OE_PAD_T$_{PZL}${!DS0&DS1&!DS2&!DS3&SL}	0.9430+0.0660*Cload	1.0885+0.0557*Cload	1.1360+0.0547*Cload
OE_PAD_T$_{PZL}${!DS0&DS1&!DS2&DS3&!SL}	0.3749+0.0175*Cload	0.4021+0.0155*Cload	0.4100+0.0153*Cload
OE_PAD_T$_{PZL}${!DS0&DS1&!DS2&DS3&SL}	0.8391+0.0295*Cload	1.0015+0.0185*Cload	1.1290+0.0160*Cload

Continued...

	Group1	**Group2**	**Group3**
OE_PAD_T$_{PZL}${!DS0&DS1&DS2&!DS3&!SL}	0.3749+0.0254*Cload	0.3984+0.0237*Cload	0.4040+0.0236*Cload
OE_PAD_T$_{PZL}${!DS0&DS1&DS2&!DS3&SL}	0.8600+0.0372*Cload	1.0210+0.0262*Cload	1.1300+0.0240*Cload
OE_PAD_T$_{PZL}${!DS0&DS1&DS2&DS3&!SL}	0.3774+0.0139*Cload	0.4097+0.0116*Cload	0.4240+0.0113*Cload
OE_PAD_T$_{PZL}${!DS0&DS1&DS2&DS3&SL}	0.8399+0.0257*Cload	0.9985+0.0151*Cload	1.1340+0.0124*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&!DS2&!DS3&!SL}	0.4271+0.0832*Cload	0.4480+0.0818*Cload	0.4590+0.0816*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&!DS2&!DS3&SL}	1.0030+0.0918*Cload	1.1270+0.0826*Cload	1.1550+0.0820*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&!DS2&DS3&!SL}	0.3750+0.0189*Cload	0.4027+0.0169*Cload	0.4130+0.0167*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&!DS2&DS3&SL}	0.8419+0.0307*Cload	1.0015+0.0199*Cload	1.1260+0.0174*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&DS2&!DS3&!SL}	0.3778+0.0291*Cload	0.3990+0.0276*Cload	0.4090+0.0274*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&DS2&!DS3&SL}	0.8710+0.0408*Cload	1.0310+0.0298*Cload	1.1280+0.0278*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&DS2&DS3&!SL}	0.3767+0.0146*Cload	0.4095+0.0123*Cload	0.4200+0.0121*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&DS2&DS3&SL}	0.8390+0.0265*Cload	1.0005+0.0157*Cload	1.1320+0.0131*Cload
OE_PAD_T$_{PZL}${DS0&DS1&!DS2&!DS3&!SL}	0.3863+0.0426*Cload	0.4045+0.0413*Cload	0.4150+0.0411*Cload
OE_PAD_T$_{PZL}${DS0&DS1&!DS2&!DS3&SL}	0.9060+0.0538*Cload	1.0620+0.0428*Cload	1.1280+0.0414*Cload
OE_PAD_T$_{PZL}${DS0&DS1&!DS2&DS3&!SL}	0.3744+0.0164*Cload	0.4029+0.0143*Cload	0.4110+0.0141*Cload
OE_PAD_T$_{PZL}${DS0&DS1&!DS2&DS3&SL}	0.8388+0.0282*Cload	0.9985+0.0175*Cload	1.1280+0.0149*Cload
OE_PAD_T$_{PZL}${DS0&DS1&DS2&!DS3&!SL}	0.3730+0.0226*Cload	0.3957+0.0209*Cload	0.4050+0.0207*Cload
OE_PAD_T$_{PZL}${DS0&DS1&DS2&!DS3&SL}	0.8520+0.0346*Cload	1.0145+0.0235*Cload	1.1290+0.0212*Cload
OE_PAD_T$_{PZL}${DS0&DS1&DS2&DS3&!SL}	0.3778+0.0133*Cload	0.4121+0.0109*Cload	0.4210+0.0107*Cload
OE_PAD_T$_{PZL}${DS0&DS1&DS2&DS3&SL}	0.8402+0.0252*Cload	0.9995+0.0145*Cload	1.1350+0.0118*Cload
Timing Arc	**(< 0.03)pf**	**(0.03-0.3)pf**	**(> 0.3)pf**
PAD_C_T$_{PHL}${!ST}	0.2721+0.3150*Cload	0.2721+0.3100*Cload	0.2717+0.3110*Cload
PAD_C_T$_{PHL}${ST}	0.5384+0.3150*Cload	0.5388+0.3060*Cload	0.5377+0.3125*Cload
PAD_C_T$_{PLH}${!ST}	0.3357+0.2850*Cload	0.3360+0.2760*Cload	0.3353+0.2790*Cload
PAD_C_T$_{PLH}${ST}	0.5859+0.2800*Cload	0.5861+0.2760*Cload	0.5854+0.2790*Cload

9.26 PRWDWUWSWEWCODCDGSH_V

Core overdrive 1.2V, Regular I/O with POC. (When in POC mode, output = Z, pull resistors = disabled.)



Truth Table

INPUT																							OUTPUT	
VDD	VDDPST12	VDDPST08	VDDPST04	ESDB	ESD12	ESD12B	POCCTRL	POCCTRLD	POCCTRL12	RTE	DS3	DS2	DS1	DS0	SL	OE	I	PD	PU	SPU	PAD	ST	IE	PAD	C
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	1	0	0/1	0/1	0/1	-	0/1	0/1	0	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	1	1	0/1	0/1	0/1	-	0/1	1	1	1
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	1	1	0/1	0/1	0/1	-	0/1	0	1	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	0/1	0/1	0/1	0	0/1	0/1	-	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	0/1	0/1	0/1	1	0/1	0	-	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	0/1	0/1	0/1	1	0/1	1	-	1
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	0	0	0	Z	0/1	0	-	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	0	0	0	Z	0/1	1	-	X
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	1	0	0	Z	0/1	0	L	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	1	0	0	Z	0/1	1	L	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	0	1	0	Z	0/1	0	H	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	0	1	0	Z	0/1	1	H	1
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	1	1	0	Z	0/1	0	previous-state	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	1	1	0	Z	0/1	1	previous-state	previous-state
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	0/1	0/1	1	Z	0/1	0	Strong-H	0
1	1	1	1	1	0	1	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0	0/1	0/1	0/1	1	Z	0/1	1	Strong-H	1
1	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	-	0/1	0/1	X	0
0	1	1	1	1	0	1	1	1	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	Z	X
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch1	Latch0	Latch	Latch	Latch	-	Latch	Latch	0	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch1	Latch1	Latch	Latch	Latch	-	Latch	Latch1	1	1
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch1	Latch1	Latch	Latch	Latch	-	Latch	Latch0	1	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	Latch	0	Latch	Latch	-	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	Latch	1	Latch	Latch0	-	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	Latch	1	Latch	Latch1	-	1
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch0	Latch0	Z	Latch	Latch0	-	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch0	Latch0	Z	Latch	Latch1	-	X
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch0	Latch0	Z	Latch	Latch0	L	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch0	Latch0	Z	Latch	Latch1	L	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch1	Latch0	Z	Latch	Latch0	H	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch1	Latch0	Z	Latch	Latch1	H	1
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch1	Latch0	Z	Latch	Latch0	previous-state	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch1	Latch0	Z	Latch	Latch1	previous-state	previous-state
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	Latch1	Z	Latch	Latch0	Strong-H	0
1	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	Latch1	Z	Latch	Latch1	Strong-H	1
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch1	Latch0	Latch	Latch	Latch	-	Latch	Latch	0	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch1	Latch1	Latch	Latch	Latch	-	Latch	Latch1	1	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch1	Latch1	Latch	Latch	Latch	-	Latch	Latch0	1	X

Continued...

VDD	VDDPST12	VDDPST08	VDDPST04	ESDB	ESD12	ESD12B	POCCTRL	POCCTRLD	POCCTRL12	RTE	DS3	DS2	DS1	DS0	SL	OE	I	PD	PU	SPU	PAD	ST	IE	PAD	C
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	Latch	0	Latch	Latch	-	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	Latch	1	Latch	Latch0	-	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	Latch	1	Latch	Latch1	-	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch0	Latch0	Z	Latch	Latch0	-	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch0	Latch0	Z	Latch	Latch1	-	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch0	Latch0	Z	Latch	Latch0	L	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch0	Latch0	Z	Latch	Latch1	L	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch1	Latch0	Z	Latch	Latch0	H	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch0	Latch1	Latch0	Z	Latch	Latch1	H	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch1	Latch0	Z	Latch	Latch0	previous-state	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch1	Latch1	Latch0	Z	Latch	Latch1	previous-state	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	Latch1	Z	Latch	Latch0	Strong-H	X
0	1	1	1	1	0	1	0	0	0	1	Latch	Latch	Latch	Latch	Latch	Latch0	Latch	Latch	Latch	Latch1	Z	Latch	Latch1	Strong-H	X
1	0	1	1	1	0	0	1	1	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	-	0/1	0/1	X	0
0	0	1	1	1	0	0	1	1	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X
1	0	1	0	1	0	0	1	1	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	-	0/1	0/1	X	0
0	0	1	0	1	0	0	1	1	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X
1	0	0	1	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	-	0/1	0/1	X	0
0	0	0	1	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X
0	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X

*All undefined states in truth table are illegal operation

Cell Information

	Value	Unit
Cell Width	17.76	um
Cell Height	55.77	um
Pad Number	1	-

Leakage Power

	Value	Unit
VDDPST12	2.134e+04	nW

Pin Capacitance

	Value	Unit
DS0	0.003212	pF
DS1	0.003093	pF
DS2	0.002619	pF
DS3	0.002482	pF
ESD12	0.009459	pF
ESD12B	0.01226	pF
ESDB	0.01024	pF
I	0.002965	pF
IE	0.002327	pF
OE	0.002753	pF
PAD	1.272	pF
PD	0.002637	pF
POCCTRL	0.006919	pF
POCCTRL12	0.008767	pF
POCCTRLD	0.00696	pF
PU	0.00272	pF
RTE	0.008115	pF
SL	0.002273	pF
SPU	0.002365	pF
ST	0.00254	pF

Propagation Delay

	Group1	Group2	Group3
Timing Arc	**(< 0.03)pf**	**(0.03-0.3)pf**	**(> 0.3)pf**
IE_C_T$_{PHL}${!ST}	0.1091+0.4800*Cload	0.1092+0.4760*Cload	0.1089+0.4785*Cload
IE_C_T$_{PHL}${ST}	0.1091+0.4800*Cload	0.1092+0.4760*Cload	0.1087+0.4790*Cload
IE_C_T$_{PLH}${!ST}	0.3025+0.4550*Cload	0.3025+0.4540*Cload	0.3034+0.4535*Cload
IE_C_T$_{PLH}${ST}	0.3317+0.4550*Cload	0.3317+0.4540*Cload	0.3329+0.4525*Cload
Timing Arc	**(< 10)pf**	**(10-70)pf**	**(> 70)pf**

Continued...

	Group1	Group2	Group3
I_PAD_T$_{PHL}${!DS0&!DS1&!DS2&!DS3&!SL}	0.6480+0.1654*Cload	0.6700+0.1638*Cload	0.6710+0.1637*Cload
I_PAD_T$_{PHL}${!DS0&!DS1&!DS2&!DS3&SL}	1.2490+0.1696*Cload	1.3155+0.1645*Cload	1.3400+0.1640*Cload
I_PAD_T$_{PHL}${!DS0&!DS1&!DS2&DS3&!SL}	0.3822+0.0207*Cload	0.4127+0.0185*Cload	0.4270+0.0182*Cload
I_PAD_T$_{PHL}${!DS0&!DS1&!DS2&DS3&SL}	0.8179+0.0313*Cload	0.9695+0.0211*Cload	1.0850+0.0188*Cload
I_PAD_T$_{PHL}${!DS0&!DS1&DS2&!DS3&!SL}	0.4118+0.0353*Cload	0.4365+0.0335*Cload	0.4460+0.0333*Cload
I_PAD_T$_{PHL}${!DS0&!DS1&DS2&!DS3&SL}	0.8900+0.0452*Cload	1.0370+0.0352*Cload	1.1210+0.0335*Cload
I_PAD_T$_{PHL}${!DS0&!DS1&DS2&DS3&!SL}	0.3789+0.0157*Cload	0.4164+0.0131*Cload	0.4330+0.0128*Cload
I_PAD_T$_{PHL}${!DS0&!DS1&DS2&DS3&SL}	0.8042+0.0262*Cload	0.9550+0.0162*Cload	1.0830+0.0137*Cload
I_PAD_T$_{PHL}${!DS0&DS1&!DS2&!DS3&!SL}	0.4491+0.0568*Cload	0.4695+0.0553*Cload	0.4850+0.0550*Cload
I_PAD_T$_{PHL}${!DS0&DS1&!DS2&!DS3&SL}	0.9600+0.0656*Cload	1.0915+0.0563*Cload	1.1390+0.0553*Cload
I_PAD_T$_{PHL}${!DS0&DS1&!DS2&DS3&!SL}	0.3776+0.0177*Cload	0.4111+0.0153*Cload	0.4250+0.0150*Cload
I_PAD_T$_{PHL}${!DS0&DS1&!DS2&DS3&SL}	0.8008+0.0282*Cload	0.9535+0.0181*Cload	1.0700+0.0158*Cload
I_PAD_T$_{PHL}${!DS0&DS1&DS2&!DS3&!SL}	0.3953+0.0264*Cload	0.4220+0.0244*Cload	0.4300+0.0242*Cload
I_PAD_T$_{PHL}${!DS0&DS1&DS2&!DS3&SL}	0.8490+0.0366*Cload	0.9970+0.0266*Cload	1.0950+0.0246*Cload
I_PAD_T$_{PHL}${!DS0&DS1&DS2&DS3&!SL}	0.3775+0.0142*Cload	0.4151+0.0116*Cload	0.4350+0.0112*Cload
I_PAD_T$_{PHL}${!DS0&DS1&DS2&DS3&SL}	0.7940+0.0247*Cload	0.9405+0.0149*Cload	1.0690+0.0123*Cload
I_PAD_T$_{PHL}${DS0&!DS1&!DS2&!DS3&!SL}	0.4990+0.0839*Cload	0.5195+0.0825*Cload	0.5300+0.0823*Cload
I_PAD_T$_{PHL}${DS0&!DS1&!DS2&!DS3&SL}	1.0490+0.0914*Cload	1.1610+0.0832*Cload	1.1910+0.0826*Cload
I_PAD_T$_{PHL}${DS0&!DS1&!DS2&DS3&!SL}	0.3801+0.0191*Cload	0.4116+0.0168*Cload	0.4250+0.0165*Cload
I_PAD_T$_{PHL}${DS0&!DS1&!DS2&DS3&SL}	0.8131+0.0296*Cload	0.9645+0.0195*Cload	1.0870+0.0171*Cload
I_PAD_T$_{PHL}${DS0&!DS1&DS2&!DS3&!SL}	0.4021+0.0300*Cload	0.4300+0.0280*Cload	0.4420+0.0278*Cload
I_PAD_T$_{PHL}${DS0&!DS1&DS2&!DS3&SL}	0.8700+0.0402*Cload	1.0175+0.0301*Cload	1.1090+0.0282*Cload
I_PAD_T$_{PHL}${DS0&!DS1&DS2&DS3&!SL}	0.3788+0.0149*Cload	0.4161+0.0123*Cload	0.4300+0.0120*Cload
I_PAD_T$_{PHL}${DS0&!DS1&DS2&DS3&SL}	0.8029+0.0254*Cload	0.9515+0.0155*Cload	1.0830+0.0129*Cload
I_PAD_T$_{PHL}${DS0&DS1&!DS2&!DS3&!SL}	0.4241+0.0433*Cload	0.4455+0.0417*Cload	0.4620+0.0414*Cload
I_PAD_T$_{PHL}${DS0&DS1&!DS2&!DS3&SL}	0.9150+0.0528*Cload	1.0545+0.0431*Cload	1.1210+0.0417*Cload
I_PAD_T$_{PHL}${DS0&DS1&!DS2&DS3&!SL}	0.3767+0.0166*Cload	0.4123+0.0141*Cload	0.4280+0.0138*Cload
I_PAD_T$_{PHL}${DS0&DS1&!DS2&DS3&SL}	0.7980+0.0271*Cload	0.9485+0.0171*Cload	1.0760+0.0146*Cload
I_PAD_T$_{PHL}${DS0&DS1&DS2&!DS3&!SL}	0.3908+0.0235*Cload	0.4199+0.0214*Cload	0.4290+0.0212*Cload
I_PAD_T$_{PHL}${DS0&DS1&DS2&!DS3&SL}	0.8380+0.0338*Cload	0.9880+0.0238*Cload	1.0920+0.0217*Cload
I_PAD_T$_{PHL}${DS0&DS1&DS2&DS3&!SL}	0.3777+0.0136*Cload	0.4176+0.0109*Cload	0.4320+0.0106*Cload
I_PAD_T$_{PHL}${DS0&DS1&DS2&DS3&SL}	0.7939+0.0240*Cload	0.9405+0.0143*Cload	1.0770+0.0116*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&!DS2&!DS3&!SL}	0.3920+0.0707*Cload	0.4185+0.0687*Cload	0.4240+0.0686*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&!DS2&!DS3&SL}	1.3500+0.0884*Cload	1.5900+0.0712*Cload	1.6840+0.0692*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&!DS2&DS3&!SL}	0.3104+0.0098*Cload	0.3316+0.0083*Cload	0.3455+0.0080*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&!DS2&DS3&SL}	0.9680+0.0284*Cload	1.1825+0.0143*Cload	1.3940+0.0102*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&DS2&!DS3&!SL}	0.3130+0.0156*Cload	0.3316+0.0143*Cload	0.3410+0.0141*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&DS2&!DS3&SL}	1.0170+0.0358*Cload	1.2585+0.0199*Cload	1.4670+0.0157*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&DS2&DS3&!SL}	0.3093+0.0076*Cload	0.3345+0.0059*Cload	0.3511+0.0056*Cload
I_PAD_T$_{PLH}${!DS0&!DS1&DS2&DS3&SL}	0.9520+0.0252*Cload	1.1480+0.0122*Cload	1.3530+0.0082*Cload
I_PAD_T$_{PLH}${!DS0&DS1&!DS2&!DS3&!SL}	0.3254+0.0247*Cload	0.3446+0.0234*Cload	0.3600+0.0231*Cload
I_PAD_T$_{PLH}${!DS0&DS1&!DS2&!DS3&SL}	1.0910+0.0460*Cload	1.3580+0.0280*Cload	1.5410+0.0243*Cload
I_PAD_T$_{PLH}${!DS0&DS1&!DS2&DS3&!SL}	0.3097+0.0085*Cload	0.3330+0.0069*Cload	0.3477+0.0066*Cload
I_PAD_T$_{PLH}${!DS0&DS1&!DS2&DS3&SL}	0.9580+0.0266*Cload	1.1615+0.0131*Cload	1.3720+0.0090*Cload
I_PAD_T$_{PLH}${!DS0&DS1&DS2&!DS3&!SL}	0.3084+0.0118*Cload	0.3282+0.0104*Cload	0.3450+0.0101*Cload
I_PAD_T$_{PLH}${!DS0&DS1&DS2&!DS3&SL}	0.9810+0.0312*Cload	1.2075+0.0163*Cload	1.4220+0.0121*Cload
I_PAD_T$_{PLH}${!DS0&DS1&DS2&DS3&!SL}	0.3107+0.0069*Cload	0.3344+0.0053*Cload	0.3539+0.0049*Cload
I_PAD_T$_{PLH}${!DS0&DS1&DS2&DS3&SL}	0.9490+0.0244*Cload	1.1425+0.0115*Cload	1.3420+0.0076*Cload
I_PAD_T$_{PLH}${DS0&!DS1&!DS2&!DS3&!SL}	0.3411+0.0361*Cload	0.3640+0.0346*Cload	0.3740+0.0344*Cload
I_PAD_T$_{PLH}${DS0&!DS1&!DS2&!DS3&SL}	1.1720+0.0570*Cload	1.4420+0.0384*Cload	1.6000+0.0352*Cload
I_PAD_T$_{PLH}${DS0&!DS1&!DS2&DS3&!SL}	0.3098+0.0091*Cload	0.3327+0.0075*Cload	0.3479+0.0072*Cload
I_PAD_T$_{PLH}${DS0&!DS1&!DS2&DS3&SL}	0.9640+0.0272*Cload	1.1695+0.0137*Cload	1.3840+0.0095*Cload
I_PAD_T$_{PLH}${DS0&!DS1&DS2&!DS3&!SL}	0.3105+0.0133*Cload	0.3294+0.0120*Cload	0.3390+0.0118*Cload
I_PAD_T$_{PLH}${DS0&!DS1&DS2&!DS3&SL}	0.9980+0.0330*Cload	1.2300+0.0178*Cload	1.4480+0.0135*Cload
I_PAD_T$_{PLH}${DS0&!DS1&DS2&DS3&!SL}	0.3103+0.0072*Cload	0.3338+0.0056*Cload	0.3469+0.0053*Cload
I_PAD_T$_{PLH}${DS0&!DS1&DS2&DS3&SL}	0.9510+0.0248*Cload	1.1460+0.0118*Cload	1.3530+0.0078*Cload
I_PAD_T$_{PLH}${DS0&DS1&!DS2&!DS3&!SL}	0.3172+0.0191*Cload	0.3352+0.0178*Cload	0.3490+0.0175*Cload
I_PAD_T$_{PLH}${DS0&DS1&!DS2&!DS3&SL}	1.0470+0.0398*Cload	1.3025+0.0229*Cload	1.5020+0.0189*Cload

Continued...

	Group1	Group2	Group3
I_PAD_T$_{PLH}${DS0&DS1&!DS2&DS3&!SL}	0.3100+0.0080*Cload	0.3335+0.0064*Cload	0.3474+0.0061*Cload
I_PAD_T$_{PLH}${DS0&DS1&!DS2&DS3&SL}	0.9560+0.0258*Cload	1.1560+0.0126*Cload	1.3670+0.0085*Cload
I_PAD_T$_{PLH}${DS0&DS1&DS2&!DS3&!SL}	0.3078+0.0106*Cload	0.3277+0.0092*Cload	0.3363+0.0090*Cload
I_PAD_T$_{PLH}${DS0&DS1&DS2&!DS3&SL}	0.9730+0.0294*Cload	1.1875+0.0153*Cload	1.4060+0.0110*Cload
I_PAD_T$_{PLH}${DS0&DS1&DS2&DS3&!SL}	0.3112+0.0067*Cload	0.3362+0.0050*Cload	0.3496+0.0047*Cload
I_PAD_T$_{PLH}${DS0&DS1&DS2&DS3&SL}	0.9510+0.0238*Cload	1.1420+0.0112*Cload	1.3430+0.0073*Cload
Timing Arc	**(< 10)pf**	**(10-70)pf**	**(> 70)pf**
OE_PAD_T$_{PHZ}${!DS0&!DS1&!DS2&!DS3&!SL}	0.1769	0.1771	0.1773
OE_PAD_T$_{PHZ}${!DS0&!DS1&!DS2&!DS3&SL}	0.1769	0.1771	0.1773
OE_PAD_T$_{PHZ}${!DS0&!DS1&!DS2&DS3&!SL}	0.1809	0.1811	0.1813
OE_PAD_T$_{PHZ}${!DS0&!DS1&!DS2&DS3&SL}	0.1808	0.1810	0.1812
OE_PAD_T$_{PHZ}${!DS0&!DS1&DS2&!DS3&!SL}	0.1755	0.1757	0.1759
OE_PAD_T$_{PHZ}${!DS0&!DS1&DS2&!DS3&SL}	0.1754	0.1756	0.1758
OE_PAD_T$_{PHZ}${!DS0&!DS1&DS2&DS3&!SL}	0.1826	0.1828	0.1830
OE_PAD_T$_{PHZ}${!DS0&!DS1&DS2&DS3&SL}	0.1826	0.1828	0.1830
OE_PAD_T$_{PHZ}${!DS0&DS1&!DS2&!DS3&!SL}	0.1777	0.1779	0.1781
OE_PAD_T$_{PHZ}${!DS0&DS1&!DS2&!DS3&SL}	0.1777	0.1779	0.1781
OE_PAD_T$_{PHZ}${!DS0&DS1&!DS2&DS3&!SL}	0.1820	0.1822	0.1824
OE_PAD_T$_{PHZ}${!DS0&DS1&!DS2&DS3&SL}	0.1820	0.1822	0.1824
OE_PAD_T$_{PHZ}${!DS0&DS1&DS2&!DS3&!SL}	0.1769	0.1771	0.1773
OE_PAD_T$_{PHZ}${!DS0&DS1&DS2&!DS3&SL}	0.1769	0.1771	0.1773
OE_PAD_T$_{PHZ}${!DS0&DS1&DS2&DS3&!SL}	0.1839	0.1841	0.1843
OE_PAD_T$_{PHZ}${!DS0&DS1&DS2&DS3&SL}	0.1839	0.1841	0.1843
OE_PAD_T$_{PHZ}${DS0&!DS1&!DS2&!DS3&!SL}	0.1793	0.1795	0.1797
OE_PAD_T$_{PHZ}${DS0&!DS1&!DS2&!DS3&SL}	0.1793	0.1795	0.1797
OE_PAD_T$_{PHZ}${DS0&!DS1&!DS2&DS3&!SL}	0.1817	0.1819	0.1821
OE_PAD_T$_{PHZ}${DS0&!DS1&!DS2&DS3&SL}	0.1817	0.1819	0.1821
OE_PAD_T$_{PHZ}${DS0&!DS1&DS2&!DS3&!SL}	0.1764	0.1766	0.1768
OE_PAD_T$_{PHZ}${DS0&!DS1&DS2&!DS3&SL}	0.1764	0.1766	0.1768
OE_PAD_T$_{PHZ}${DS0&!DS1&DS2&DS3&!SL}	0.1835	0.1837	0.1839
OE_PAD_T$_{PHZ}${DS0&!DS1&DS2&DS3&SL}	0.1835	0.1837	0.1839
OE_PAD_T$_{PHZ}${DS0&DS1&!DS2&!DS3&!SL}	0.1790	0.1792	0.1794
OE_PAD_T$_{PHZ}${DS0&DS1&!DS2&!DS3&SL}	0.1790	0.1792	0.1794
OE_PAD_T$_{PHZ}${DS0&DS1&!DS2&DS3&!SL}	0.1829	0.1831	0.1833
OE_PAD_T$_{PHZ}${DS0&DS1&!DS2&DS3&SL}	0.1829	0.1831	0.1833
OE_PAD_T$_{PHZ}${DS0&DS1&DS2&!DS3&!SL}	0.1780	0.1782	0.1784
OE_PAD_T$_{PHZ}${DS0&DS1&DS2&!DS3&SL}	0.1780	0.1782	0.1784
OE_PAD_T$_{PHZ}${DS0&DS1&DS2&DS3&!SL}	0.1849	0.1851	0.1853
OE_PAD_T$_{PHZ}${DS0&DS1&DS2&DS3&SL}	0.1849	0.1851	0.1853
OE_PAD_T$_{PLZ}${!DS0&!DS1&!DS2&!DS3&!SL}	0.2021	0.2023	0.2025
OE_PAD_T$_{PLZ}${!DS0&!DS1&!DS2&!DS3&SL}	0.2003	0.2005	0.2007
OE_PAD_T$_{PLZ}${!DS0&!DS1&!DS2&DS3&!SL}	0.1967	0.1969	0.1971
OE_PAD_T$_{PLZ}${!DS0&!DS1&!DS2&DS3&SL}	0.1955	0.1957	0.1959
OE_PAD_T$_{PLZ}${!DS0&!DS1&DS2&!DS3&!SL}	0.1890	0.1892	0.1894
OE_PAD_T$_{PLZ}${!DS0&!DS1&DS2&!DS3&SL}	0.1883	0.1885	0.1887
OE_PAD_T$_{PLZ}${!DS0&!DS1&DS2&DS3&!SL}	0.1972	0.1974	0.1976
OE_PAD_T$_{PLZ}${!DS0&!DS1&DS2&DS3&SL}	0.1961	0.1963	0.1965
OE_PAD_T$_{PLZ}${!DS0&DS1&!DS2&!DS3&!SL}	0.2045	0.2047	0.2049
OE_PAD_T$_{PLZ}${!DS0&DS1&!DS2&!DS3&SL}	0.2032	0.2034	0.2036
OE_PAD_T$_{PLZ}${!DS0&DS1&!DS2&DS3&!SL}	0.1967	0.1969	0.1971
OE_PAD_T$_{PLZ}${!DS0&DS1&!DS2&DS3&SL}	0.1956	0.1958	0.1960
OE_PAD_T$_{PLZ}${!DS0&DS1&DS2&!DS3&!SL}	0.1901	0.1903	0.1905
OE_PAD_T$_{PLZ}${!DS0&DS1&DS2&!DS3&SL}	0.1893	0.1895	0.1897
OE_PAD_T$_{PLZ}${!DS0&DS1&DS2&DS3&!SL}	0.1972	0.1974	0.1976
OE_PAD_T$_{PLZ}${!DS0&DS1&DS2&DS3&SL}	0.1961	0.1963	0.1965
OE_PAD_T$_{PLZ}${DS0&!DS1&!DS2&!DS3&!SL}	0.2056	0.2058	0.2060
OE_PAD_T$_{PLZ}${DS0&!DS1&!DS2&!DS3&SL}	0.2047	0.2049	0.2051

Continued...

	Group1	Group2	Group3
OE_PAD_T$_{PLZ}${DS0&!DS1&!DS2&DS3&!SL}	0.1971	0.1973	0.1975
OE_PAD_T$_{PLZ}${DS0&!DS1&!DS2&DS3&SL}	0.1961	0.1963	0.1965
OE_PAD_T$_{PLZ}${DS0&!DS1&DS2&!DS3&!SL}	0.1890	0.1892	0.1894
OE_PAD_T$_{PLZ}${DS0&!DS1&DS2&!DS3&SL}	0.1882	0.1884	0.1886
OE_PAD_T$_{PLZ}${DS0&!DS1&DS2&DS3&!SL}	0.1977	0.1979	0.1981
OE_PAD_T$_{PLZ}${DS0&!DS1&DS2&DS3&SL}	0.1964	0.1966	0.1968
OE_PAD_T$_{PLZ}${DS0&DS1&!DS2&!DS3&!SL}	0.2031	0.2033	0.2035
OE_PAD_T$_{PLZ}${DS0&DS1&!DS2&!DS3&SL}	0.2016	0.2018	0.2020
OE_PAD_T$_{PLZ}${DS0&DS1&!DS2&DS3&!SL}	0.1972	0.1974	0.1976
OE_PAD_T$_{PLZ}${DS0&DS1&!DS2&DS3&SL}	0.1960	0.1962	0.1964
OE_PAD_T$_{PLZ}${DS0&DS1&DS2&!DS3&!SL}	0.1901	0.1903	0.1905
OE_PAD_T$_{PLZ}${DS0&DS1&DS2&!DS3&SL}	0.1893	0.1895	0.1897
OE_PAD_T$_{PLZ}${DS0&DS1&DS2&DS3&!SL}	0.1977	0.1979	0.1981
OE_PAD_T$_{PLZ}${DS0&DS1&DS2&DS3&SL}	0.1965	0.1967	0.1969
OE_PAD_T$_{PZH}${!DS0&!DS1&!DS2&!DS3&!SL}	0.3780+0.0706*Cload	0.4020+0.0688*Cload	0.4050+0.0687*Cload
OE_PAD_T$_{PZH}${!DS0&!DS1&!DS2&!DS3&SL}	1.3220+0.0886*Cload	1.5625+0.0713*Cload	1.6540+0.0693*Cload
OE_PAD_T$_{PZH}${!DS0&!DS1&!DS2&DS3&!SL}	0.3030+0.0099*Cload	0.3255+0.0083*Cload	0.3393+0.0080*Cload
OE_PAD_T$_{PZH}${!DS0&!DS1&!DS2&DS3&SL}	0.9480+0.0286*Cload	1.1620+0.0144*Cload	1.3770+0.0102*Cload
OE_PAD_T$_{PZH}${!DS0&!DS1&DS2&!DS3&!SL}	0.3052+0.0157*Cload	0.3247+0.0143*Cload	0.3340+0.0141*Cload
OE_PAD_T$_{PZH}${!DS0&!DS1&DS2&!DS3&SL}	0.9950+0.0362*Cload	1.2415+0.0199*Cload	1.4500+0.0157*Cload
OE_PAD_T$_{PZH}${!DS0&!DS1&DS2&DS3&!SL}	0.3028+0.0076*Cload	0.3286+0.0059*Cload	0.3452+0.0056*Cload
OE_PAD_T$_{PZH}${!DS0&!DS1&DS2&DS3&SL}	0.9330+0.0254*Cload	1.1345+0.0121*Cload	1.3370+0.0082*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&!DS2&!DS3&!SL}	0.3165+0.0248*Cload	0.3365+0.0234*Cload	0.3520+0.0231*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&!DS2&!DS3&SL}	1.0680+0.0462*Cload	1.3415+0.0279*Cload	1.5220+0.0243*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&!DS2&DS3&!SL}	0.3025+0.0086*Cload	0.3270+0.0069*Cload	0.3417+0.0066*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&!DS2&DS3&SL}	0.9390+0.0266*Cload	1.1435+0.0131*Cload	1.3540+0.0090*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&DS2&!DS3&!SL}	0.3015+0.0118*Cload	0.3219+0.0104*Cload	0.3310+0.0102*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&DS2&!DS3&SL}	0.9610+0.0314*Cload	1.1880+0.0164*Cload	1.4060+0.0121*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&DS2&DS3&!SL}	0.3036+0.0070*Cload	0.3285+0.0053*Cload	0.3480+0.0049*Cload
OE_PAD_T$_{PZH}${!DS0&DS1&DS2&DS3&SL}	0.9310+0.0244*Cload	1.1255+0.0115*Cload	1.3260+0.0076*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&!DS2&!DS3&!SL}	0.3314+0.0361*Cload	0.3540+0.0346*Cload	0.3640+0.0344*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&!DS2&!DS3&SL}	1.1460+0.0574*Cload	1.4220+0.0384*Cload	1.5800+0.0352*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&!DS2&DS3&!SL}	0.3025+0.0092*Cload	0.3266+0.0075*Cload	0.3418+0.0072*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&!DS2&DS3&SL}	0.9430+0.0276*Cload	1.1515+0.0137*Cload	1.3680+0.0095*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&DS2&!DS3&!SL}	0.3029+0.0134*Cload	0.3229+0.0120*Cload	0.3330+0.0118*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&DS2&!DS3&SL}	0.9760+0.0334*Cload	1.2130+0.0178*Cload	1.4320+0.0135*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&DS2&DS3&!SL}	0.3031+0.0073*Cload	0.3278+0.0056*Cload	0.3410+0.0053*Cload
OE_PAD_T$_{PZH}${DS0&!DS1&DS2&DS3&SL}	0.9330+0.0248*Cload	1.1300+0.0118*Cload	1.3300+0.0079*Cload
OE_PAD_T$_{PZH}${DS0&DS1&!DS2&!DS3&!SL}	0.3095+0.0191*Cload	0.3303+0.0177*Cload	0.3420+0.0175*Cload
OE_PAD_T$_{PZH}${DS0&DS1&!DS2&!DS3&SL}	1.0240+0.0402*Cload	1.2845+0.0229*Cload	1.4840+0.0189*Cload
OE_PAD_T$_{PZH}${DS0&DS1&!DS2&DS3&!SL}	0.3028+0.0081*Cload	0.3275+0.0064*Cload	0.3415+0.0061*Cload
OE_PAD_T$_{PZH}${DS0&DS1&!DS2&DS3&SL}	0.9360+0.0260*Cload	1.1380+0.0126*Cload	1.3430+0.0086*Cload
OE_PAD_T$_{PZH}${DS0&DS1&DS2&!DS3&!SL}	0.3004+0.0107*Cload	0.3215+0.0092*Cload	0.3370+0.0089*Cload
OE_PAD_T$_{PZH}${DS0&DS1&DS2&!DS3&SL}	0.9510+0.0298*Cload	1.1705+0.0153*Cload	1.3900+0.0110*Cload
OE_PAD_T$_{PZH}${DS0&DS1&DS2&DS3&!SL}	0.3047+0.0067*Cload	0.3302+0.0050*Cload	0.3437+0.0047*Cload
OE_PAD_T$_{PZH}${DS0&DS1&DS2&DS3&SL}	0.9300+0.0242*Cload	1.1250+0.0112*Cload	1.3200+0.0074*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&!DS2&!DS3&!SL}	0.5270+0.1656*Cload	0.5530+0.1638*Cload	0.5610+0.1637*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&!DS2&!DS3&SL}	1.1170+0.1708*Cload	1.1975+0.1645*Cload	1.2300+0.1640*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&!DS2&DS3&!SL}	0.3734+0.0207*Cload	0.4033+0.0185*Cload	0.4180+0.0182*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&!DS2&DS3&SL}	0.7949+0.0321*Cload	0.9560+0.0212*Cload	1.0760+0.0188*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&DS2&!DS3&!SL}	0.3901+0.0353*Cload	0.4145+0.0335*Cload	0.4240+0.0333*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&DS2&!DS3&SL}	0.8510+0.0464*Cload	1.0115+0.0353*Cload	1.0930+0.0336*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&DS2&DS3&!SL}	0.3734+0.0157*Cload	0.4108+0.0131*Cload	0.4270+0.0128*Cload
OE_PAD_T$_{PZL}${!DS0&!DS1&DS2&DS3&SL}	0.7848+0.0270*Cload	0.9445+0.0163*Cload	1.0770+0.0137*Cload
OE_PAD_T$_{PZL}${!DS0&DS1&!DS2&!DS3&!SL}	0.4088+0.0569*Cload	0.4305+0.0553*Cload	0.4470+0.0550*Cload
OE_PAD_T$_{PZL}${!DS0&DS1&!DS2&!DS3&SL}	0.9020+0.0670*Cload	1.0525+0.0563*Cload	1.1010+0.0553*Cload
OE_PAD_T$_{PZL}${!DS0&DS1&!DS2&DS3&!SL}	0.3707+0.0177*Cload	0.4039+0.0153*Cload	0.4180+0.0150*Cload
OE_PAD_T$_{PZL}${!DS0&DS1&!DS2&DS3&SL}	0.7791+0.0291*Cload	0.9385+0.0183*Cload	1.0630+0.0158*Cload

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	Group1	**Group2**	**Group3**
OE_PAD_T$_{PZL}${!DS0&DS1&DS2&!DS3&!SL}	0.3800+0.0264*Cload	0.4070+0.0244*Cload	0.4150+0.0242*Cload
OE_PAD_T$_{PZL}${!DS0&DS1&DS2&!DS3&SL}	0.8160+0.0378*Cload	0.9775+0.0267*Cload	1.0810+0.0246*Cload
OE_PAD_T$_{PZL}${!DS0&DS1&DS2&DS3&!SL}	0.3729+0.0142*Cload	0.4105+0.0116*Cload	0.4300+0.0112*Cload
OE_PAD_T$_{PZL}${!DS0&DS1&DS2&DS3&SL}	0.7750+0.0256*Cload	0.9335+0.0149*Cload	1.0720+0.0122*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&!DS2&!DS3&!SL}	0.4378+0.0841*Cload	0.4615+0.0825*Cload	0.4730+0.0823*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&!DS2&!DS3&SL}	0.9720+0.0928*Cload	1.0995+0.0833*Cload	1.1330+0.0826*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&!DS2&DS3&!SL}	0.3729+0.0190*Cload	0.4034+0.0168*Cload	0.4160+0.0165*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&!DS2&DS3&SL}	0.7911+0.0304*Cload	0.9520+0.0196*Cload	1.0790+0.0171*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&DS2&!DS3&!SL}	0.3842+0.0300*Cload	0.4095+0.0281*Cload	0.4240+0.0278*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&DS2&!DS3&SL}	0.8340+0.0414*Cload	0.9950+0.0302*Cload	1.0920+0.0282*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&DS2&DS3&!SL}	0.3737+0.0149*Cload	0.4110+0.0123*Cload	0.4250+0.0120*Cload
OE_PAD_T$_{PZL}${DS0&!DS1&DS2&DS3&SL}	0.7841+0.0262*Cload	0.9410+0.0156*Cload	1.0780+0.0129*Cload
OE_PAD_T$_{PZL}${DS0&DS1&!DS2&!DS3&!SL}	0.3940+0.0434*Cload	0.4175+0.0417*Cload	0.4270+0.0415*Cload
OE_PAD_T$_{PZL}${DS0&DS1&!DS2&!DS3&SL}	0.8660+0.0542*Cload	1.0255+0.0431*Cload	1.0930+0.0417*Cload
OE_PAD_T$_{PZL}${DS0&DS1&!DS2&DS3&!SL}	0.3706+0.0166*Cload	0.4058+0.0141*Cload	0.4210+0.0138*Cload
OE_PAD_T$_{PZL}${DS0&DS1&!DS2&DS3&SL}	0.7771+0.0280*Cload	0.9370+0.0172*Cload	1.0620+0.0147*Cload
OE_PAD_T$_{PZL}${DS0&DS1&DS2&!DS3&!SL}	0.3776+0.0235*Cload	0.4072+0.0214*Cload	0.4170+0.0212*Cload
OE_PAD_T$_{PZL}${DS0&DS1&DS2&!DS3&SL}	0.8072+0.0350*Cload	0.9705+0.0239*Cload	1.0800+0.0217*Cload
OE_PAD_T$_{PZL}${DS0&DS1&DS2&DS3&!SL}	0.3735+0.0136*Cload	0.4135+0.0109*Cload	0.4280+0.0106*Cload
OE_PAD_T$_{PZL}${DS0&DS1&DS2&DS3&SL}	0.7759+0.0248*Cload	0.9335+0.0143*Cload	1.0730+0.0116*Cload
Timing Arc	**(< 0.03)pf**	**(0.03-0.3)pf**	**(> 0.3)pf**
PAD_C_T$_{PHL}${!ST}	0.2467+0.4750*Cload	0.2466+0.4780*Cload	0.2483+0.4745*Cload
PAD_C_T$_{PHL}${ST}	0.5228+0.4750*Cload	0.5226+0.4800*Cload	0.5227+0.4775*Cload
PAD_C_T$_{PLH}${!ST}	0.3202+0.4550*Cload	0.3203+0.4540*Cload	0.3197+0.4580*Cload
PAD_C_T$_{PLH}${ST}	0.5590+0.4550*Cload	0.5590+0.4560*Cload	0.5592+0.4545*Cload

9.27 PVDD08CODCDGM_H

Digital VDDPST08 power and ground combo cell

Truth Table

INPUT											OUTPUT
VDDPST12	VDDPST08	VDDPST04	VDD	ESDB	ESD12	ESD12B	POCCTRL	POCCTRL12	POCCTRLD	RTE	ESDB
1	1	1	0/1	-	-	-	-	-	-	-	1
0	1	0/1	0/1	-	-	-	-	-	-	-	1
0	0	0/1	0/1	-	-	-	-	-	-	-	0

*All undefined states in truth table are illegal operation

Cell Information

	Value	Unit
Cell Width	55.584	um
Cell Height	31.2	um
Pad Number	2	-

Leakage Power

	Value	Unit
VDDPST12	19.12	nW

Pin Capacitance

	Value	Unit
ESD12	0.008066	pF
ESD12B	0.007131	pF
ESDB	5.498	pF
POCCTRL	0.006758	pF
POCCTRL12	0.006706	pF
POCCTRLD	0.006663	pF
RTE	0.00659	pF

9.28 PVDD08CODCDGM_V

Digital VDDPST08 power and ground combo cell

Truth Table

INPUT											OUTPUT
VDDPST12	VDDPST08	VDDPST04	VDD	ESDB	ESD12	ESD12B	POCCTRL	POCCTRL12	POCCTRLD	RTE	ESDB
1	1	1	0/1	-	-	-	-	-	-	-	1
0	1	0/1	0/1	-	-	-	-	-	-	-	1
0	0	0/1	0/1	-	-	-	-	-	-	-	0

*All undefined states in truth table are illegal operation

Cell Information

	Value	Unit
Cell Width	31.104	um
Cell Height	55.77	um
Pad Number	2	-

Leakage Power

	Value	Unit
VDDPST12	19.28	nW

Leakage Power

	Value	Unit
VDDPST08	2.295e+04	nW

Leakage Power

	Value	Unit
VDD	0	nW

Leakage Power

	Value	Unit
VDDPST04	0	nW

Pin Capacitance

	Value	Unit
ESD12	0.008072	pF
ESD12B	0.007209	pF
ESDB	4.988	pF
POCCTRL	0.006299	pF
POCCTRL12	0.006228	pF
POCCTRLD	0.006124	pF
RTE	0.006308	pF

9.29 PVDD1204CODCDGM_H

Digital 1.2V power, VDDPST04 and ground combo cell

Truth Table

INPUT											OUTPUT	
VDDPST12	VDDPST08	VDDPST04	VDD	ESDB	ESD12	ESD12B	POCCTRL	POCCTRL12	POCCTRLD	RTE	ESD12	ESD12B
1	1	1	0/1	-	-	-	-	-	-	-	0	1
0	1	0/1	0/1	-	-	-	-	-	-	-	0	0
0	0	0/1	0/1	-	-	-	-	-	-	-	0	0

*All undefined states in truth table are illegal operation

Cell Information

	Value	Unit
Cell Width	55.584	um
Cell Height	62.4	um
Pad Number	3	-

Leakage Power

	Value	Unit
VDDPST12	2.988e+04	nW

Leakage Power

	Value	Unit
VDDPST08	0	nW

Leakage Power

	Value	Unit
VDD	0	nW

Leakage Power

	Value	Unit
VDDPST04	1.047e+04	nW

Pin Capacitance

	Value	Unit
ESD12	1.48	pF
ESD12B	26.62	pF
ESDB	0.01696	pF
POCCTRL	0.01462	pF
POCCTRL12	0.01567	pF
POCCTRLD	0.01429	pF
RTE	0.01587	pF

9.30 PVDD1204CODCDGM_V

Digital 1.2V power, VDDPST04 and ground combo cell

Truth Table

INPUT											OUTPUT	
VDDPST12	VDDPST08	VDDPST04	VDD	ESDB	ESD12	ESD12B	POCCTRL	POCCTRL12	POCCTRLD	RTE	ESD12	ESD12B
1	1	1	0/1	-	-	-	-	-	-	-	0	1
0	1	0/1	0/1	-	-	-	-	-	-	-	0	0
0	0	0/1	0/1	-	-	-	-	-	-	-	0	0

*All undefined states in truth table are illegal operation

Cell Information

	Value	Unit
Cell Width	62.016	um
Cell Height	55.77	um
Pad Number	3	-

Leakage Power

	Value	Unit
VDDPST12	2.959e+04	nW

Leakage Power

	Value	Unit
VDDPST08	0	nW

Leakage Power

	Value	Unit
VDD	0	nW

Leakage Power

	Value	Unit
VDDPST04	1.064e+04	nW

Pin Capacitance

	Value	Unit
ESD12	1.37	pF
ESD12B	12.29	pF
ESDB	0.01642	pF
POCCTRL	0.0153	pF
POCCTRL12	0.01345	pF
POCCTRLD	0.01521	pF
RTE	0.01373	pF

9.31 PVDD12CODCDGM_H

Digital 1.2V power and ground combo cell

Truth Table

INPUT											OUTPUT	
VDDPST12	VDDPST08	VDDPST04	VDD	ESDB	ESD12	ESD12B	POCCTRL	POCCTRL12	POCCTRLD	RTE	ESD12	ESD12B
1	1	1	0/1	-	-	-	-	-	-	-	0	1
0	1	0/1	0/1	-	-	-	-	-	-	-	0	0
0	0	0/1	0/1	-	-	-	-	-	-	-	0	0

*All undefined states in truth table are illegal operation

Cell Information

	Value	Unit
Cell Width	55.584	um
Cell Height	72.8	um
Pad Number	2	-

Leakage Power

	Value	Unit
VDDPST12	6.521e+04	nW

Leakage Power

	Value	Unit
VDDPST08	0	nW

Leakage Power

	Value	Unit
VDD	0	nW

Leakage Power

	Value	Unit
VDDPST04	0	nW

Pin Capacitance

	Value	Unit
ESD12	3.022	pF
ESD12B	3.129	pF
ESDB	0.01396	pF
POCCTRL	0.0113	pF
POCCTRL12	0.01138	pF
POCCTRLD	0.01108	pF
RTE	0.01053	pF

9.32 PVDD12CODCDGM_V

Digital 1.2V power and ground combo cell

Truth Table

INPUT											OUTPUT	
VDDPST12	VDDPST08	VDDPST04	VDD	ESDB	ESD12	ESD12B	POCCTRL	POCCTRL12	POCCTRLD	RTE	ESD12	ESD12B
1	1	1	0/1	-	-	-	-	-	-	-	0	1
0	1	0/1	0/1	-	-	-	-	-	-	-	0	0
0	0	0/1	0/1	-	-	-	-	-	-	-	0	0

*All undefined states in truth table are illegal operation

Cell Information

	Value	Unit
Cell Width	72.768	um
Cell Height	55.77	um
Pad Number	2	-

Leakage Power

	Value	Unit
VDDPST12	6.532e+04	nW

Leakage Power

	Value	Unit
VDDPST08	0	nW

Leakage Power

	Value	Unit
VDD	0	nW

Leakage Power

	Value	Unit
VDDPST04	0	nW

Pin Capacitance

	Value	Unit
ESD12	2.583	pF
ESD12B	2.697	pF
ESDB	0.01678	pF
POCCTRL	0.0135	pF
POCCTRL12	0.01454	pF
POCCTRLD	0.0144	pF
RTE	0.01453	pF

9.33 PVDD12CODPOC_H

Power-on-control cell

Truth Table

INPUT								OUTPUT				
VDD	VDDPST12	VDDPST08	VDDPST04	ESDB	ESD12	ESD12B	IRTE	RTE	POCCTRL	POCCTRLD	POCCTRL12	TIEL
1	1	1	1	1	0	1	0	0	0	0	0	0
0	1	1	1	1	0	1	0	0	1	1	0	0
0/1	1	1	1	1	0	1	1	1	0	0	0	0
1	0	1	1	1	0	0	0	0	1	1	0	0
0	0	1	1	1	0	0	0	0	1	1	0	0
1	0	1	0	1	0	0	0	0	1	1	0	0
0	0	1	0	1	0	0	0	0	1	1	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0

*All undefined states in truth table are illegal operation

Cell Information

	Value	Unit
Cell Width	55.584	um
Cell Height	28.08	um

Leakage Power

	Value	Unit
VDDPST12	1.399e+04	nW

Leakage Power

	Value	Unit
VDDPST08	4906	nW

Leakage Power

	Value	Unit
VDD	15.87	nW

Leakage Power

	Value	Unit
VDDPST04	1e-10	nW

Pin Capacitance

	Value	Unit
ESD12	0.00675	pF
ESD12B	0.005518	pF
ESDB	0.01219	pF
IRTE	0.03417	pF

9.34 PVDD12CODPOC_V

Power-on-control cell

Truth Table

INPUT								OUTPUT				
VDD	VDDPST12	VDDPST08	VDDPST04	ESDB	ESD12	ESD12B	IRTE	RTE	POCCTRL	POCCTRLD	POCCTRL12	TIEL
1	1	1	1	1	0	1	0	0	0	0	0	0
0	1	1	1	1	0	1	0	0	1	1	0	0
0/1	1	1	1	1	0	1	1	1	0	0	0	0
1	0	1	1	1	0	0	0	0	1	1	0	0
0	0	1	1	1	0	0	0	0	1	1	0	0
1	0	1	0	1	0	0	0	0	1	1	0	0
0	0	1	0	1	0	0	0	0	1	1	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0

*All undefined states in truth table are illegal operation

Cell Information

	Value	Unit
Cell Width	28.08	um
Cell Height	55.77	um

Leakage Power

	Value	Unit
VDDPST12	1.399e+04	nW

Leakage Power

	Value	Unit
VDDPST08	4907	nW

Leakage Power

	Value	Unit
VDD	15.87	nW

Leakage Power

	Value	Unit
VDDPST04	1e-10	nW

Pin Capacitance

	Value	Unit
ESD12	0.009292	pF
ESD12B	0.00818	pF
ESDB	0.01566	pF
IRTE	0.03705	pF

9.35 PVDD1CODANAM_H

Analog core power and ground combo cell, compatible to be used in digital IO domain

Cell Information

	Value	Unit
Cell Width	55.584	um
Cell Height	31.2	um
Pad Number	2	-

Leakage Power

	Value	Unit
AVDD	2.038e+04	nW

Pin Capacitance

	Value	Unit
ESD12	0.008954	pF
ESD12B	0.008177	pF
ESDB	0.008917	pF
POCCTRL	0.00698	pF
POCCTRL12	0.007196	pF
POCCTRLD	0.007395	pF
RTE	0.007383	pF

9.36 PVDD1CODANAM_V

Analog core power and ground combo cell, compatible to be used in digital IO domain

Cell Information

	Value	Unit
Cell Width	31.104	um
Cell Height	55.77	um
Pad Number	2	-

Leakage Power

	Value	Unit
AVDD	2.007e+04	nW

Pin Capacitance

	Value	Unit
ESD12	0.007885	pF
ESD12B	0.008174	pF
ESDB	0.008219	pF
POCCTRL	0.006652	pF
POCCTRL12	0.006851	pF
POCCTRLD	0.006939	pF
RTE	0.006695	pF

9.37 PVDD1CODCDGM_H

Digital core power VDD and ground combo cell

Cell Information

	Value	Unit
Cell Width	55.584	um
Cell Height	31.2	um
Pad Number	2	-

Leakage Power

	Value	Unit
VDDPST12	0	nW

Leakage Power

	Value	Unit
VDDPST08	0	nW

Leakage Power

	Value	Unit
VDD	2.038e+04	nW

Leakage Power

	Value	Unit
VDDPST04	0	nW

Pin Capacitance

	Value	Unit
ESD12	0.008938	pF
ESD12B	0.008166	pF
ESDB	0.008948	pF
POCCTRL	0.00699	pF
POCCTRL12	0.007195	pF
POCCTRLD	0.007373	pF
RTE	0.007418	pF

9.38 PVDD1CODCDGM_V

Digital core power VDD and ground combo cell

Cell Information

	Value	Unit
Cell Width	31.104	um
Cell Height	55.77	um
Pad Number	2	-

Leakage Power

	Value	Unit
VDDPST12	0	nW

Leakage Power

	Value	Unit
VDDPST08	0	nW

Leakage Power

	Value	Unit
VDD	2.007e+04	nW

Leakage Power

	Value	Unit
VDDPST04	0	nW

Pin Capacitance

	Value	Unit
ESD12	0.007895	pF
ESD12B	0.008173	pF
ESDB	0.008281	pF
POCCTRL	0.006656	pF
POCCTRL12	0.006885	pF
POCCTRLD	0.006904	pF
RTE	0.006693	pF