* When running the **awg\_dig\_pd** HVI sequence, make sure the DIG external trigger is set to "output+input" (Module -> Trigger/Clock settings...).
* At the AWG HVI sequence, the second instruction ("Waveshape") is used to enable the output relays. It can be set into a separated HVI sequence and run only once (if the AWG board hasn’t been used after power on). It requires at least 125 us in order to enable them.
* For the HVI phase detector demo, configure the DIG front panel at **VIRTUALknob**:

2500 points  
CH0: 2v, 50 ohms  
CH1: 2v, 50 ohms  
Mode: Slave

* At the **awg\_dig\_pd** HVI sequence, if the Register 9 of the DIG board shows a big value, initial phase between signals can be tweaked changing the default value of the AWG’s Register 1 (10º by default, Module -> Register Settings…).
* At the **PC\_PORTS** phase detector example the AWG output signals have an error of 4 degrees (which leads into an initial phase difference of 356 degrees). It can be corrected by setting an initial phase for CH1 of 4 degrees.