

# TCA9535 Low-Voltage 16-Bit I<sup>2</sup>C and SMBus Low-Power I/O Expander with Interrupt Output and Configuration Registers

## 1 Features

- I<sup>2</sup>C to Parallel port expander
- Wide power supply voltage range of 1.65 V to 5 V
- Low standby-current consumption
- Open-drain active-low interrupt output
- 5-V tolerant I/O ports
- 400-kHz Fast I<sup>2</sup>C bus
- Polarity inversion register
- Address by three hardware address pins for use of up to eight devices
- Latched outputs with high-current drive capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD 78, class II
- ESD protection exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

## 2 Applications

- Servers
- Routers (telecom switching equipment)
- [Personal computers](#)
- [Personal electronics](#) (for example, gaming consoles)
- [Industrial automation](#)
- [Products with GPIO-limited processors](#)

## 3 Description

The TCA9535 is a 24-pin device that provides 16 bits of general purpose parallel input and output (I/O) expansion for the two-line bidirectional I<sup>2</sup>C bus or (SMBus) protocol. The device can operate with a power supply voltage ranging from 1.65 V to 5.5 V.

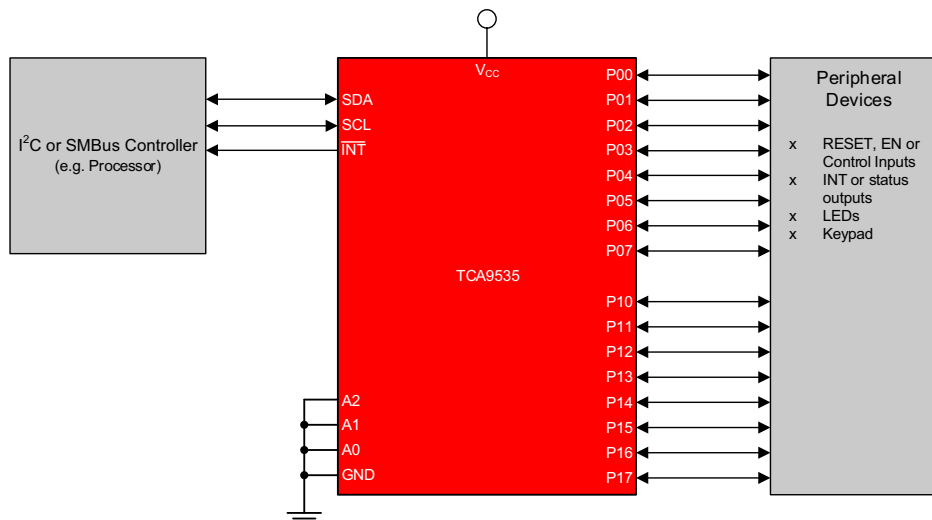
The TCA9535 consists of two 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active-high or active-low operation) registers. At power on, the I/Os are configured as inputs. The system controller can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits.

The TCA9535 is identical to the [TCA9555](#), except that the TCA9535 does not include the internal I/O pull-up resistor, which requires pull-ups and pull-downs on unused I/O pins when configured as an input and undriven.

### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
TCA9535	TSSOP (24)	7.80 mm x 4.40 mm
	SSOP (24)	6.20 mm x 5.30 mm
	WQFN (24)	4.00 mm x 4.00 mm
	VQFN (24)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Block Diagram



## Table of Contents

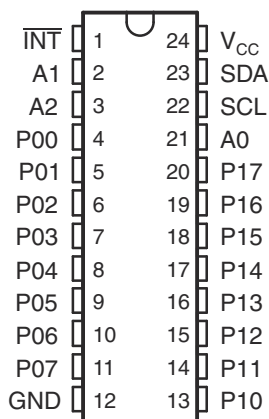
<b>1 Features</b> .....	<b>1</b>	7.5 Programming.....	<b>16</b>
<b>2 Applications</b> .....	<b>1</b>	7.6 Register Maps.....	<b>22</b>
<b>3 Description</b> .....	<b>1</b>	<b>8 Application and Implementation</b> .....	<b>23</b>
<b>4 Revision History</b> .....	<b>2</b>	8.1 Application Information.....	<b>23</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	8.2 Typical Application.....	<b>23</b>
<b>6 Specifications</b> .....	<b>4</b>	<b>9 Power Supply Recommendations</b> .....	<b>27</b>
6.1 Absolute Maximum Ratings.....	<b>4</b>	<b>10 Layout</b> .....	<b>29</b>
6.2 ESD Ratings.....	<b>4</b>	10.1 Layout Guidelines.....	<b>29</b>
6.3 Recommended Operating Conditions.....	<b>4</b>	10.2 Layout Example.....	<b>29</b>
6.4 Thermal Information.....	<b>5</b>	<b>11 Device and Documentation Support</b> .....	<b>30</b>
6.5 Electrical Characteristics.....	<b>5</b>	11.1 Documentation Support.....	<b>30</b>
6.6 I <sup>2</sup> C Interface Timing Requirements.....	<b>6</b>	11.2 Receiving Notification of Documentation Updates..	<b>30</b>
6.7 Switching Characteristics.....	<b>7</b>	11.3 Support Resources.....	<b>30</b>
6.8 Typical Characteristics.....	<b>8</b>	11.4 Trademarks.....	<b>30</b>
<b>7 Detailed Description</b> .....	<b>14</b>	11.5 Electrostatic Discharge Caution.....	<b>30</b>
7.1 Overview.....	<b>14</b>	11.6 Glossary.....	<b>30</b>
7.2 Functional Block Diagram.....	<b>14</b>	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	<b>30</b>
7.3 Feature Description.....	<b>15</b>		
7.4 Device Functional Modes.....	<b>16</b>		

## 4 Revision History

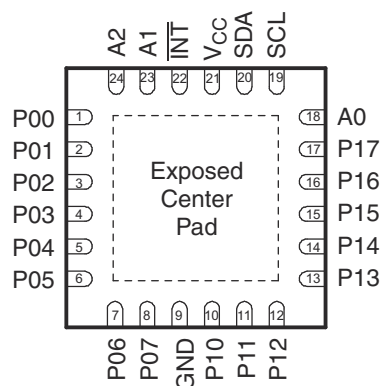
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision D (June 2016) to Revision E (May 2022)</b>	<b>Page</b>
• Globally changed instances of legacy terminology to controller and target where I <sup>2</sup> C is mentioned.....	<b>1</b>
• Changed V <sub>CC</sub> to GND on the Controlled Switch in <a href="#">Figure 8-1</a> .....	<b>23</b>
<b>Changes from Revision C (May 2016) to Revision D (June 2016)</b>	<b>Page</b>
• Added DB package .....	<b>1</b>
<b>Changes from Revision B (August 2015) to Revision C (May 2016)</b>	<b>Page</b>
• Added RGE package.....	<b>1</b>
• Added I <sub>OL</sub> for different T <sub>j</sub> .....	<b>4</b>
• Deleted ΔI <sub>CC</sub> spec from the Electrical Characteristics table, added ΔI <sub>CC</sub> typical characteristics graph.....	<b>5</b>
• Changed I <sub>CC</sub> standby into different input states, with increased maximums .....	<b>5</b>
• Changed C <sub>io</sub> maximum .....	<b>5</b>
<b>Changes from Revision A (September 2009) to Revision B (August 2015)</b>	<b>Page</b>
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	<b>1</b>

## 5 Pin Configuration and Functions



**Figure 5-1. DB, PW (TSSOP) Package  
24-Pin (Top View)**



The exposed center pad, if used, must be connected as a secondary ground or left electrically open.

**Figure 5-2. RTW (WQFN), RGE (VQFN) Package  
24-Pin (Top View)**

**Table 5-1. Pin Functions**

PIN			TYPE	DESCRIPTION
NAME	NO.			
	DB, PW	RTW, RGE		
A0	21	18	Input	Address input 0. Connect directly to V <sub>CC</sub> or ground
A1	2	23	Input	Address input 1. Connect directly to V <sub>CC</sub> or ground
A2	3	24	Input	Address input 2. Connect directly to V <sub>CC</sub> or ground
GND	12	9	—	Ground
INT	1	22	Output	Interrupt output. Connect to V <sub>CC</sub> through an external pull-up resistor
P00 <sup>(1)</sup>	4	1	I/O	P-port I/O. Push-pull design structure. At power on, P00 is configured as an input
P01 <sup>(1)</sup>	5	2	I/O	P-port I/O. Push-pull design structure. At power on, P01 is configured as an input
P02 <sup>(1)</sup>	6	3	I/O	P-port I/O. Push-pull design structure. At power on, P02 is configured as an input
P03 <sup>(1)</sup>	7	4	I/O	P-port I/O. Push-pull design structure. At power on, P03 is configured as an input
P04 <sup>(1)</sup>	8	5	I/O	P-port I/O. Push-pull design structure. At power on, P04 is configured as an input
P05 <sup>(1)</sup>	9	6	I/O	P-port I/O. Push-pull design structure. At power on, P05 is configured as an input
P06 <sup>(1)</sup>	10	7	I/O	P-port I/O. Push-pull design structure. At power on, P06 is configured as an input
P07 <sup>(1)</sup>	11	8	I/O	P-port I/O. Push-pull design structure. At power on, P07 is configured as an input
P10 <sup>(1)</sup>	13	10	I/O	P-port I/O. Push-pull design structure. At power on, P10 is configured as an input
P11 <sup>(1)</sup>	14	11	I/O	P-port I/O. Push-pull design structure. At power on, P11 is configured as an input
P12 <sup>(1)</sup>	15	12	I/O	P-port I/O. Push-pull design structure. At power on, P12 is configured as an input
P13 <sup>(1)</sup>	16	13	I/O	P-port I/O. Push-pull design structure. At power on, P13 is configured as an input
P14 <sup>(1)</sup>	17	14	I/O	P-port I/O. Push-pull design structure. At power on, P14 is configured as an input
P15 <sup>(1)</sup>	18	15	I/O	P-port I/O. Push-pull design structure. At power on, P15 is configured as an input
P16 <sup>(1)</sup>	19	16	I/O	P-port I/O. Push-pull design structure. At power on, P16 is configured as an input
P17 <sup>(1)</sup>	20	17	I/O	P-port I/O. Push-pull design structure. At power on, P17 is configured as an input
SCL	22	19	Input	Serial clock bus. Connect to V <sub>CC</sub> through a pull-up resistor
SDA	23	20	Input	Serial data bus. Connect to V <sub>CC</sub> through a pull-up resistor
V <sub>CC</sub>	24	21	—	Supply voltage

(1) If port is unused, it must be tied to either V<sub>CC</sub> or GND through a resistor of moderate value (about 10 kΩ)

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	–0.5	6	V
V <sub>I</sub>	Input voltage <sup>(2)</sup>	–0.5	6	V
V <sub>O</sub>	Output voltage <sup>(2)</sup>	–0.5	6	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		–20 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		–20 mA
I <sub>IOK</sub>	Input-output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>		±20 mA
I <sub>OL</sub>	Continuous output low current	V <sub>O</sub> = 0 to V <sub>CC</sub>		50 mA
I <sub>OH</sub>	Continuous output high current	V <sub>O</sub> = 0 to V <sub>CC</sub>		–50 mA
I <sub>CC</sub>	Continuous current through GND			–250 mA
	Continuous current through V <sub>CC</sub>			160 mA
T <sub>J(MAX)</sub>	Maximum junction temperature			100 °C
T <sub>stg</sub>	Storage temperature	–65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		1.65	5.5	V
V <sub>IH</sub>	High-level input voltage	SCL, SDA	0.7 × V <sub>CC</sub>	V <sub>CC</sub> <sup>(1)</sup>	V
		A2–A0, P07–P00, P17–P10	0.7 × V <sub>CC</sub>	5.5	V
V <sub>IL</sub>	Low-level input voltage	SCL, SDA, A2–A0, P07–P00, P17–P10	–0.5	0.3 × V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	P07–P00, P17–P10		–10	mA
I <sub>OL</sub>	Low-level output current <sup>(2)</sup>	P07–P00, P17–P10	T <sub>J</sub> ≤ 65°C	25	mA
			T <sub>J</sub> ≤ 85°C	18	
			T <sub>J</sub> ≤ 100°C	11	
I <sub>OL</sub>	Low-level output current <sup>(2)</sup>	INT, SDA	T <sub>J</sub> ≤ 85°C	6	mA
			T <sub>J</sub> ≤ 100°C	3.5	
T <sub>A</sub>	Operating free-air temperature		–40	85	°C

- (1) For voltages applied above V<sub>CC</sub>, an increase in I<sub>CC</sub> results.
- (2) The values shown apply to specific junction temperatures, which depend on the R<sub>θJA</sub> of the package used. See the [Calculating Junction Temperature and Power Dissipation](#) section on how to calculate the junction temperature.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TCA9535				UNIT
		PW (TSSOP)	DB (SSOP)	RTW (WQFN)	RGE (VQFN)	
		24 PINS	24 PINS	24 PINS	24 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	108.8	92.9	43.6	48.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	54	53.5	46.2	58.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	62.8	50.4	22.1	27.1	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	11.1	21.9	1.5	3.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	62.3	50.1	22.2	27.2	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	10.7	15.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IK</sub>	Input diode clamp voltage	I <sub>I</sub> = –18 mA	1.65 V to 5.5 V	–1.2			V
V <sub>PORR</sub>	Power-on reset voltage, V <sub>CC</sub> rising	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0			1.2	1.5	V
V <sub>PORF</sub>	Power-on reset voltage, V <sub>CC</sub> falling	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0		0.75	1		V
V <sub>OH</sub>	P-port high-level output voltage <sup>(2)</sup>	I <sub>OH</sub> = –8 mA	1.65 V	1.2			V
			2.3 V	1.8			
			3 V	2.6			
			4.75 V	4.1			
		I <sub>OH</sub> = –10 mA	1.65 V	1			
			2.3 V	1.7			
			3 V	2.5			
			4.75 V	4			
I <sub>OL</sub>	Low-level output current	SDA	V <sub>OL</sub> = 0.4 V	1.65 V to 5.5 V	3		mA
		P port <sup>(3)</sup>	V <sub>OL</sub> = 0.5 V	1.65 V to 5.5 V	8		
			V <sub>OL</sub> = 0.7 V	1.65 V to 5.5 V	10		
		INT	V <sub>OL</sub> = 0.4 V	1.65 V to 5.5 V	3		
I <sub>I</sub>	Input leakage current	SCL, SDA Input leakage	V <sub>I</sub> = V <sub>CC</sub> or GND	1.65 V to 5.5 V		±1	μA
		A2–A0 Input leakage	V <sub>I</sub> = V <sub>CC</sub> or GND	1.65 V to 5.5 V		±1	
I <sub>IH</sub>	Input high leakage current	P port	V <sub>I</sub> = V <sub>CC</sub>	1.65 V to 5.5 V		1	μA
I <sub>IL</sub>	Input low leakage current	P port	V <sub>I</sub> = GND	1.65 V to 5.5 V		–1	μA

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
I <sub>CC</sub>	Quiescent current	Operating mode V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0, I/O = inputs, f <sub>SCL</sub> = 400 kHz, No load	5.5 V		22	40	μA
			3.6 V		11	30	
			2.7 V		8	19	
			1.95 V		5	11	
	Standby mode	V <sub>I</sub> = V <sub>CC</sub> , I <sub>O</sub> = 0, I/O = inputs, f <sub>SCL</sub> = 0 kHz, No load	5.5 V		1.5	3.9	
			3.6 V		0.9	2.2	
			2.7 V		0.6	1.8	
			1.95 V		0.6	1.5	
		V <sub>I</sub> = GND, I <sub>O</sub> = 0, I/O = inputs, f <sub>SCL</sub> = 0 kHz, No load	5.5 V		1.5	8.7	
			3.6 V		0.9	4	
			2.7 V		0.6	3	
			1.95 V		0.4	2.2	
C <sub>I</sub>	Input capacitance	SCL	V <sub>I</sub> = V <sub>CC</sub> or GND	1.65 V to 5.5 V	3	8	pF
C <sub>IO</sub>	Input-output pin capacitance	SDA	V <sub>IO</sub> = V <sub>CC</sub> or GND	1.65 V to 5.5 V	3	9.5	pF
		P port	V <sub>IO</sub> = V <sub>CC</sub> or GND	1.65 V to 5.5 V	3.7	9.5	

- (1) All typical values are at nominal supply voltage (1.8-, 2.5-, 3.3-, or 5-V V<sub>CC</sub>) and T<sub>A</sub> = 25°C.
- (2) Each I/O must be externally limited to a maximum of 25 mA, and each octal (P07–P00 and P17–P10) must be limited to a maximum current of 100 mA, for a device total of 200 mA.
- (3) The total current sourced by all I/Os must be limited to 160 mA (80 mA for P07–P00 and 80 mA for P17–P10).

## 6.6 I<sup>2</sup>C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-2](#))

			MIN	MAX	UNIT
<b>I<sup>2</sup>C BUS—STANDARD MODE</b>					
f <sub>scl</sub>	I <sup>2</sup> C clock frequency		0	100	kHz
t <sub>sch</sub>	I <sup>2</sup> C clock high time		4		μs
t <sub>scl</sub>	I <sup>2</sup> C clock low time		4.7		μs
t <sub>sp</sub>	I <sup>2</sup> C spike time			50	ns
t <sub>sds</sub>	I <sup>2</sup> C serial-data setup time		250		ns
t <sub>sdh</sub>	I <sup>2</sup> C serial-data hold time		0		ns
t <sub>icr</sub>	I <sup>2</sup> C input rise time			1000	ns
t <sub>icf</sub>	I <sup>2</sup> C input fall time			300	ns
t <sub>ocf</sub>	I <sup>2</sup> C output fall time	10-pF to 400-pF bus		300	ns
t <sub>buf</sub>	I <sup>2</sup> C bus free time between stop and start		4.7		μs
t <sub>sts</sub>	I <sup>2</sup> C start or repeated start condition setup		4.7		μs
t <sub>sth</sub>	I <sup>2</sup> C start or repeated start condition hold		4		μs
t <sub>sps</sub>	I <sup>2</sup> C stop condition setup		4		μs
t <sub>vd(data)</sub>	Valid data time	SCL low to SDA output valid		3.45	μs
t <sub>vd(ack)</sub>	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		3.45	μs
C <sub>b</sub>	I <sup>2</sup> C bus capacitive load			400	pF
<b>I<sup>2</sup>C BUS—FAST MODE</b>					
f <sub>scl</sub>	I <sup>2</sup> C clock frequency		0	400	kHz
t <sub>sch</sub>	I <sup>2</sup> C clock high time		0.6		μs
t <sub>scl</sub>	I <sup>2</sup> C clock low time		1.3		μs

## 6.6 I<sup>2</sup>C Interface Timing Requirements (continued)

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-2](#))

			MIN	MAX	UNIT
t <sub>sp</sub>	I <sup>2</sup> C spike time			50	ns
t <sub>sds</sub>	I <sup>2</sup> C serial-data setup time		100		ns
t <sub>sdh</sub>	I <sup>2</sup> C serial-data hold time		0		ns
t <sub>icr</sub>	I <sup>2</sup> C input rise time		20	300	ns
t <sub>icf</sub>	I <sup>2</sup> C input fall time		20 × (V <sub>CC</sub> / 5.5 V)	300	ns
t <sub>ocf</sub>	I <sup>2</sup> C output fall time	10-pF to 400-pF bus	20 × (V <sub>CC</sub> / 5.5 V)	300	ns
t <sub>buf</sub>	I <sup>2</sup> C bus free time between stop and start		1.3		μs
t <sub>sts</sub>	I <sup>2</sup> C start or repeated start condition setup		0.6		μs
t <sub>sth</sub>	I <sup>2</sup> C start or repeated start condition hold		0.6		μs
t <sub>sps</sub>	I <sup>2</sup> C stop condition setup		0.6		μs
t <sub>vd(data)</sub>	Valid data time	SCL low to SDA output valid		0.9	μs
t <sub>vd(ack)</sub>	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		0.9	μs
C <sub>b</sub>	I <sup>2</sup> C bus capacitive load			400	pF

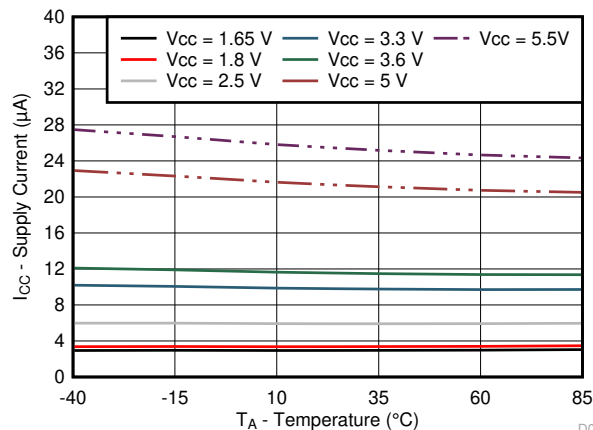
## 6.7 Switching Characteristics

over recommended operating free-air temperature range, C<sub>L</sub> ≤ 100 pF (unless otherwise noted) (see [Figure 7-2](#) and [Figure 7-3](#))

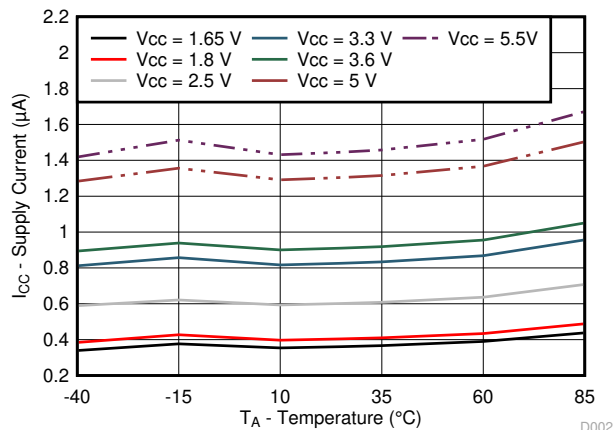
PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t <sub>iv</sub>	Interrupt valid time	P port	INT		4	μs
t <sub>ir</sub>	Interrupt reset delay time	SCL	INT		4	μs
t <sub>pv</sub>	Output data valid; For V <sub>CC</sub> = 2.3 V–5.5 V	SCL	P port		200	ns
	Output data valid; For V <sub>CC</sub> = 1.65 V–2.3 V				300	ns
t <sub>ps</sub>	Input data setup time	P port	SCL	150		ns
t <sub>ph</sub>	Input data hold time	P port	SCL	1		μs

## 6.8 Typical Characteristics

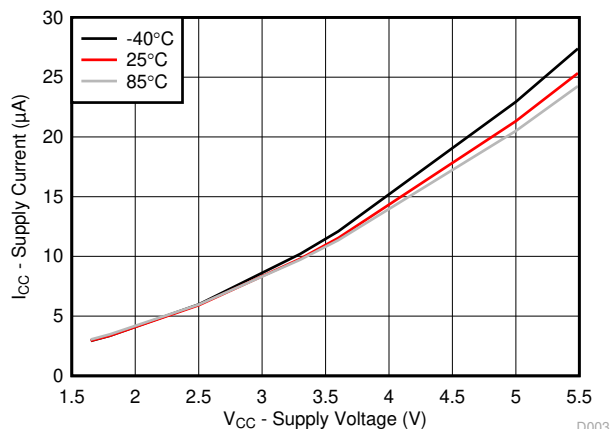
$T_A = 25^\circ\text{C}$  (unless otherwise noted)



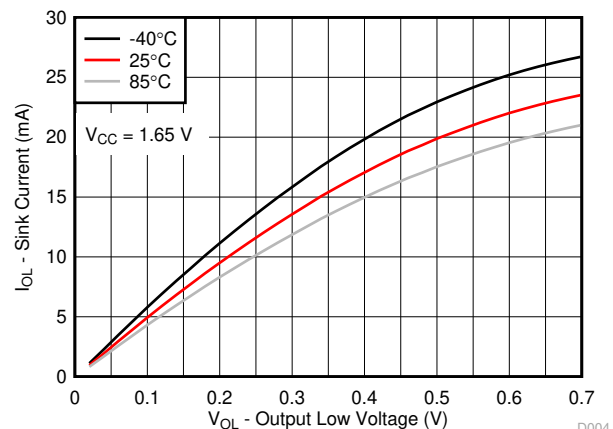
**Figure 6-1. Supply Current vs Temperature for Different Supply Voltage ( $V_{CC}$ )**



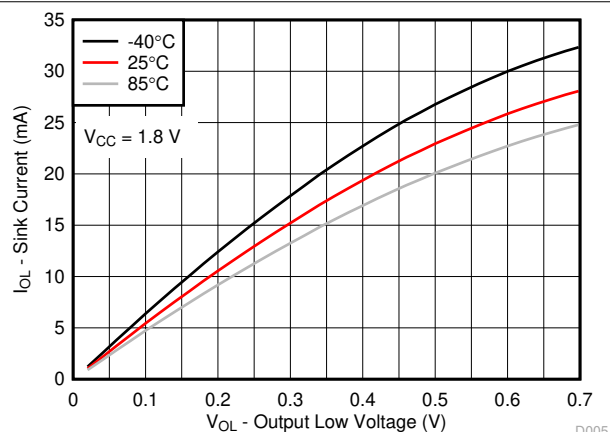
**Figure 6-2. Standby Supply Current vs Temperature for Different Supply Voltage ( $V_{CC}$ )**



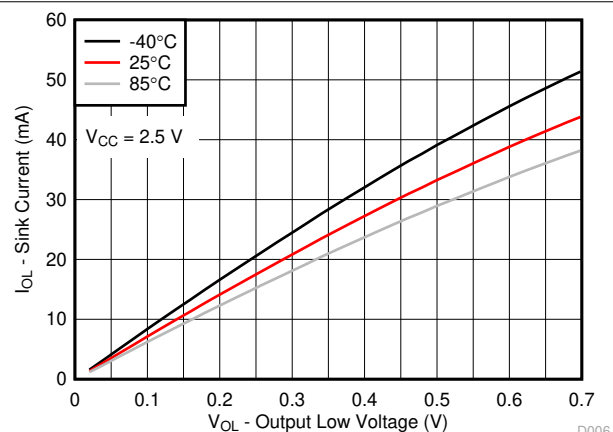
**Figure 6-3. Supply Current vs Supply Voltage for Different Temperature ( $T_A$ )**



**Figure 6-4. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 1.65\text{ V}$**



**Figure 6-5. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 1.8\text{ V}$**

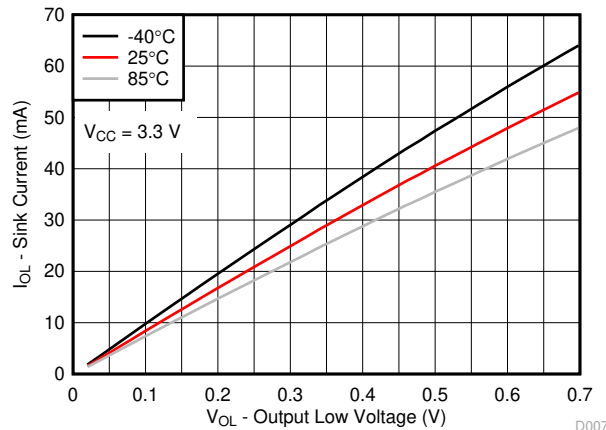


**Figure 6-6. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 2.5\text{ V}$**

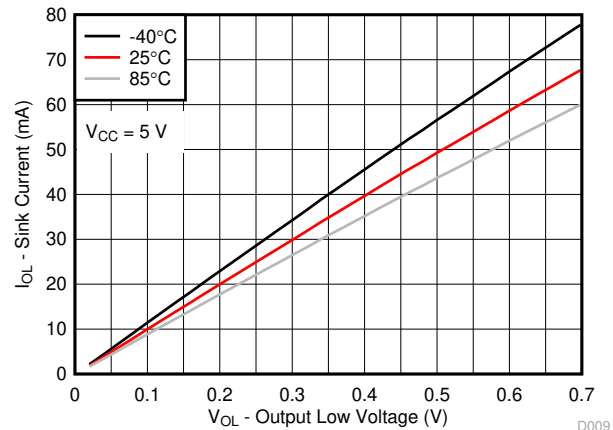


## 6.8 Typical Characteristics (continued)

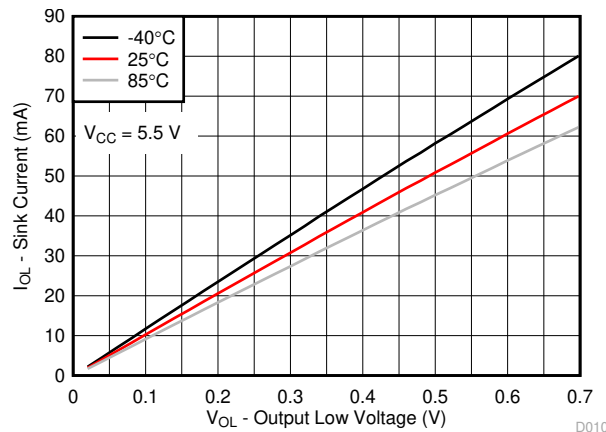
$T_A = 25^\circ\text{C}$  (unless otherwise noted)



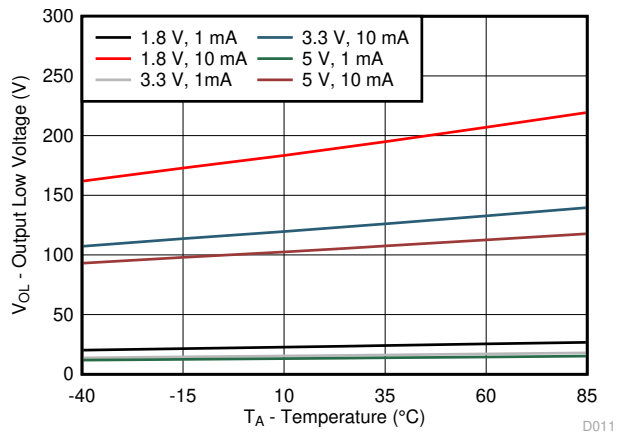
**Figure 6-7. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 3.3\text{ V}$**



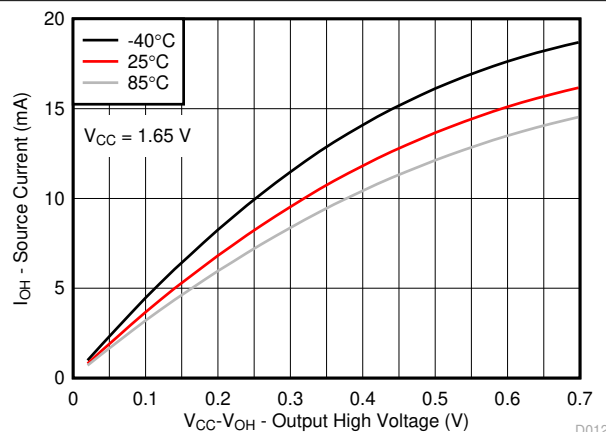
**Figure 6-8. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 5\text{ V}$**



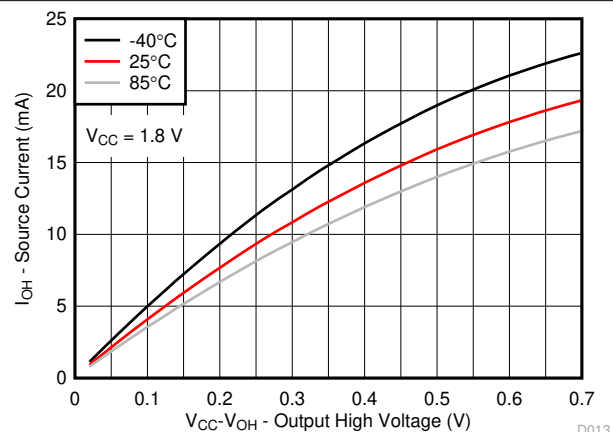
**Figure 6-9. I/O Sink Current vs Output Low Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 5.5\text{ V}$**



**Figure 6-10. I/O Low Voltage vs Temperature for Different  $V_{CC}$  and  $I_{OL}$**



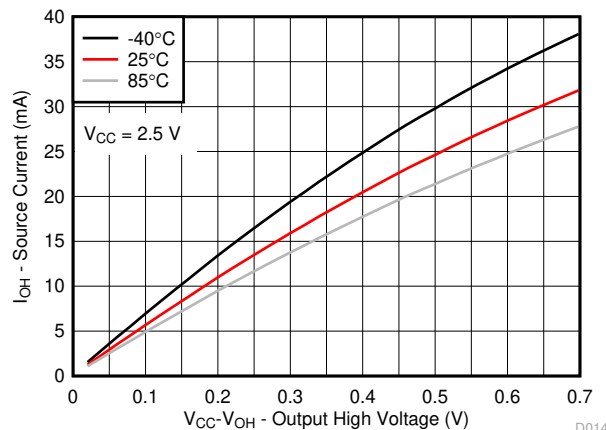
**Figure 6-11. I/O Source Current vs Output High Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 1.65\text{ V}$**



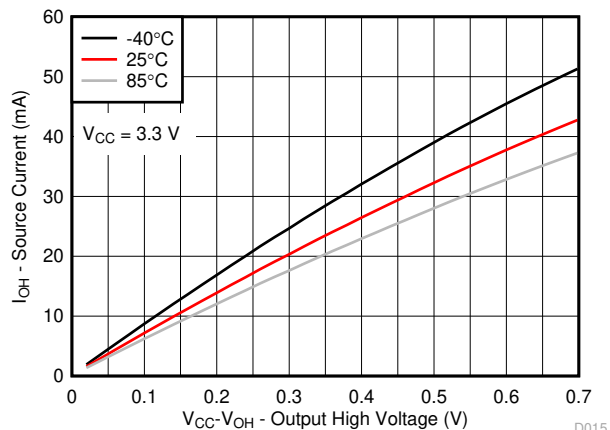
**Figure 6-12. I/O Source Current vs Output High Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 1.8\text{ V}$**

## 6.8 Typical Characteristics (continued)

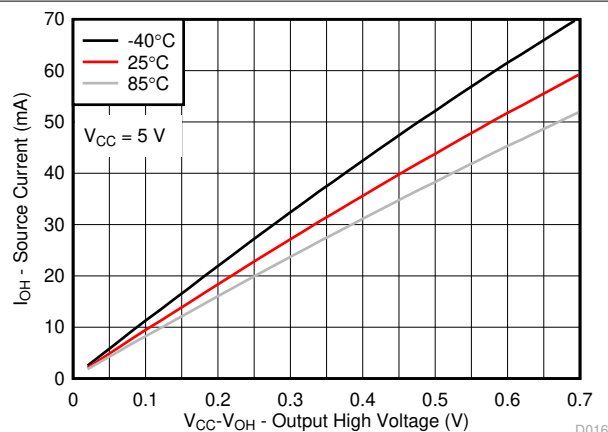
$T_A = 25^\circ\text{C}$  (unless otherwise noted)



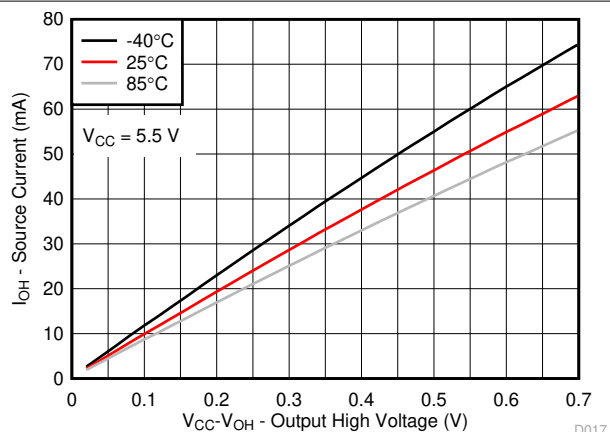
**Figure 6-13. I/O Source Current vs Output High Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 2.5\text{ V}$**



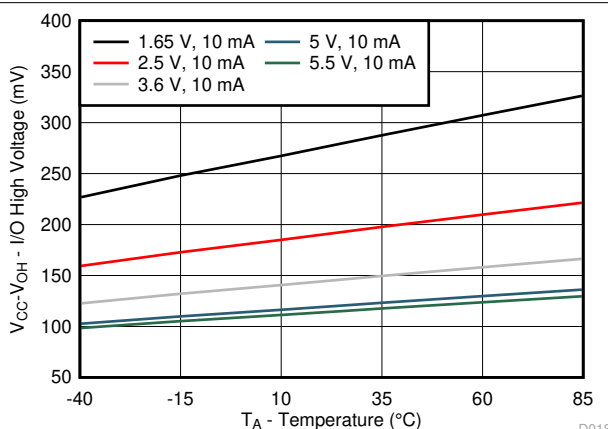
**Figure 6-14. I/O Source Current vs Output High Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 3.3\text{ V}$**



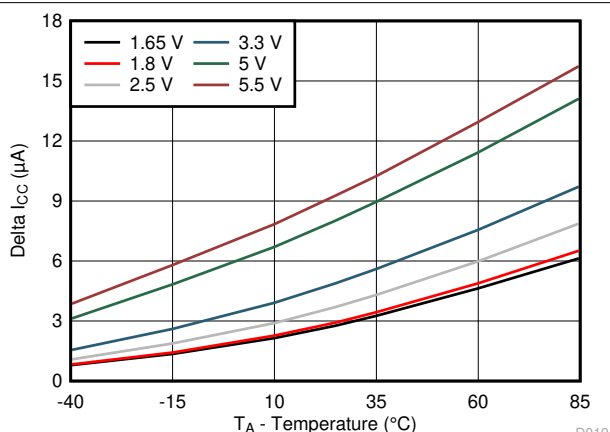
**Figure 6-15. I/O Source Current vs Output High Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 5\text{ V}$**



**Figure 6-16. I/O Source Current vs Output High Voltage for Different Temperature ( $T_A$ ) for  $V_{CC} = 5.5\text{ V}$**

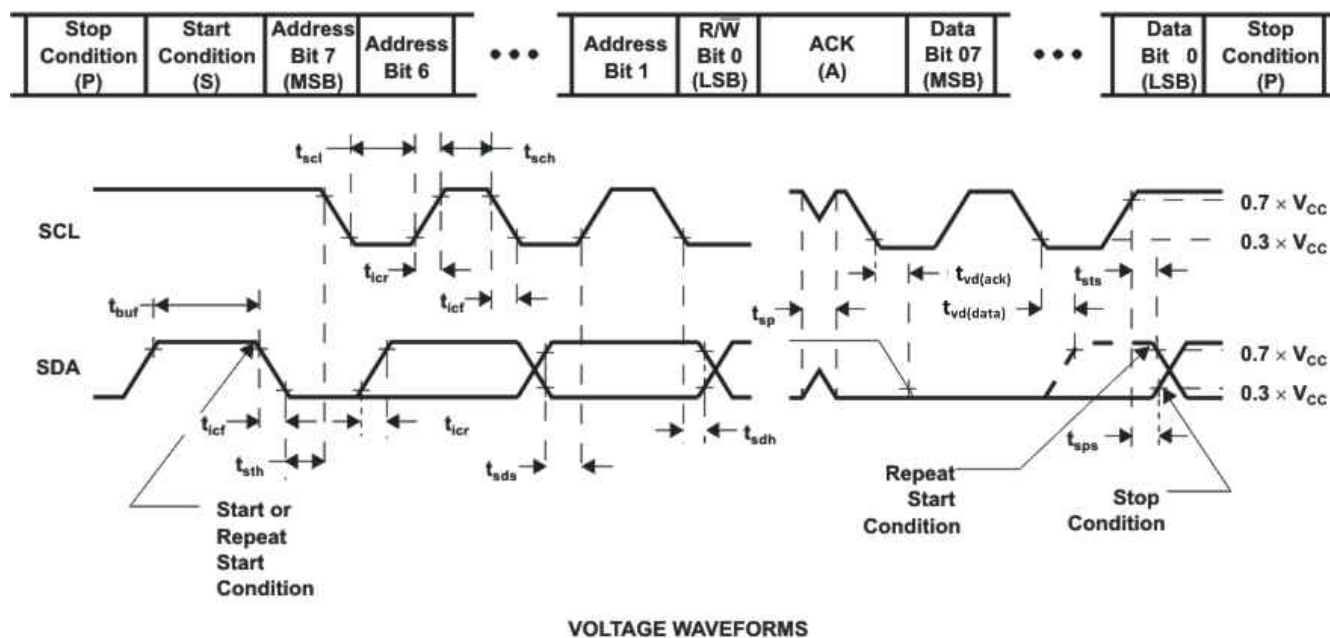
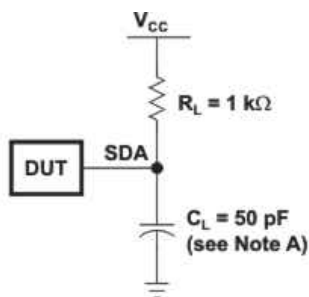


**Figure 6-17.  $V_{CC} - V_{OH}$  Voltage vs Temperature for Different  $V_{CC}$**



**Figure 6-18.  $\Delta I_{CC}$  vs Temperature for Different  $V_{CC}$  ( $V_I = V_{CC} - 0.6\text{ V}$ )**

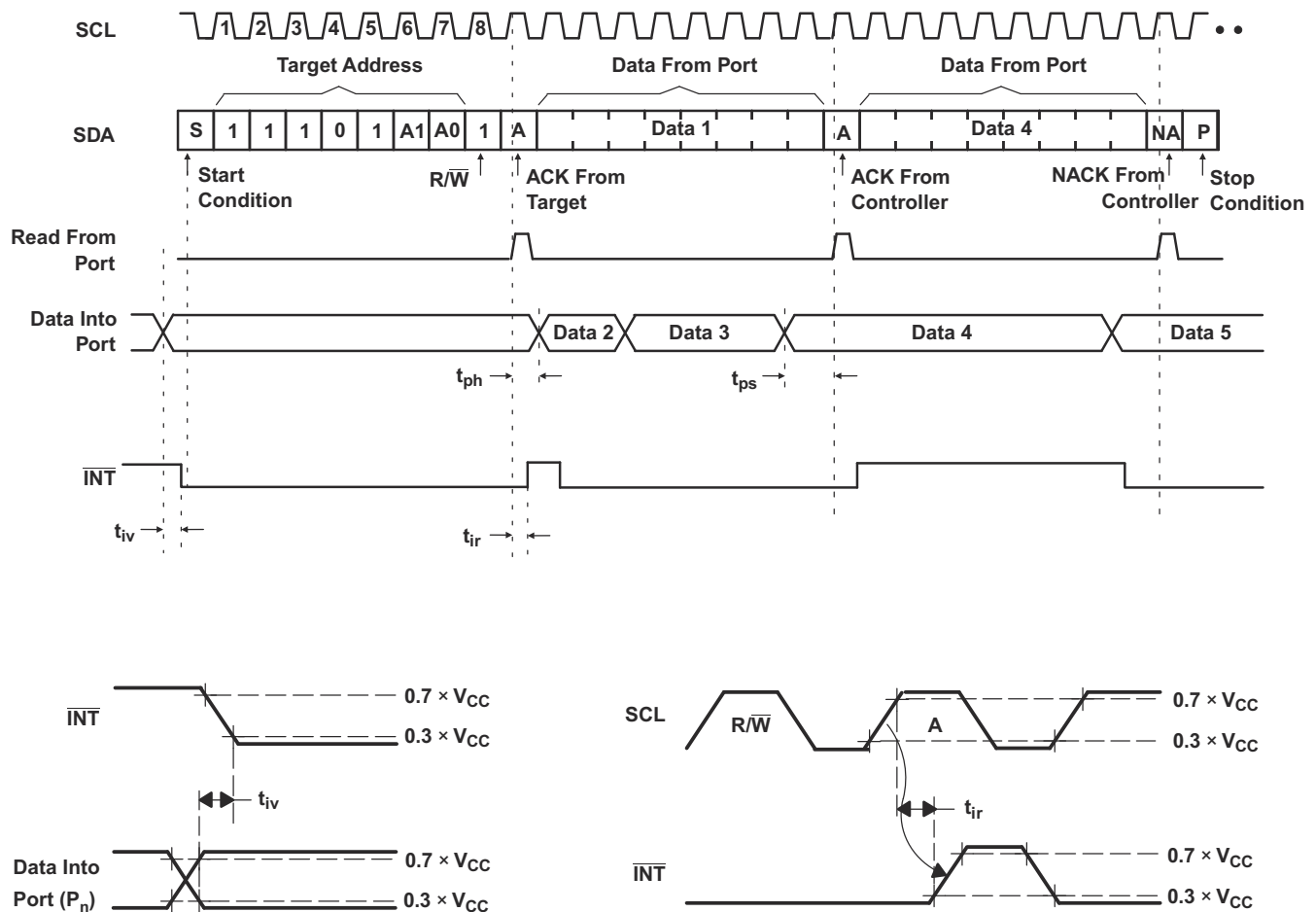
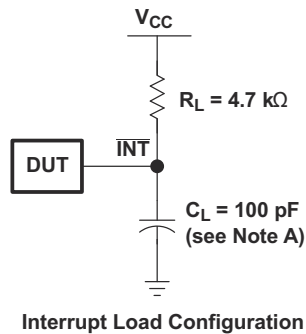
## Parameter Measurement Information



BYTE	DESCRIPTION
1	I <sup>2</sup> C address
2, 3	P-port data

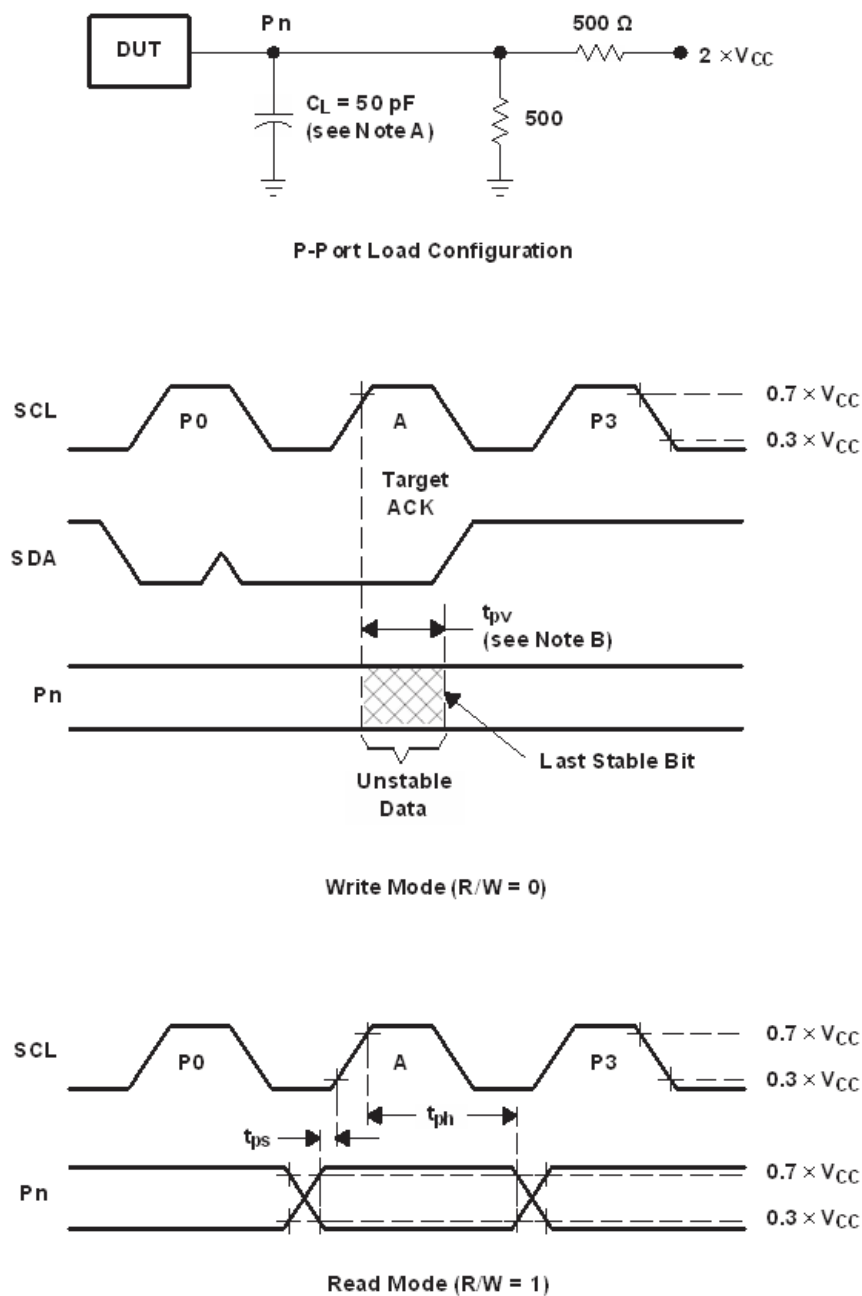
- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- C. All parameters and waveforms are not applicable to all devices.

**Figure 7-1. I<sup>2</sup>C Interface Load Circuit and Voltage Waveforms**



- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- C. All parameters and waveforms are not applicable to all devices.

**Figure 7-2. Interrupt Load Circuit and Voltage Waveforms**



- A.  $C_L$  includes probe and jig capacitance.
- B.  $t_{pv}$  is measured from  $0.7 \times V_{CC}$  on SCL to 50% I/O ( $P_n$ ) output.
- C. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

**Figure 7-3. P-Port Load Circuit and Voltage Waveforms**

## 7 Detailed Description

### 7.1 Overview

The TCA9535 device is a 16-bit I/O expander for the I<sup>2</sup>C bus and is designed for 1.65-V to 5.5-V  $V_{CC}$  operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I<sup>2</sup>C interface.

The TCA9535 consists of two 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active-high or active-low operation) registers. At power-on, the I/Os are configured as inputs. The system controller can enable the I/Os as either inputs or outputs by writing to the I/O configuration register bits. The data for each input or output is kept in the corresponding Input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system controller.

The TCA9535 open-drain interrupt ( $\overline{INT}$ ) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system controller that an input state has changed.

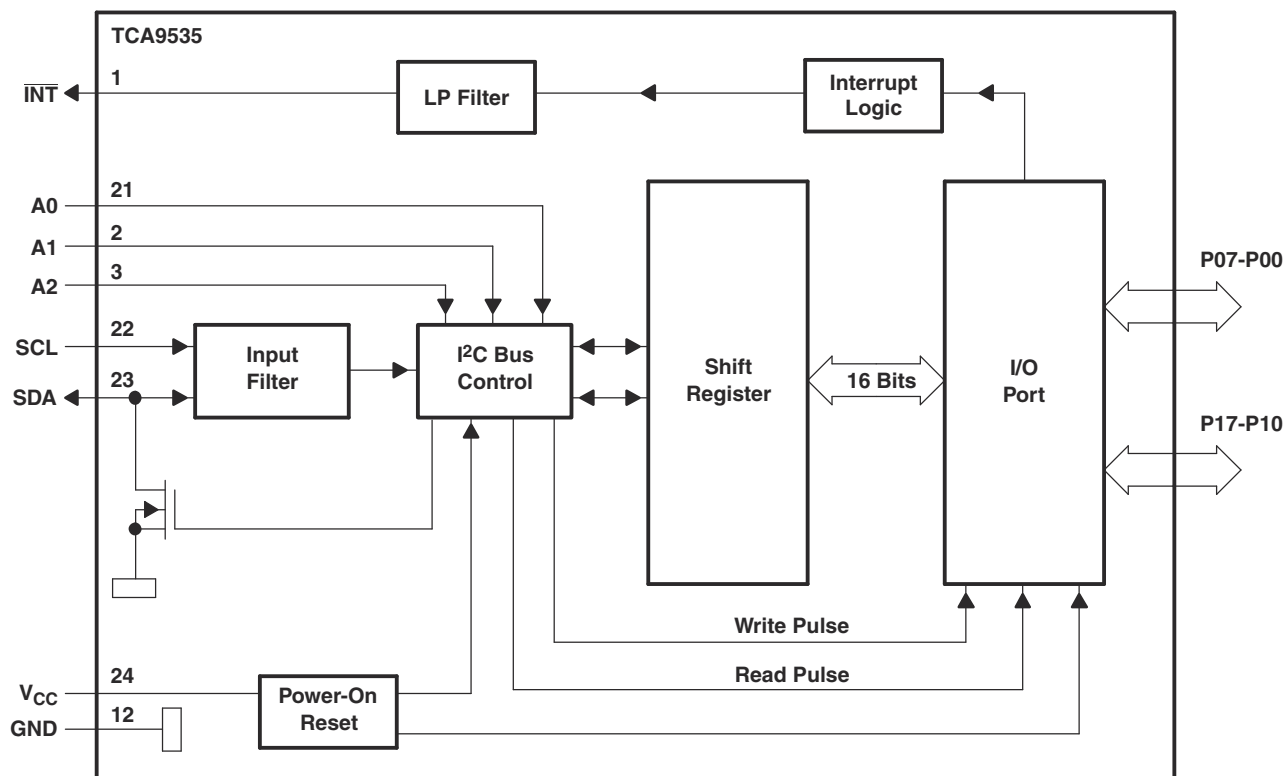
$\overline{INT}$  can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I<sup>2</sup>C bus. Thus, the TCA9535 can remain a simple target device.

The device outputs (latched) have high-current drive capability for directly driving LEDs. The device has low current consumption.

The TCA9535 device is similar to the PCA9555, except for the removal of the internal I/O pull-up resistor, which greatly reduces power consumption when the I/Os are held low. The TCA9535 is equivalent to the PCA9535 with lower voltage support (down to  $V_{CC} = 1.65$  V), and also improved power-on-reset circuitry for different application scenarios.

Three hardware pins (A0, A1 and A2) are used to program and vary the fixed I<sup>2</sup>C address and allow up to 8 devices to share the same I<sup>2</sup>C bus or SMBus.

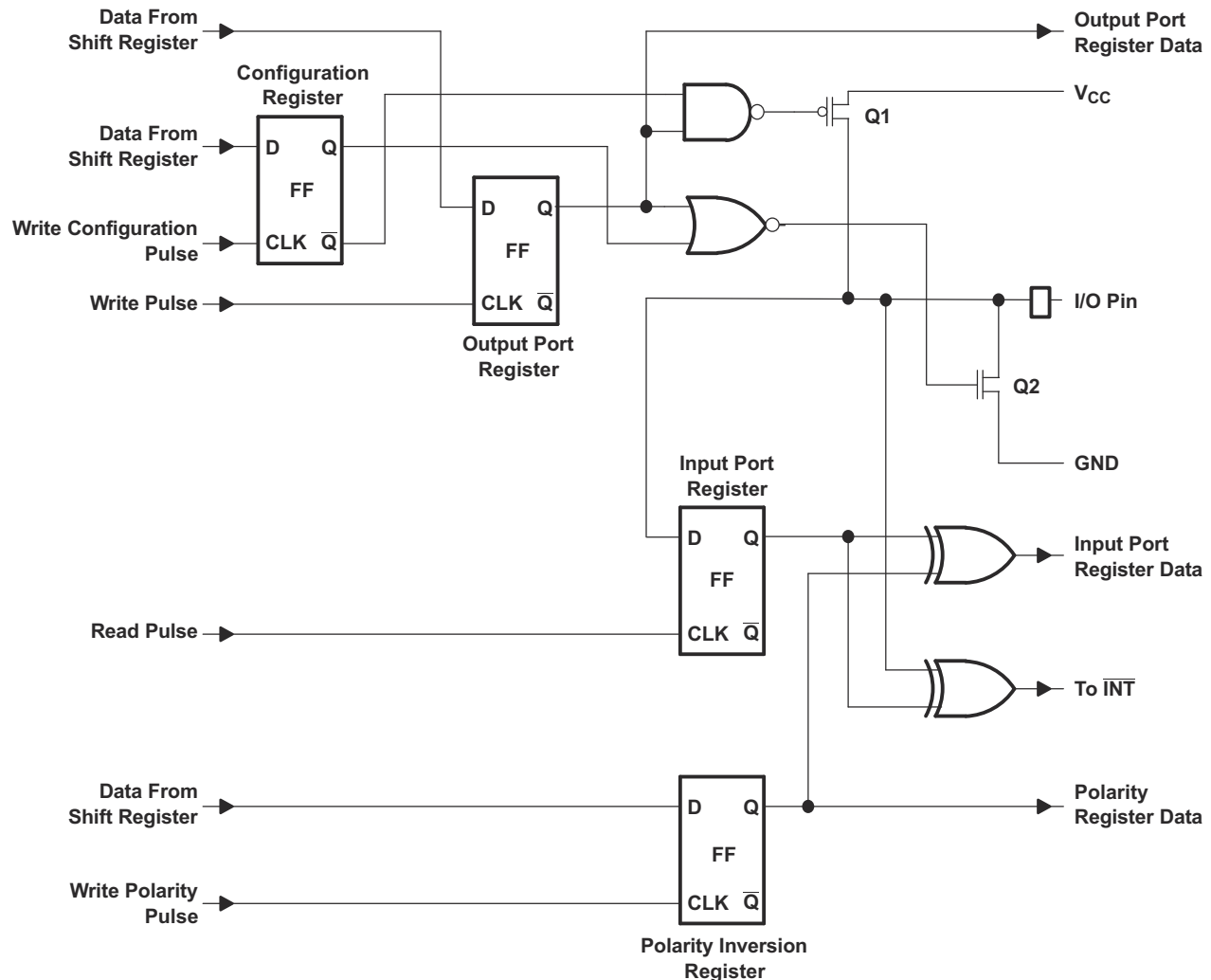
### 7.2 Functional Block Diagram



Pin numbers shown are for the PW package.

All I/Os are set to inputs at reset.

**Figure 7-1. Logic Diagram (Positive Logic)**



At power-on reset, all registers return to default values.

**Figure 7-2. Simplified Schematic of P-Port I/Os**

## 7.3 Feature Description

### 7.3.1 5-V Tolerant I/O Ports

The TCA9535 features I/O ports, which are tolerant up to 5 V. This allows the TCA9535 to be connected to a large array of devices. To minimize  $I_{CC}$ , any input signals must be designed so the input voltage stays within  $V_{IH}$  and  $V_{IL}$  of the device as described in the [Electrical Characteristics](#) section.

### 7.3.2 Hardware Address Pins

The TCA9535 features 3 hardware address pins (A0, A1, and A2). The user selects the device I<sup>2</sup>C address by pulling each pin to either  $V_{CC}$  or GND to signify the bit value in the address. This allows up to 8 TCA9535 devices to be on the same bus without address conflicts. See the [Functional Block Diagram](#) for the 3 address pins. The voltage on the pins must not change while the device is powered up in order to prevent possible I<sup>2</sup>C glitches as a result of the device address changing during a transmission. All of the pins must be tied either to  $V_{CC}$  or GND and cannot be left floating.

### 7.3.3 Interrupt ( $\overline{\text{INT}}$ ) Output

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time  $t_{iv}$ , the signal  $\overline{\text{INT}}$  is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal. Note that the  $\overline{\text{INT}}$  is reset at the ACK just before the byte of changed data is sent. Interrupts that occur during the ACK clock pulse can be lost (or be very short) because of the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as  $\overline{\text{INT}}$ .

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register. Because each 8-bit port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1, or the interrupt caused by port 1 is not cleared by a read of port 0.

$\overline{\text{INT}}$  has an open-drain structure.  $\overline{\text{INT}}$  requires a pull-up resistor to  $V_{CC}$  of moderate value (typically about 10 k $\Omega$ ).

## 7.4 Device Functional Modes

### 7.4.1 Power-On Reset (POR)

When power (from 0 V) is applied to  $V_{CC}$ , an internal power-on reset circuit holds the TCA9535 in a reset condition until  $V_{CC}$  has reached  $V_{PORR}$ . At that time, the reset condition is released. The TCA9535 registers and I<sup>2</sup>C-SMBus state machine initialize to their default states. Then,  $V_{CC}$  must be lowered to below  $V_{PORF}$  and back up to the operating voltage for a power-reset cycle.

### 7.4.2 Powered-Up

When power has been applied to  $V_{CC}$  above  $V_{PORR}$ , and the POR has taken place, the device is in a functioning mode. In this state, the device is ready to accept any incoming I<sup>2</sup>C requests and is monitoring for changes on the input ports.

## 7.5 Programming

### 7.5.1 I<sup>2</sup>C Interface

The TCA9535 has a standard bidirectional I<sup>2</sup>C interface that is controlled by a controller device in order to be configured or read the status of this device. Each target on the I<sup>2</sup>C bus has a specific device address to differentiate between other target devices that are on the same I<sup>2</sup>C bus. Many target devices require configuration upon startup to set the behavior of the device. This is typically done when the controller accesses internal register maps of the target, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read. For more information see *Understanding the I<sup>2</sup>C Bus* application report, [SLVA704](#).

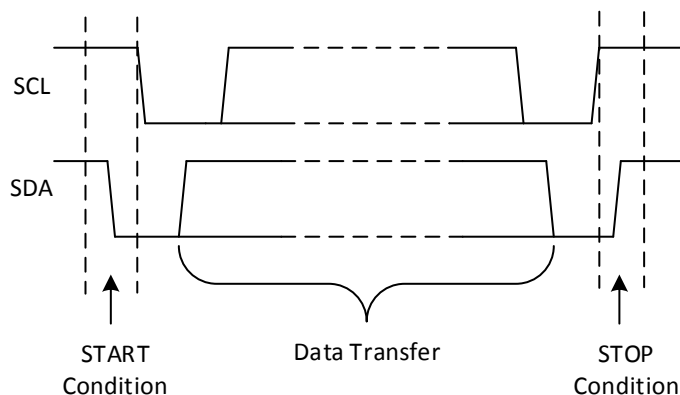
The physical I<sup>2</sup>C interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to  $V_{CC}$  through a pull-up resistor. The size of the pull-up resistor is determined by the amount of capacitance on the I<sup>2</sup>C lines. For further details, see *I<sup>2</sup>C Pull-up Resistor Calculation* application report, [SLVA689](#). Data transfer may be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition. See [Table 7-1](#).

[Figure 7-3](#) and [Figure 7-4](#) show the general procedure for a controller to access a target device:

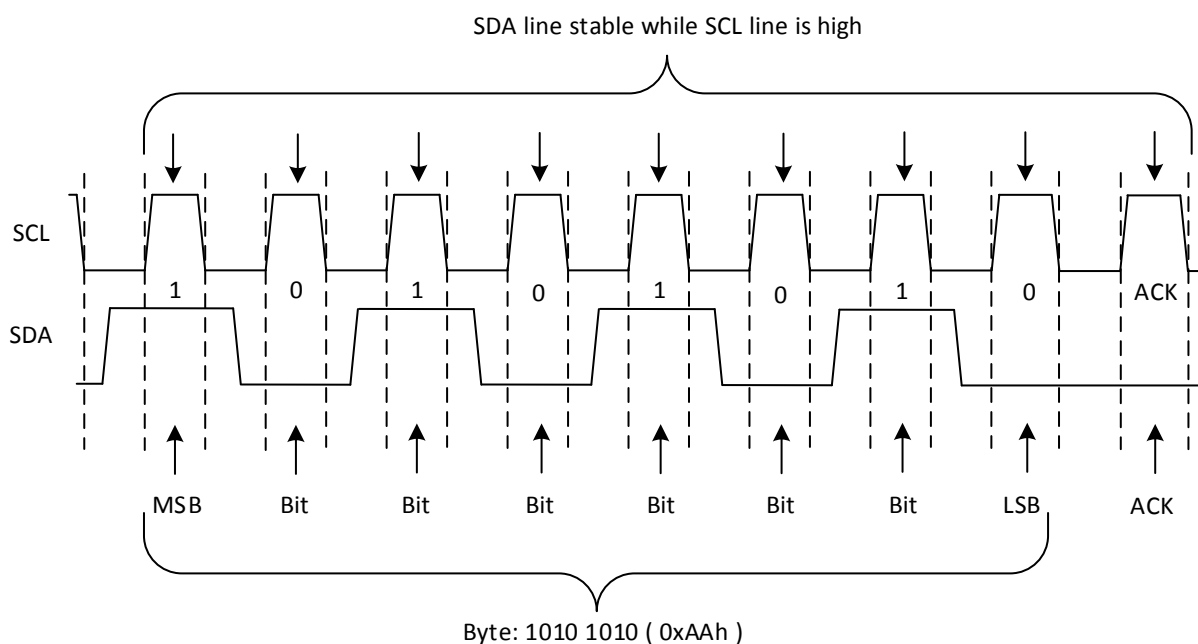
1. If a controller wants to send data to a target:
  - Controller-transmitter sends a START condition and addresses the target-receiver.
  - Controller-transmitter sends data to target-receiver.
  - Controller-transmitter terminates the transfer with a STOP condition.
2. If a controller wants to receive or read data from a target:
  - Controller-receiver sends a START condition and addresses the target-transmitter.
  - Controller-receiver sends the requested register to read to target-transmitter.
  - Controller-receiver receives data from the target-transmitter.



- Controller-receiver terminates the transfer with a STOP condition.



**Figure 7-3. Definition of Start and Stop Conditions**



**Figure 7-4. Bit Transfer**

Table 7-1 shows the interface definition.

**Table 7-1. Interface Definition**

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I <sup>2</sup> C target address	L	H	L	L	A2	A1	A0	R/ $\overline{W}$
P0x I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
P1x I/O data bus	P17	P16	P15	P14	P13	P12	P11	P10

#### 7.5.1.1 Bus Transactions

Data is exchanged between the controller and the TCA9535 through write and read commands, and this is accomplished by reading from or writing to registers in the target device.

Registers are locations in the memory of the target which contain information, whether it be the configuration information or some sampled data to send back to the controller. The controller must write information to these registers in order to instruct the target device to perform a task.

### 7.5.1.1.1 Writes

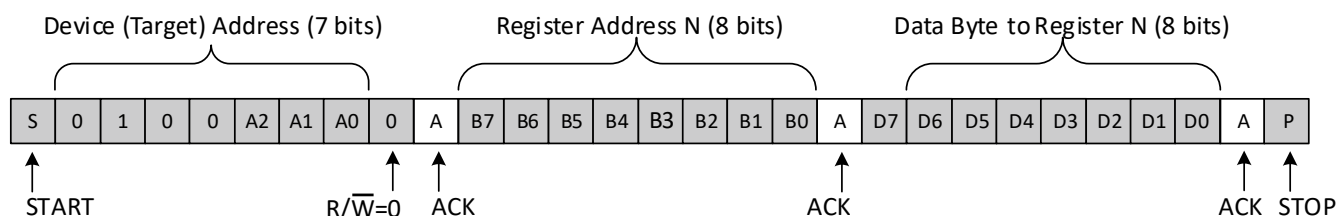
To write on the I<sup>2</sup>C bus, the controller sends a START condition on the bus with the address of the target, as well as the last bit (the R/  $\overline{W}$  bit) set to 0, which signifies a write. After the target sends the acknowledge bit, the controller then sends the register address of the register to which it wishes to write. The target acknowledges again, letting the controller know it is ready. After this, the controller starts sending the register data to the target until the controller has sent all the data necessary (which is sometimes only a single byte), and the controller terminates the transmission with a STOP condition.

See the [Control Register and Command Byte](#) section to see list of the TCA9535 internal registers and a description of each one.

Figure 7-5 shows an example of writing a single byte to a target register.

- ☒ Controller controls SDA line
- ☐ Target controls SDA line

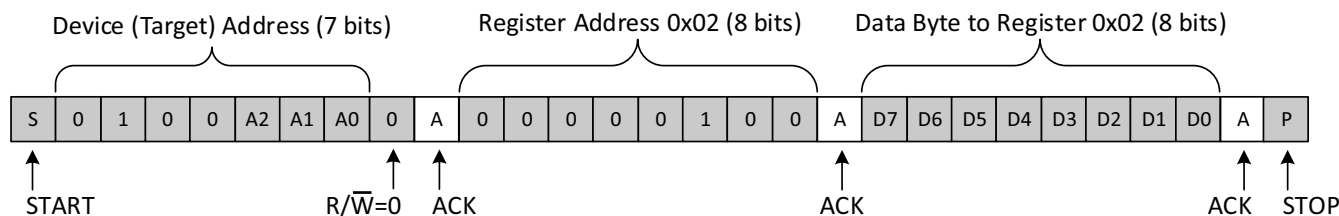
#### Write to one register in a device



**Figure 7-5. Write to Register**

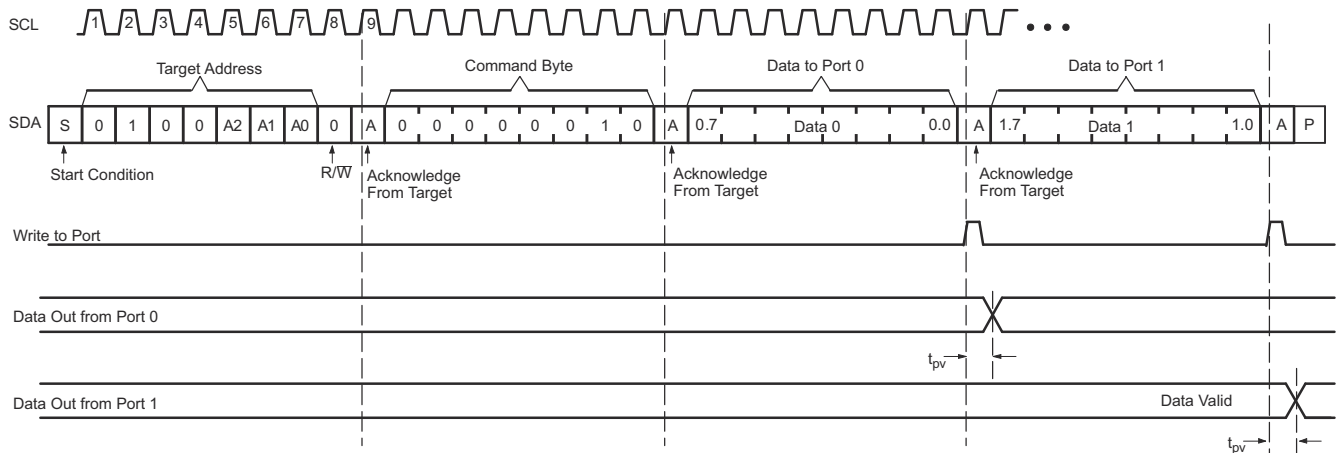
Figure 7-6 shows the Write to the Polarity Inversion Register.

- ☒ Controller controls SDA line
- ☐ Target controls SDA line



**Figure 7-6. Write to the Polarity Inversion Register**

Figure 7-7 shows the Write to Output Port Registers.



**Figure 7-7. Write to Output Port Registers**

#### 7.5.1.1.2 Reads

Reading from a target is very similar to writing, but requires some additional steps. In order to read from a target, the controller must first instruct the target which register it wishes to read from. This is done by the controller starting off the transmission in a similar fashion as the write, by sending the address with the  $R/\bar{W}$  bit equal to 0 (signifying a write), followed by the register address it wishes to read from. When the target acknowledges this register address, the controller sends a START condition again, followed by the target address with the  $R/\bar{W}$  bit set to 1 (signifying a read). This time, the target acknowledges the read request, and the controller releases the SDA bus but continues supplying the clock to the target. During this part of the transaction, the controller becomes the controller-receiver, and the target becomes the target-transmitter.

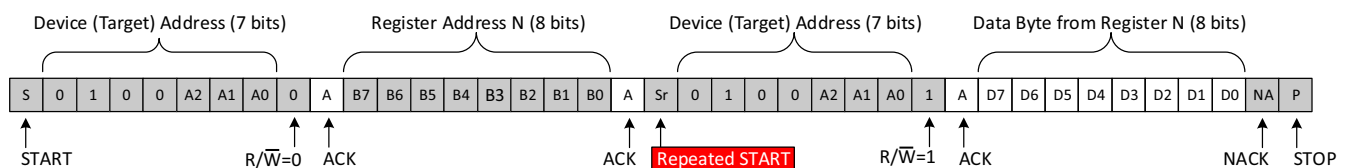
The controller continues to send out the clock pulses, but releases the SDA line so that the target can transmit data. At the end of every byte of data, the controller sends an ACK to the target, letting the target know that it is ready for more data. When the controller has received the number of bytes it is expecting, it sends a NACK, signaling to the target to halt communications and release the bus. The controller follows this up with a STOP condition.

See the [Control Register and Command Byte](#) section to see list of the TCA9535's internal registers and a description of each one.

Figure 7-8 shows an example of reading a single byte from a target register.

- ☒ Controller controls SDA line
- ☐ Target controls SDA line

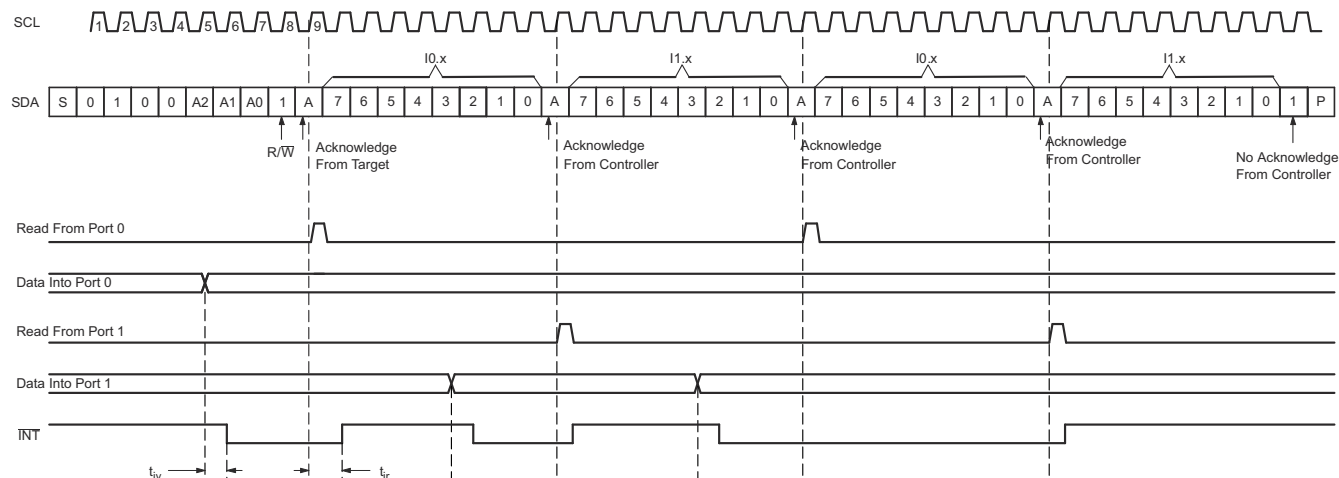
#### Read from one register in a device



**Figure 7-8. Read from Register**

After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. For example, if the command byte references Input Port 1 before the restart, and the restart occurs when Input Port 0 is being read, the stored command byte changes to reference Input Port 0. The original command byte is forgotten. If a subsequent restart occurs, Input Port 0 is read first. Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflect the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0.

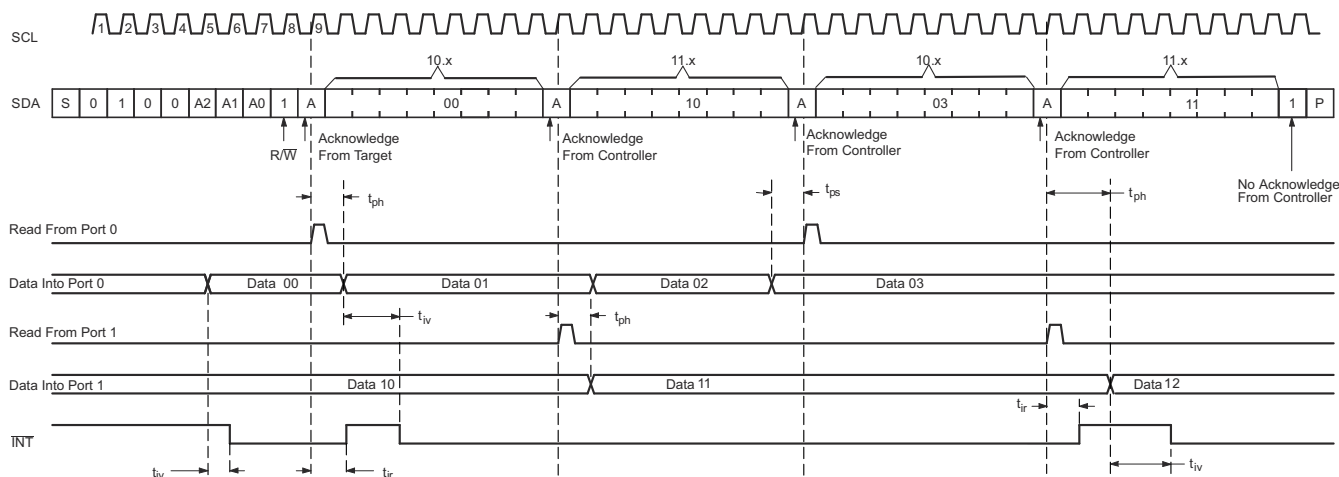
Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus controller must not acknowledge the data. [Figure 7-9](#) and [Figure 7-10](#) show two different scenarios of Read Input Port Register.



Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).

This figure eliminates the command byte transfer, a restart, and target address call between the initial target address call and actual data transfer from the P port.

**Figure 7-9. Read Input Port Register, Scenario 1**



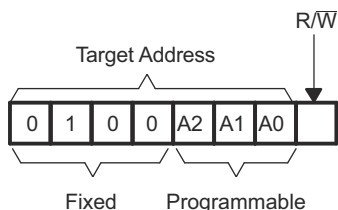
Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).

This figure eliminates the command byte transfer, a restart, and target address call between the initial target address call and actual data transfer from the P port.

**Figure 7-10. Read Input Port Register, Scenario 2**

## 7.5.2 Device Address

[Figure 7-11](#) shows the address byte of the TCA9535.



**Figure 7-11. TCA9535 Address**

Table 7-2 shows the address reference of the TCA9535.

**Table 7-2. Address Reference**

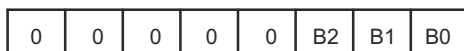
INPUTS			I <sup>2</sup> C BUS TARGET ADDRESS
A2	A1	A0	
L	L	L	32 (decimal), 0x20 (hexadecimal)
L	L	H	33 (decimal), 0x21 (hexadecimal)
L	H	L	34 (decimal), 0x22 (hexadecimal)
L	H	H	35 (decimal), 0x23 (hexadecimal)
H	L	L	36 (decimal), 0x24 (hexadecimal)
H	L	H	37 (decimal), 0x25 (hexadecimal)
H	H	L	38 (decimal), 0x26 (hexadecimal)
H	H	H	39 (decimal), 0x27 (hexadecimal)

The last bit of the target address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

### 7.5.3 Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus controller sends a command byte shown in Table 7-3 that is stored in the control register in the TCA9535. Three bits of this data byte state the operation (read or write) and the internal register (input, output, polarity inversion, or configuration) that is affected. This register can be written or read through the I<sup>2</sup>C bus. The command byte is sent only during a write transmission.

When a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent. Figure 7-12 shows the control register bits.



**Figure 7-12. Control Register Bits**

**Table 7-3. Command Byte**

CONTROL REGISTER BITS			COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B2	B1	B0				
0	0	0	0x00	Input Port 0	Read byte	xxxx xxxx
0	0	1	0x01	Input Port 1	Read byte	xxxx xxxx
0	1	0	0x02	Output Port 0	Read-write byte	1111 1111
0	1	1	0x03	Output Port 1	Read-write byte	1111 1111
1	0	0	0x04	Polarity Inversion Port 0	Read-write byte	0000 0000
1	0	1	0x05	Polarity Inversion Port 1	Read-write byte	0000 0000
1	1	0	0x06	Configuration Port 0	Read-write byte	1111 1111
1	1	1	0x07	Configuration Port 1	Read-write byte	1111 1111

## 7.6 Register Maps

### 7.6.1 Register Descriptions

The Input Port registers (registers 0 and 1) shown in [Table 7-4](#) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration Register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to let the I<sup>2</sup>C device know that the Input Port registers are accessed next.

**Table 7-4. Registers 0 and 1 (Input Port Registers)**

Bit	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X
Bit	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

The Output Port registers (registers 2 and 3) shown in [Table 7-5](#) show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

**Table 7-5. Registers 2 and 3 (Output Port Registers)**

Bit	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1
Bit	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

The Polarity Inversion registers (registers 4 and 5) shown in [Table 7-6](#) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding pin's original polarity is retained.

**Table 7-6. Registers 4 and 5 (Polarity Inversion Registers)**

Bit	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0
Bit	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

The Configuration registers (registers 6 and 7) shown in [Table 7-7](#) configure the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

**Table 7-7. Registers 6 and 7 (Configuration Registers)**

Bit	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1
Bit	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

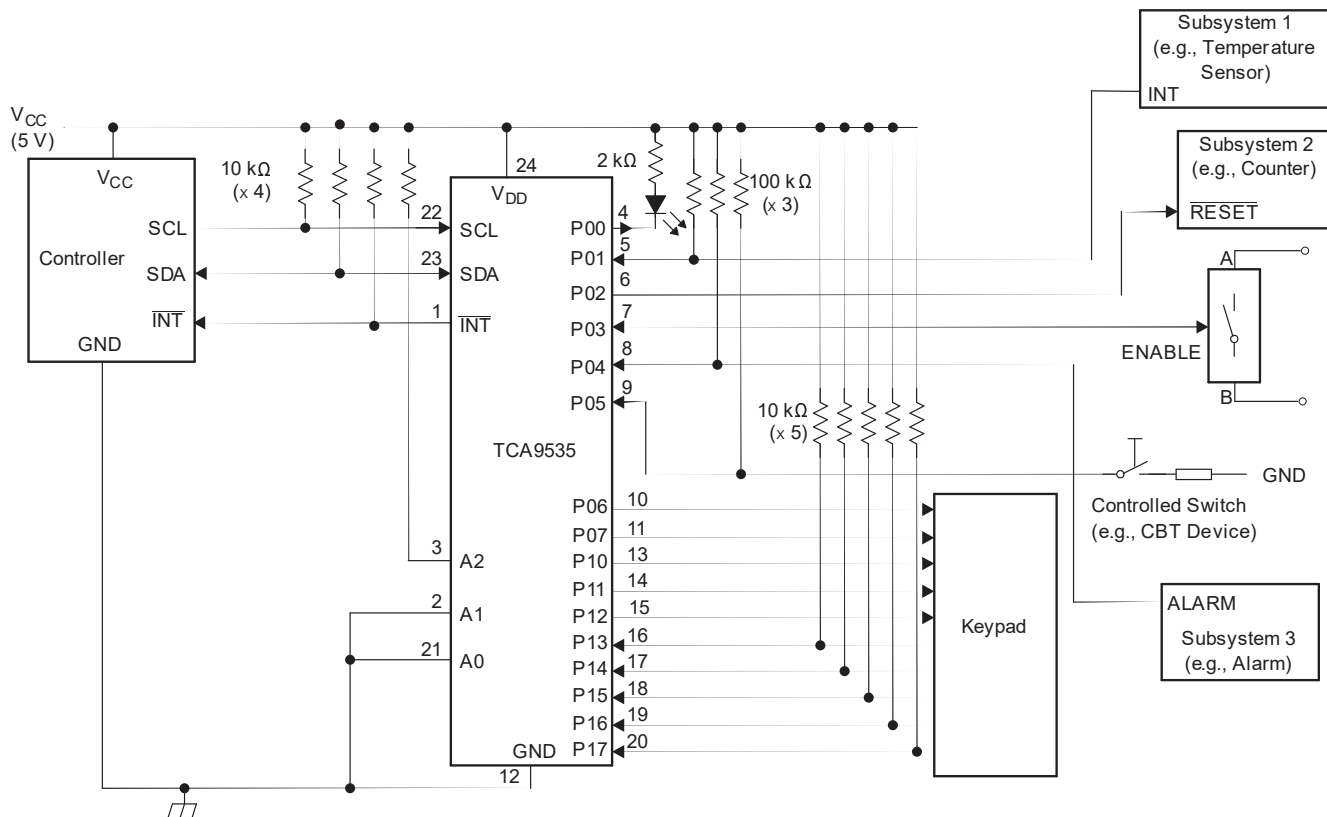
### 8.1 Application Information

Applications of the TCA9535 has the device connected as a target to an I<sup>2</sup>C controller (processor), and the I<sup>2</sup>C bus may contain any number of other target devices. The TCA9535 is typically in a remote location from the controller, placed close to the GPIOs to which the controller needs to monitor or control.

IO Expanders such as the TCA9535 are typically used for controlling LEDs (for feedback or status lights), controlling enable or reset signals of other devices, and even reading the outputs of other devices or buttons.

### 8.2 Typical Application

Figure 8-1 shows an application in which the TCA9535 can be used.



Device address is configured as 0100100 for this example.

P00, P02, and P03 are configured as outputs.

P01, P04–P07, and P10–P17 are configured as inputs.

Pin numbers shown are for the PW package.

**Figure 8-1. Application Schematic**

#### 8.2.1 Design Requirements

The designer must take into consideration the system, to be sure not to violate any of the parameters. Table 8-1 shows some key parameters which must not be violated.

**Table 8-1. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
I <sup>2</sup> C and Subsystem Voltage (V <sub>CC</sub> )	5 V
Output current rating, P-port sinking (I <sub>OL</sub> )	25 mA
I <sup>2</sup> C bus clock (SCL) speed	400 kHz

**8.2.1.1 Calculating Junction Temperature and Power Dissipation**

When designing with this device, it is important that the [Recommended Operating Conditions](#) not be violated. Many of the parameters of this device are rated based on junction temperature. So junction temperature must be calculated in order to verify that safe operation of the device is met. The basic equation for junction temperature is shown in [Equation 1](#).

$$T_J = T_A + (\theta_{JA} \times P_d) \quad (1)$$

$\theta_{JA}$  is the standard junction to ambient thermal resistance measurement of the package, as seen in [Thermal Information](#) table.  $P_d$  is the total power dissipation of the device, and the approximation is shown in [Equation 2](#).

$$P_d \approx (I_{CC\_STATIC} \times V_{CC}) + \sum P_{d\_PORT\_L} + \sum P_{d\_PORT\_H} \quad (2)$$

[Equation 2](#) is the approximation of power dissipation in the device. The equation is the static power plus the summation of power dissipated by each port (with a different equation based on if the port is outputting high, or outputting low. If the port is set as an input, then power dissipation is the input leakage of the pin multiplied by the voltage on the pin). Note that this ignores power dissipation in the  $\overline{INT}$  and SDA pins, assuming these transients to be small. They can easily be included in the power dissipation calculation by using [Equation 3](#) to calculate the power dissipation in  $\overline{INT}$  or SDA while they are pulling low, and this gives maximum power dissipation.

$$P_{d\_PORT\_L} = (I_{OL} \times V_{OL}) \quad (3)$$

[Equation 3](#) shows the power dissipation for a single port which is set to output low. The power dissipated by the port is the  $V_{OL}$  of the port multiplied by the current it is sinking.

$$P_{d\_PORT\_H} = (I_{OH} \times (V_{CC} - V_{OH})) \quad (4)$$

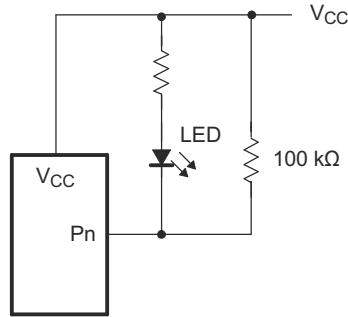
[Equation 4](#) shows the power dissipation for a single port which is set to output high. The power dissipated by the port is the current sourced by the port multiplied by the voltage drop across the device (difference between  $V_{CC}$  and the output voltage).

**8.2.1.2 Minimizing I<sub>CC</sub> When I/O is Used to Control LED**

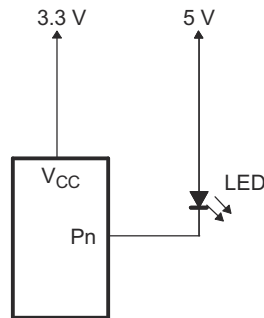
When an I/O is used to control an LED, normally it is connected to  $V_{CC}$  through a resistor as shown in [Figure 8-1](#). Because the LED acts as a diode, when the LED is off, the I/O  $V_{IN}$  is about 1.2 V less than  $V_{CC}$ . The  $\Delta I_{CC}$  parameter in the [Electrical Characteristics](#) table shows how  $I_{CC}$  increases as  $V_{IN}$  becomes lower than  $V_{CC}$ . For battery-powered applications, it is essential that the voltage of I/O pins is greater than or equal to  $V_{CC}$  when the LED is off to minimize current consumption.

[Figure 8-2](#) shows a high-value resistor in parallel with the LED. [Figure 8-3](#) shows  $V_{CC}$  less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O  $V_{IN}$  at or above  $V_{CC}$  and prevent additional supply current consumption when the LED is off.





**Figure 8-2. High-Value Resistor in Parallel With LED**



**Figure 8-3. Device Supplied by Lower Voltage**

### 8.2.2 Detailed Design Procedure

The pull-up resistors,  $R_P$ , for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all targets on the I<sup>2</sup>C bus. The minimum pull-up resistance is a function of  $V_{CC}$ ,  $V_{OL(max)}$ , and  $I_{OL}$  as shown in [Equation 5](#).

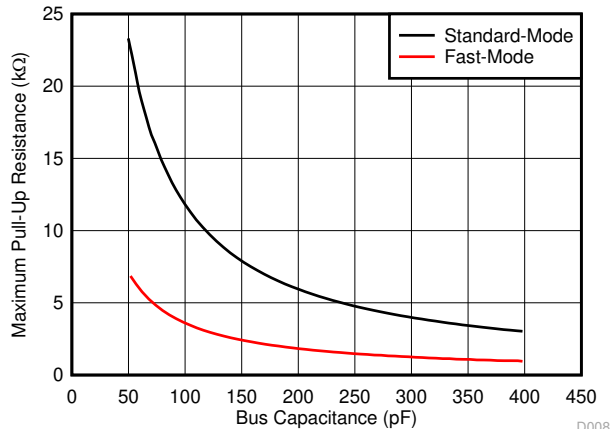
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (5)$$

The maximum pull-up resistance is a function of the maximum rise time,  $t_r$  (300 ns for fast-mode operation,  $f_{SCL} = 400$  kHz) and bus capacitance,  $C_b$  as shown in [Equation 6](#).

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (6)$$

The maximum bus capacitance for an I<sup>2</sup>C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9535,  $C_i$  for SCL or  $C_{IO}$  for SDA, the capacitance of wires/connections/traces, and the capacitance of additional targets on the bus. For further details, refer to *I<sup>2</sup>C Pull-up Resistor Calculation* application report, [SLVA689](#).

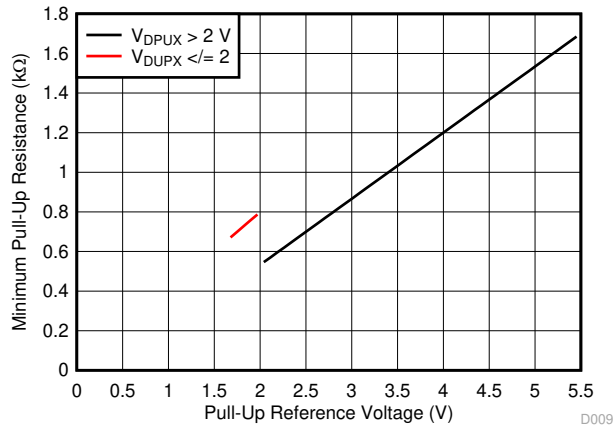
### 8.2.3 Application Curves



Standard-mode:  $f_{SCL} = 100 \text{ kHz}$ ,  $t_r = 1 \mu\text{s}$

Fast-mode:  $f_{SCL} = 400 \text{ kHz}$ ,  $t_r = 300 \text{ ns}$

**Figure 8-4. Maximum Pull-Up Resistance ( $R_{p(max)}$ ) vs Bus Capacitance ( $C_b$ )**



$V_{OL} = 0.2 \times V_{CC}$ ,  $I_{OL} = 2 \text{ mA}$  when  $V_{CC} \leq 2 \text{ V}$

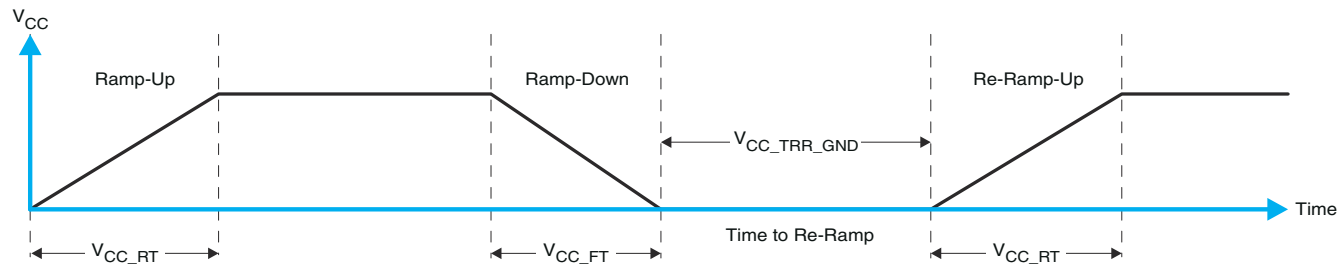
$V_{OL} = 0.4 \text{ V}$ ,  $I_{OL} = 3 \text{ mA}$  when  $V_{CC} > 2 \text{ V}$

**Figure 8-5. Minimum Pull-Up Resistance ( $R_{p(min)}$ ) vs Pull-Up Reference Voltage ( $V_{CC}$ )**

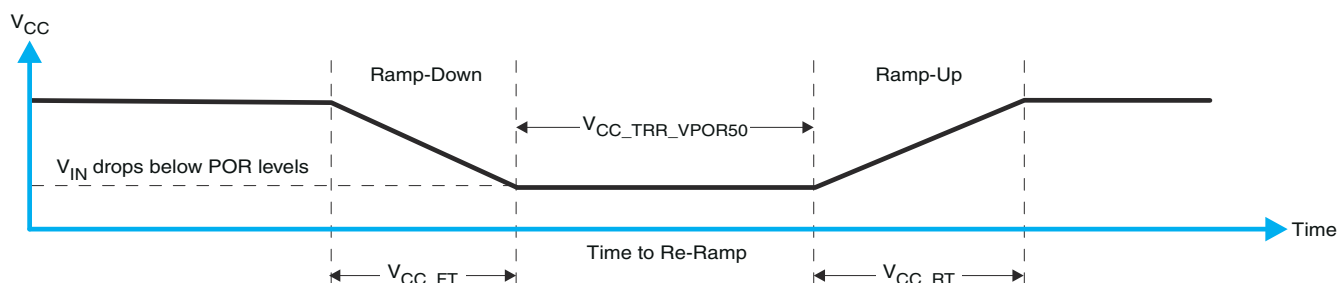
## 9 Power Supply Recommendations

In the event of a glitch or data corruption, TCA9535 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in [Figure 9-1](#) and [Figure 9-2](#).



**Figure 9-1.  $V_{CC}$  Is Lowered Below 0.2 V Or 0 V And Then Ramped Up To  $V_{CC}$**



**Figure 9-2.  $V_{CC}$  Is Lowered Below The Por Threshold, Then Ramped Back Up To  $V_{CC}$**

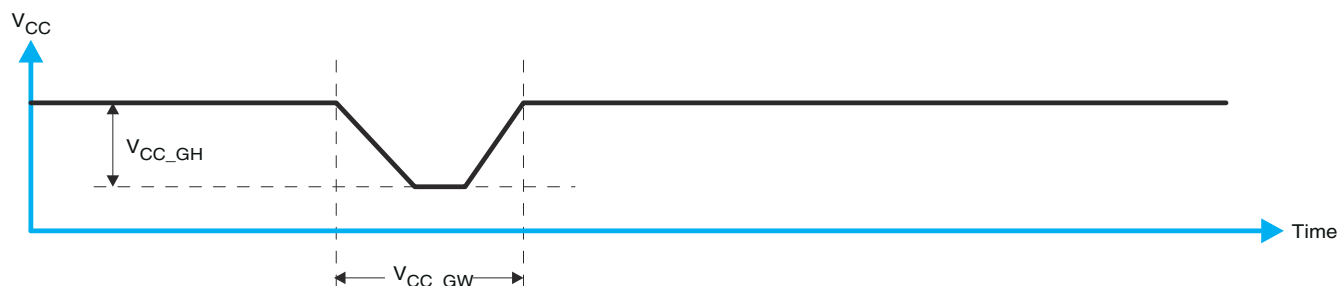
[Table 9-1](#) specifies the performance of the power-on reset feature for TCA9535 for both types of power-on reset.

**Table 9-1. Recommended Supply Sequencing And Ramp Rates**

PARAMETER <sup>(1)</sup>			MIN	TYP	MAX	UNIT
$V_{CC\_FT}$	Fall rate	See <a href="#">Figure 9-1</a>	0.1			ms
$V_{CC\_RT}$	Rise rate	See <a href="#">Figure 9-1</a>	0.01			ms
$V_{CC\_TRR}$	Time to re-ramp (when $V_{CC}$ drops to $V_{VOR\_MIN} - 50$ mV or when $V_{CC}$ drops to GND)	See <a href="#">Figure 9-1</a>	1			$\mu$ s
$V_{CC\_GH}$	The level (referenced to $V_{CC}$ ) that $V_{CC}$ can glitch down to, but not cause a functional disruption when $V_{CC\_GW}$	See <a href="#">Figure 9-3</a>			1.2	V
$V_{CC\_MV}$	The minimum voltage that $V_{CC}$ can glitch down to without causing a reset ( $V_{CC\_GH}$ must not be violated)	See <a href="#">Figure 9-3</a>	1.5			V
$V_{CC\_GW}$	Glitch width that will not cause a functional disruption	See <a href="#">Figure 9-3</a>			10	$\mu$ s
$V_{PORF}$	Voltage trip point of POR on falling $V_{CC}$		0.75	1	1	V
$V_{PORR}$	Voltage trip point of POR on rising $V_{CC}$			1.2	1.5	V

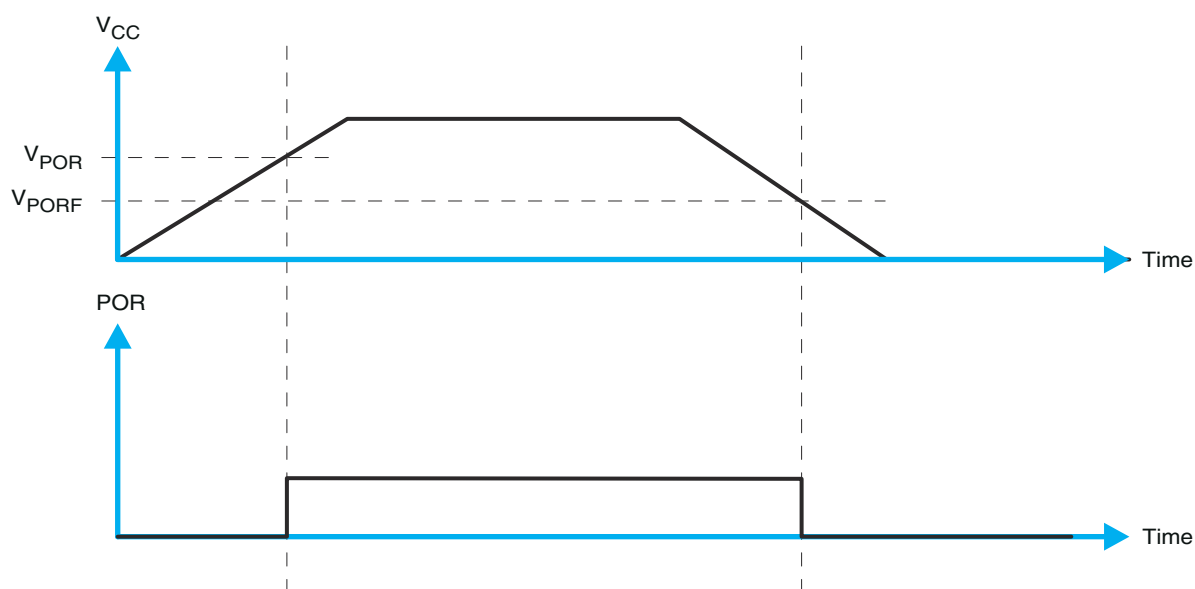
(1)  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ( $V_{CC\_GW}$ ) and height ( $V_{CC\_GH}$ ) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. [Figure 9-3](#) and [Table 9-1](#) provide more information on how to measure these specifications.



**Figure 9-3. Glitch Width And Glitch Height**

$V_{PORR}$  is critical to the power-on reset.  $V_{PORR}$  is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C/SMBus state machine are initialized to their default states. The value of  $V_{POR}$  differs based on the  $V_{CC}$  being lowered to or from 0. [Figure 9-4](#) and [Table 9-1](#) provide more details on this specification.



**Figure 9-4.  $V_{POR}$**

## 10 Layout

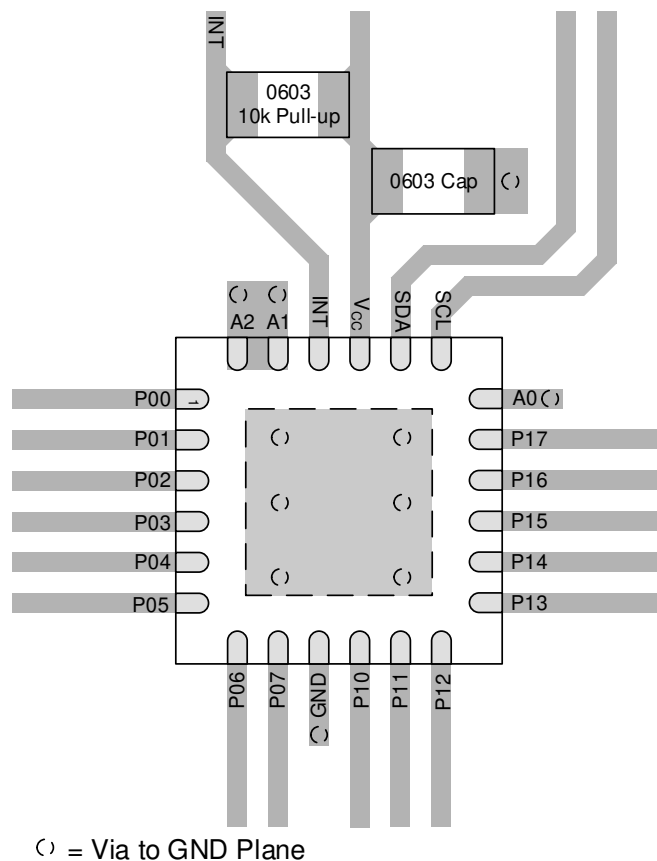
### 10.1 Layout Guidelines

For printed circuit board (PCB) layout of the TCA9535, common PCB layout practice must be followed, but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I<sup>2</sup>C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the V<sub>CC</sub> pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors must be placed as close to the TCA9535 as possible. These best practices are shown in the [Layout Example](#).

For the layout example provided in the [Layout Example](#), it must be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (V<sub>CC</sub>) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to V<sub>CC</sub>, or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in the [Layout Example](#).

### 10.2 Layout Example



**Figure 10-1. TCA9535 Layout Example**

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

- *I2C Bus Pull-Up Resistor Calculation*, [SLVA689](#)
- *Maximum Clock Frequency of I2C Bus Using Repeaters*, [SLVA695](#)
- *Introduction to Logic*, [SLVA700](#)
- *Understanding the I2C Bus*, [SLVA704](#)
- *IO Expander EVM User's Guide*, [SLVUA59A](#)

#### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 11.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

#### 11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

#### 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9535DBR	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TD9535	<a href="#">Samples</a>
TCA9535DBT	ACTIVE	SSOP	DB	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TD9535	<a href="#">Samples</a>
TCA9535MRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TD9535	<a href="#">Samples</a>
TCA9535PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW535	<a href="#">Samples</a>
TCA9535RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TD9535	<a href="#">Samples</a>
TCA9535RTWR	ACTIVE	WQFN	RTW	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PW535	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9535DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
TCA9535DBT	SSOP	DB	24	250	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
TCA9535MRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TCA9535PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TCA9535RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TCA9535RTWR	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

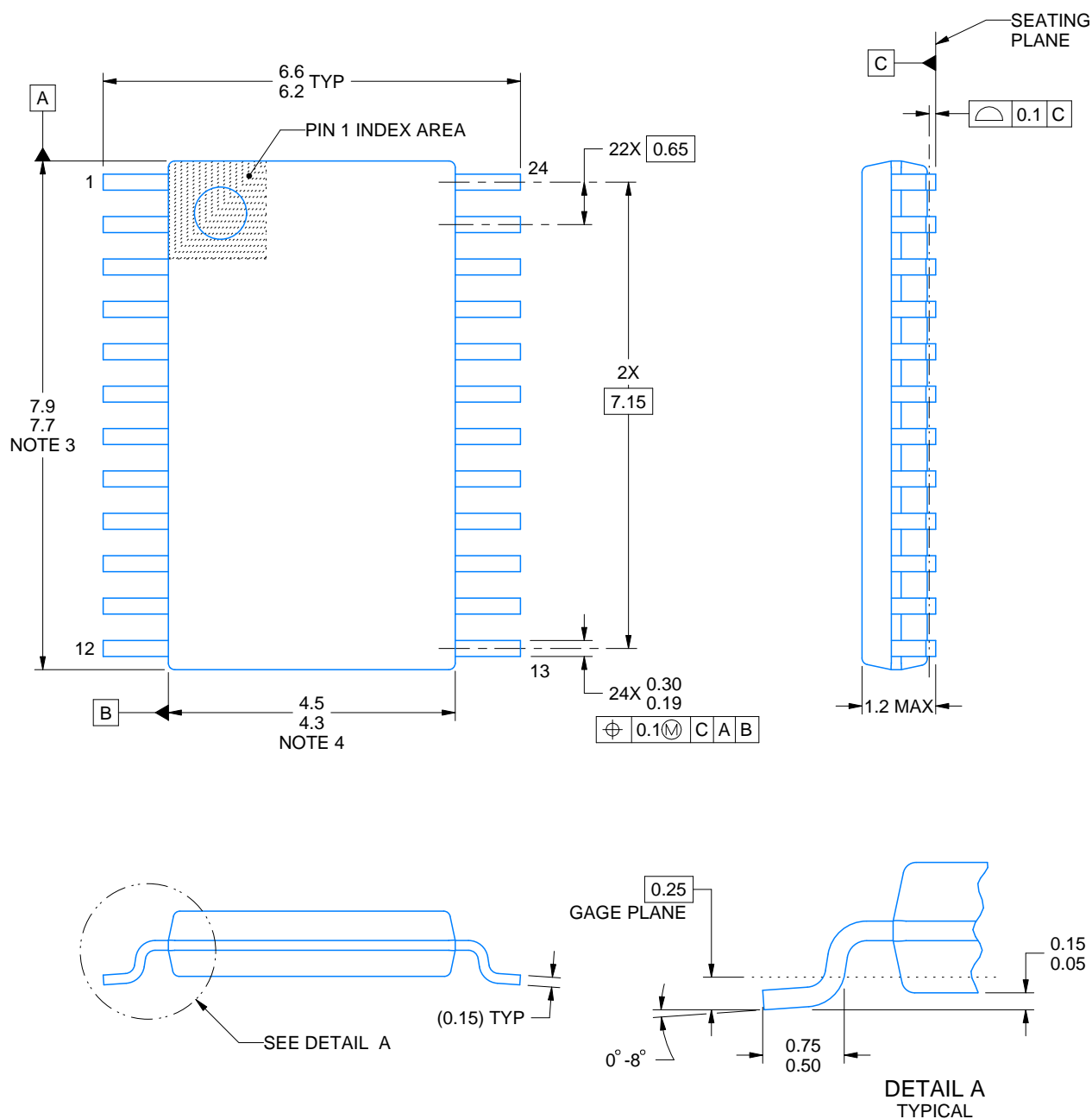
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9535DBR	SSOP	DB	24	2000	356.0	356.0	35.0
TCA9535DBT	SSOP	DB	24	250	356.0	356.0	35.0
TCA9535MRGER	VQFN	RGE	24	3000	346.0	346.0	33.0
TCA9535PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
TCA9535RGER	VQFN	RGE	24	3000	346.0	346.0	33.0
TCA9535RTWR	WQFN	RTW	24	3000	356.0	356.0	35.0



## PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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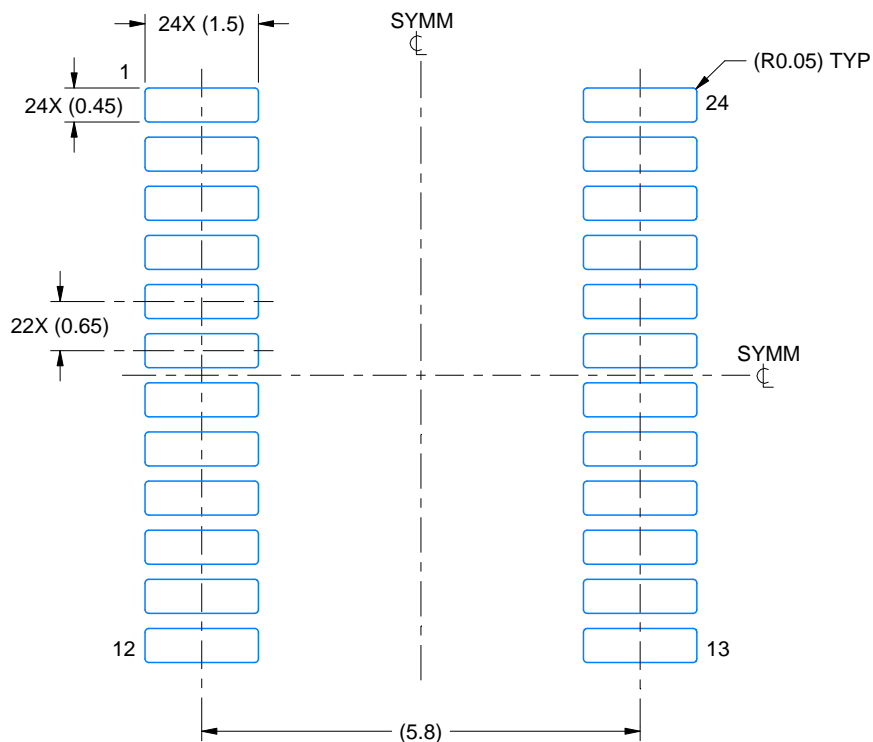
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

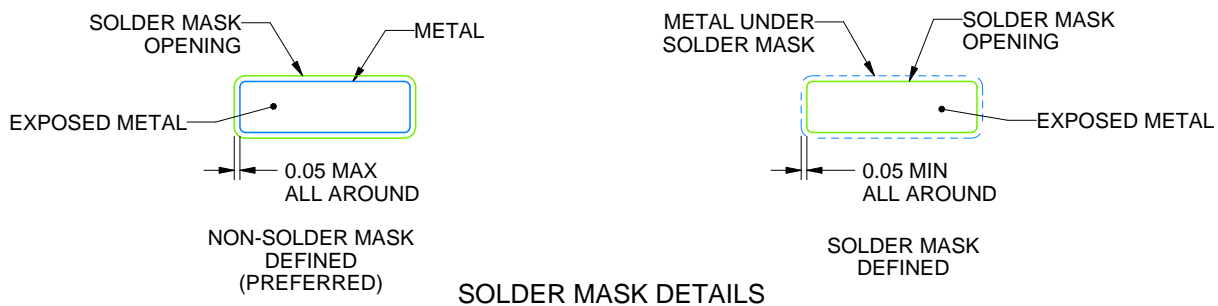
**PW0024A**

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

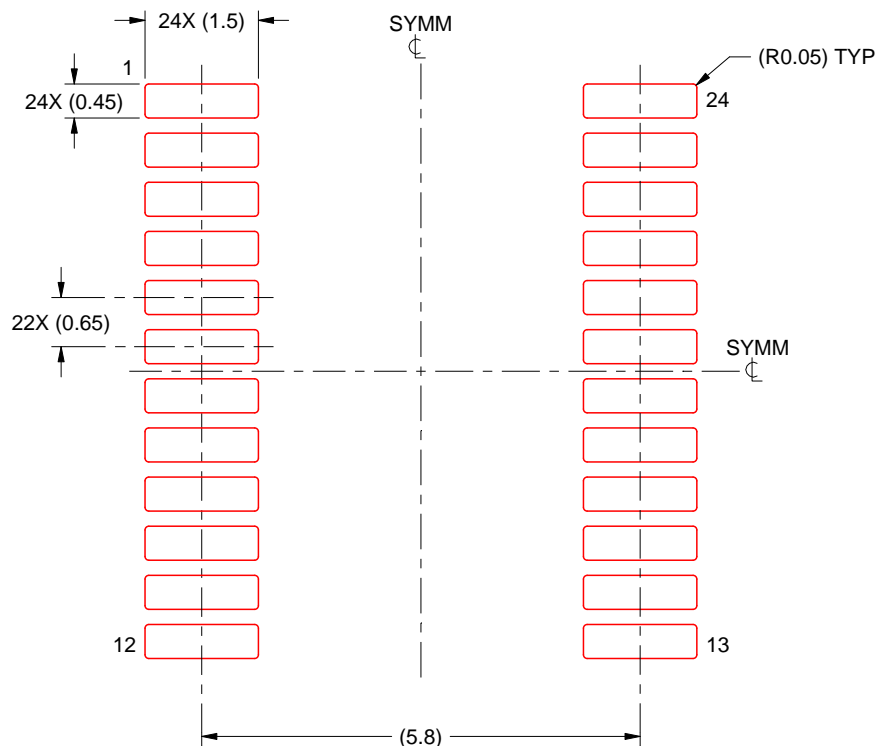
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

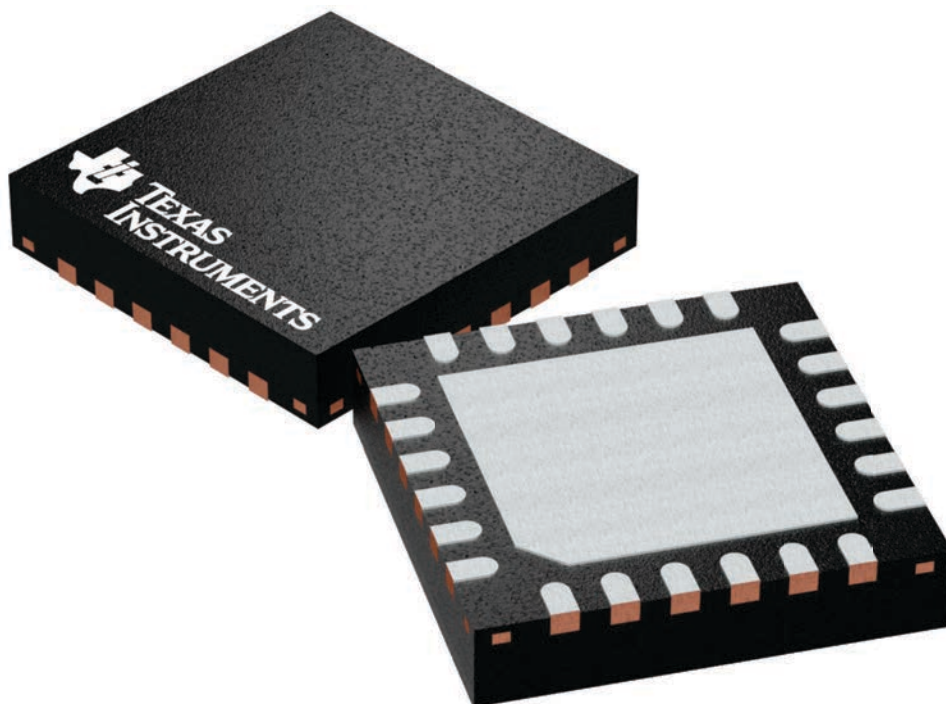
**RTW 24**

**WQFN - 0.8 mm max height**

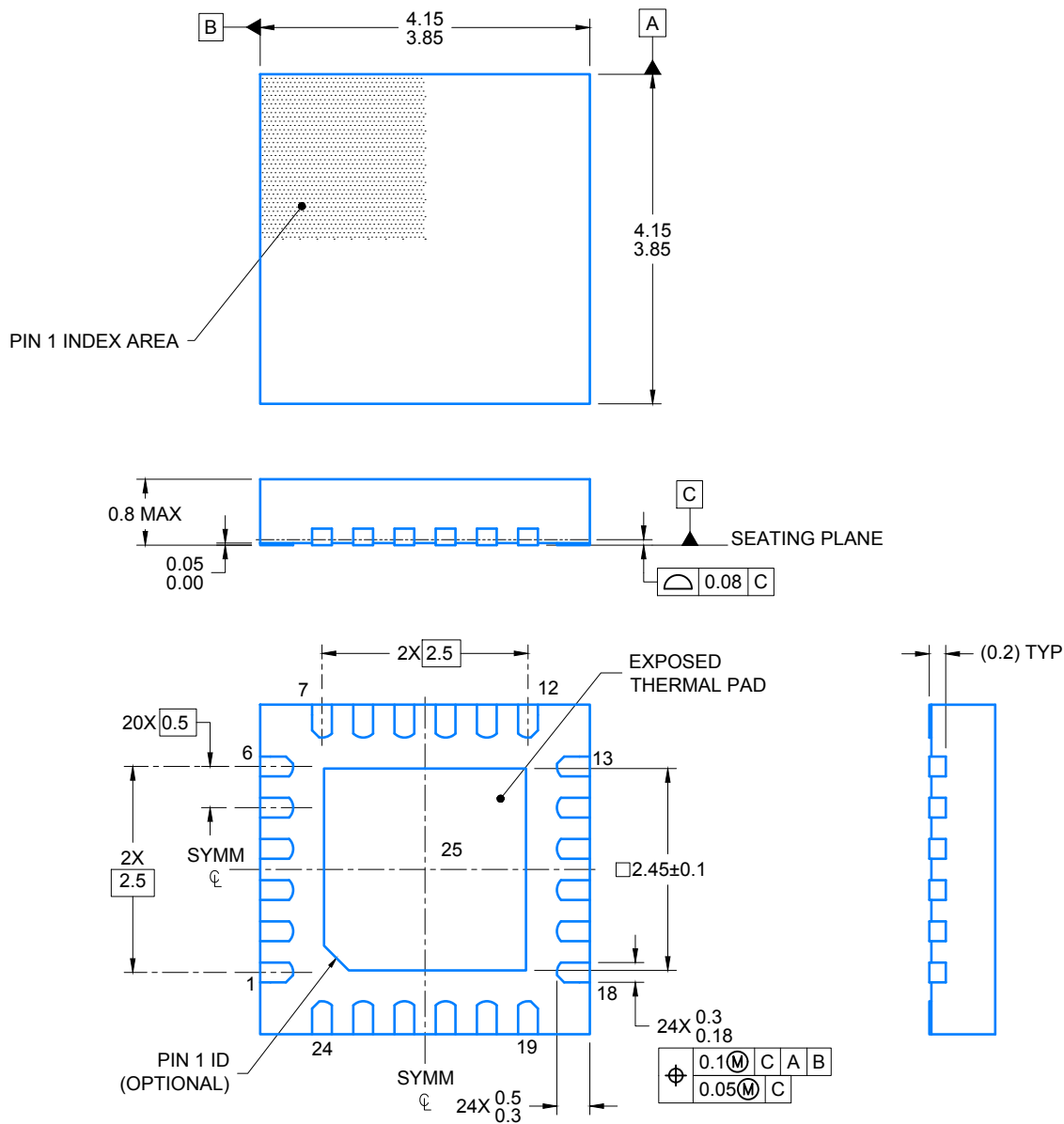
4 x 4, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224801/A



4219135/B 11/2016

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

**WQFN - 0.8 mm max height**

24X (0.6)

24X (0.24)

SYM

20X (0.5)

(R0.05) TYP

(Ø0.2) TYP VIA

2.45

3.8

13

1

6

7

12

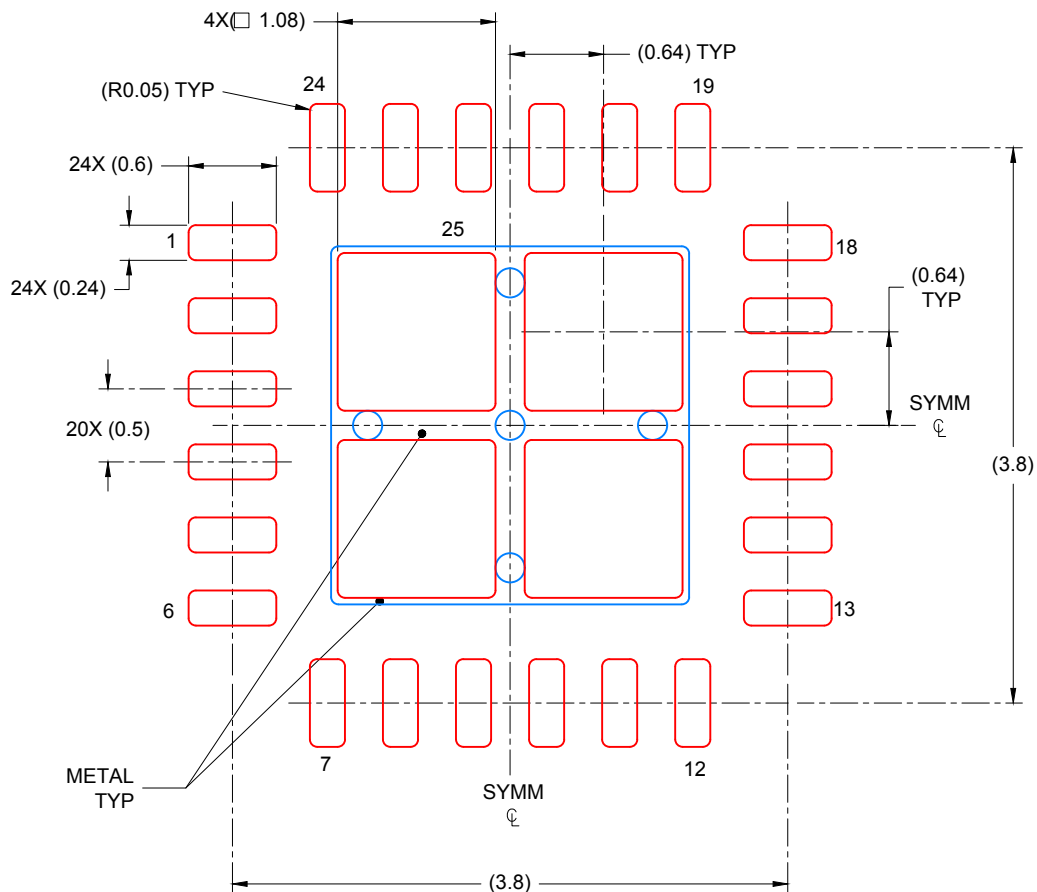
18

25

4219135/B 11/2016

3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sl原因271](http://www.ti.com/lit/sl原因271)).





SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:  
 78% PRINTED COVERAGE BY AREA UNDER PACKAGE  
 SCALE: 20X

4219135/B 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



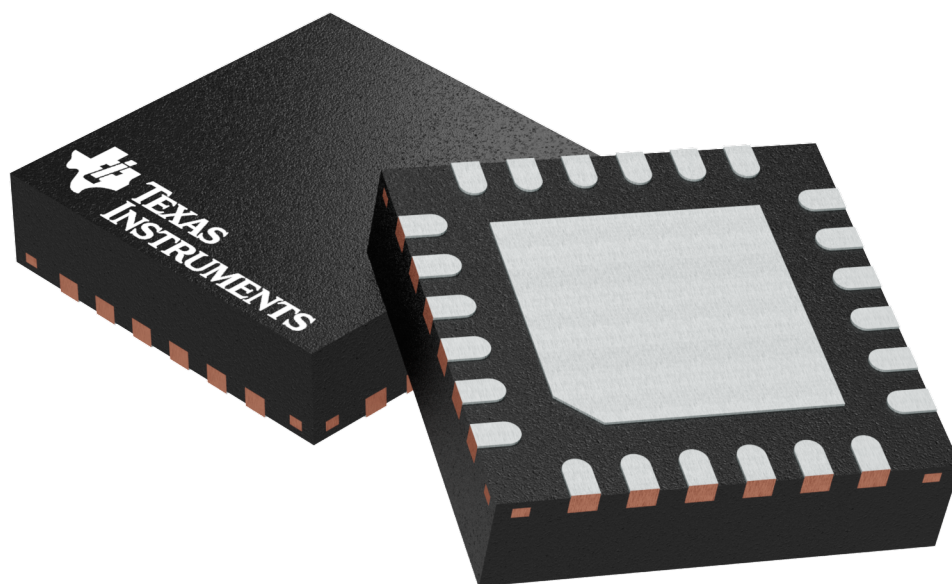
- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

**RGE 24**

**GENERIC PACKAGE VIEW**

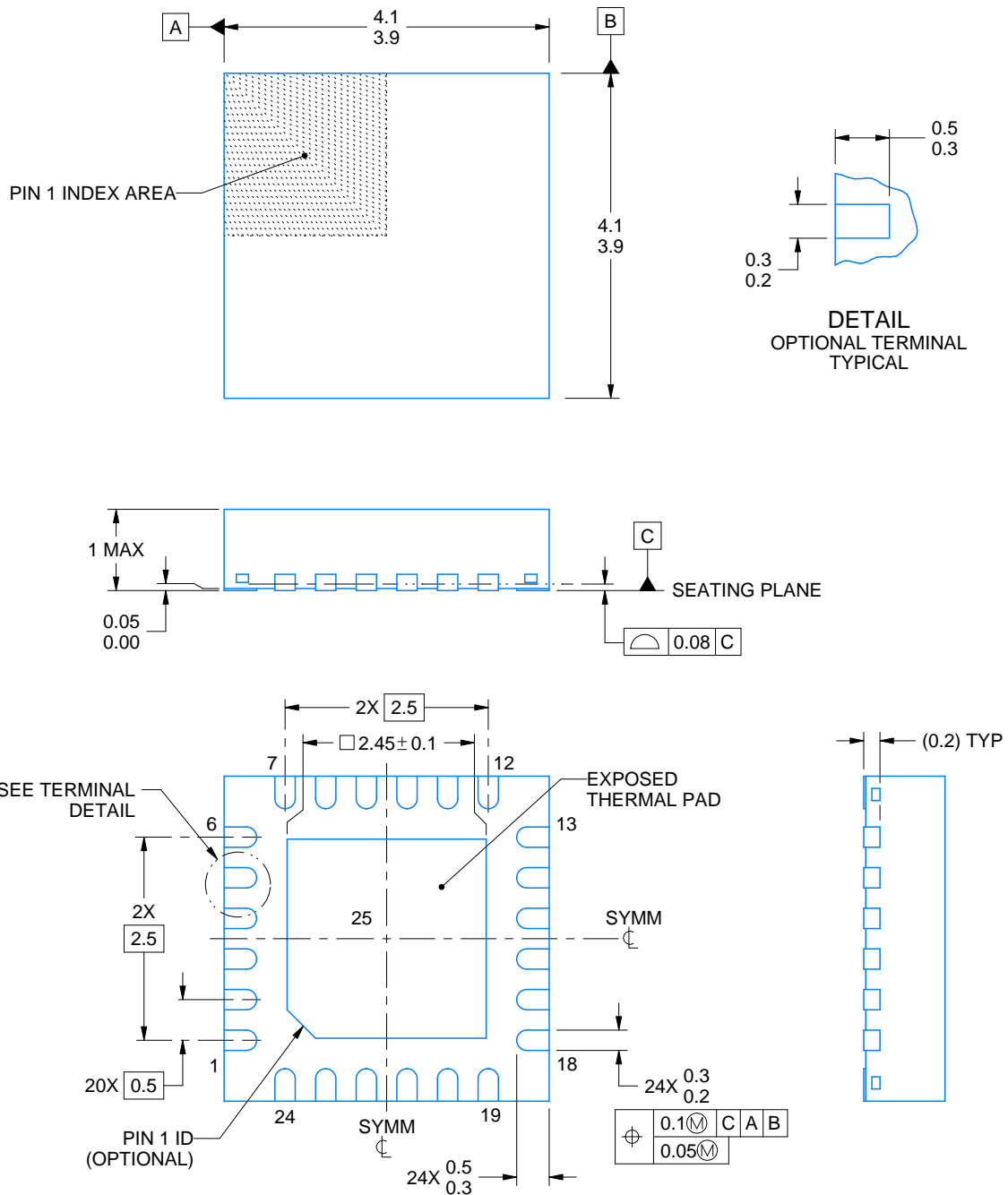
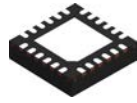
**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204104/H



4219013/A 05/2017

## NOTES:

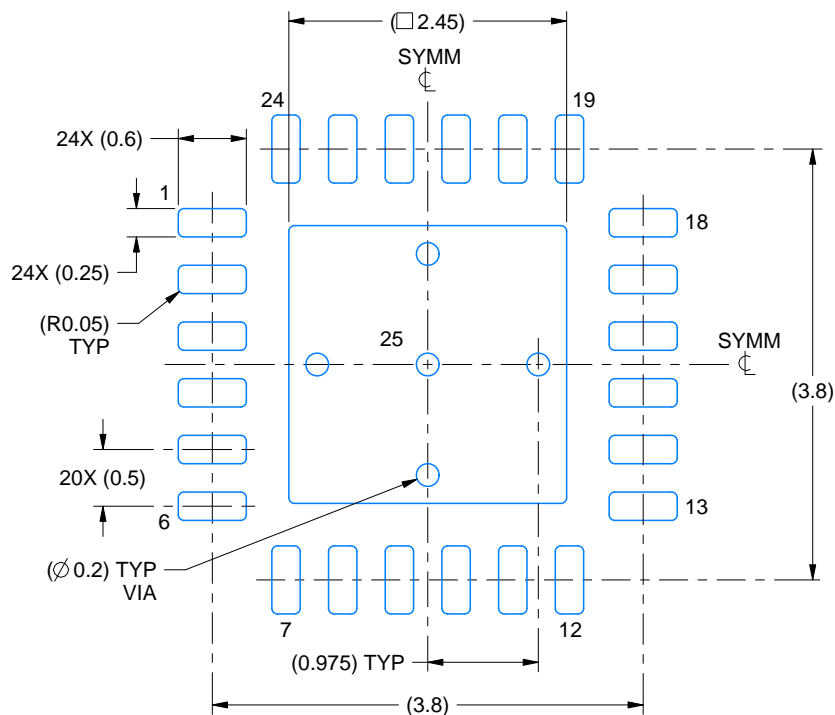
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

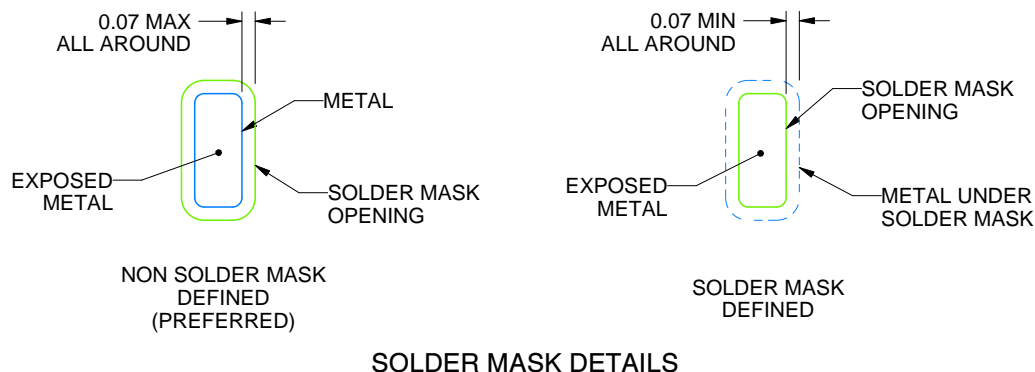
RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

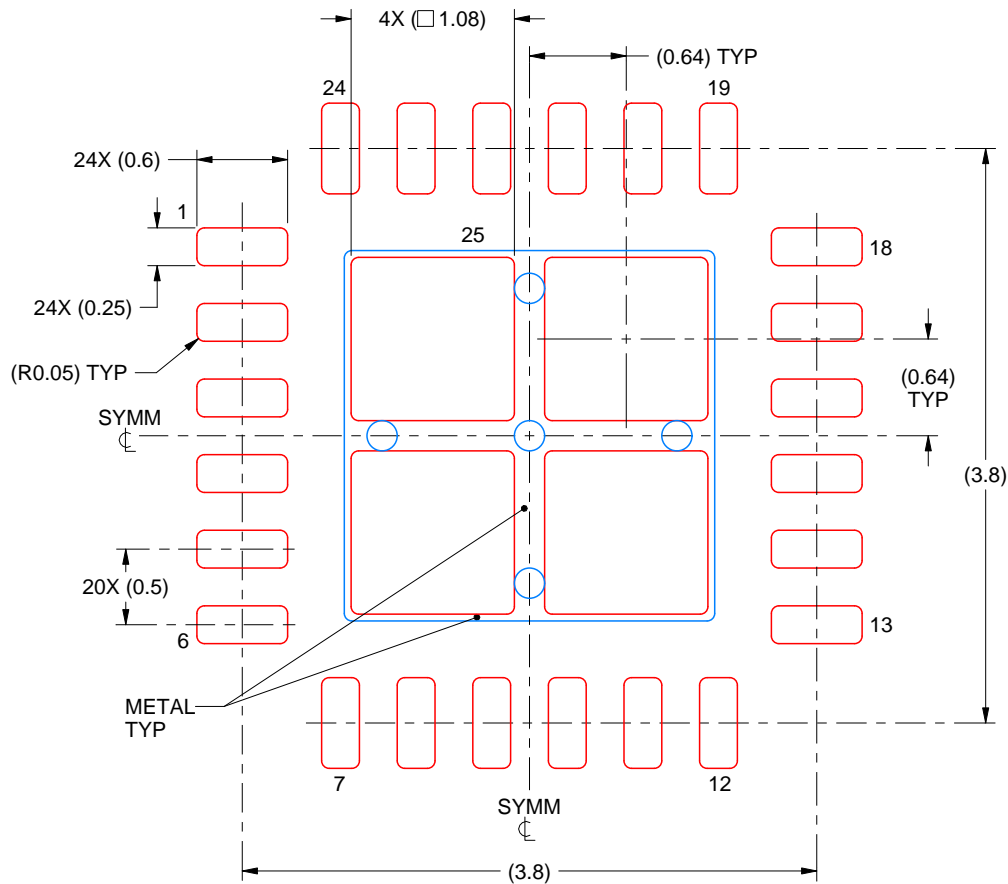
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25  
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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