AIMM: Artificially Intelligent Memory Mapping in Near-Memory Processing System

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***Abstract*—The resurgence of near-memory processing (NMP) with the advent of big data has shifted the computation paradigm from processor-centric to memory-centric computing. To meet the bandwidth and capacity demands of memory-centric computing, 3D memory has been adopted to form a scalable memory-cube network. Along with NMP and memory system development, the mapping for placing data and guiding computation in the memory-cube network has become crucial in driving the performance improvement in NMP. However, it is very challenging to design a universal optimal mapping for all applications due to unique application behavior and intractable decision space.**

In this paper, we propose an artificially intelligent memory mapping scheme, AIMM, that optimizes data placement and resource utilization through page and computation remapping. Our proposed technique involves continuous evaluation and learning of the impact of mapping decisions on system performance for any workload. AIMM uses a neural network to achieve a near-optimal mapping during execution, trained using a reinforcement learning algorithm that is known to be effective for exploring a vast design space. We also provide a detailed AIMM hardware design that can be adopted as a plugin module for various NMP systems. Our experimental evaluation shows that AIMM improves the baseline NMP performance in single and multiple program scenarios up to 55% and 50%, respectively.

I. Introduction

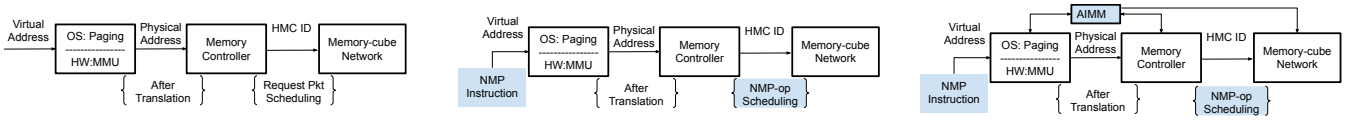
With the explosion of data, emerging applications such as machine learning and graph processing [1], [2] have driven copious data movement across the modern memory hierarchy. Due to the limited bandwidth of traditional double data rate (DDR) memory interfaces, memory wall becomes a major bottleneck for system performance [3], [4]. Consequently, 3D-stacked memory cubes such as the hybrid memory cube (HMC) [5] and high bandwidth memory (HBM) [6] were invented to provide high bandwidth that suffices the tremendous bandwidth requirement of big data applications. Although high-bandwidth stacked memory has reduced the bandwidth pressure, modern processor-centric computation fails to process large data sets efficiently due to the expensive data movement of low-reuse data. To avoid the high cost of data movement, near-memory processing (NMP) was revived and enabled memory-centric computing by moving the computation close to the data in the memory [7], [8], [9], [10], [11].

Recently, memory-centric NMP systems demand even larger memory capacity to accommodate the increasing sizes of data sets and workloads. For example, the recent GPT-3 transformer model [12] has 175 billion parameters and requires at least 350 GB memory to load a model for inference and even more memory for training. As a solution, multiple memory cubes can be combined to satisfy the high demands [11]. For instance, the recently announced AMD Radeon VII and NVIDIA A100 GPU have each included 4 and 6 HBMs, respectively. More memory cubes are adopted in recent works to form a memory-cube network [13], [14] for further scale-up. Moreover, NMP support for memory-cube network has also been investigated in recent proposals to accelerate data-intensive applications [10].

Along with the NMP and memory system developments, memory mapping for placing data and computation in the memory-cube network has become an important design consideration for NMP system performance. Figure 1a shows an overview of the data mapping in two steps—virtual-to-physical page mapping and physical-to-DRAM address mapping. The paging system maps a virtual page to a physical page frame, then the memory controller hashes the physical address to DRAM address, which identifies the location in the DRAM. For NMP systems, the memory mapping should handle computation as well as data, as shown in Figure 1b. Besides the data mapping, the memory controller also decides the memory cube in which the NMP operation is to be scheduled.

Many works have focused on physical-to-DRAM address mapping to improve the memory-level parallelism [15], [16], [17]. Recently, DRAM address mapping has been investigated in NMP systems to better co-locate data in the same cubes [11]. However, adapting the mapping for the dynamic NMP application behavior is problematic due to the possibility of excessive data migration for every memory byte in order to reflect the new mappings. On the other hand, virtual-to-physical page frame mapping provides an alternative approach to adjust the data mapping during run time. Although such research has existed for processor-centric NUMA systems [18], [19], [20], [21], it has not yet been explored for the memory-centric NMP systems, where computation is finer grained and tightly coupled with data in the memory system.

Furthermore, recent NMP research [7], [10] tightly couple the computation mapping with given data mapping for static offloading, which has not considered the co-exploration of the intermingling between them. This may cause computation resource under utilization in different cubes and lead to performance degradation, especially for irregular data such as graphs [22] and sparse matrices [23]. Thus, it is challenging to achieve an optimal memory mapping for NMP with another dimension of computation mapping. Moreover, the unique and dynamic application behaviors as well as the intractable decision space. We conservatively calculate the decision space by taking the minimum number of pages touched (n pages) in any epoch in our set of applications, and mapping them to any of the m cubes, which constitutes = m^n, where MIN(n) = 12 and m = 16 in our system $\approx 10^{14}$. With NMP in the



(a) Data mapping in conventional system. (b) Memory (data/compute) mapping in NMP system. (c) Memory mapping in NMP system with AIMM.

Fig. 1: Memory mapping in different systems: (a) data mapping in conventional system, (b) data and compute mapping in NMP system, and (c) data and compute mapping in NMP system with AIMM.

memory-cube network make it even more challenging to design a universal optimal mapping for all types of workloads.

In this paper, we propose an artificially intelligent memory mapping scheme, AIMM, that optimizes data placement and resource utilization through page and computation remapping. AIMM can adapt to different applications and runtime behaviors by continuously evaluating and learning the impact of mapping decisions on system performance. It uses a neural network to learn the near-optimal mapping at any instance during execution, and is trained using reinforcement learning, which is known to excel at exploring vast design space. Figure 1c depicts a system overview augmented by AIMM. In the proposed system, AIMM interacts with the paging system, the memory controller, and the memory-cube network. It continuously evaluates the NMP performance through the memory controller and makes data remapping decisions through the paging and page migration systems in the memory network. It is also consulted for computation remapping to improve NMP operation scheduling and performance.

The contributions of this paper are as follows.

- An artificially intelligent memory mapping, AIMM, for adjusting the memory mapping dynamically to adapt to application behavior and to improve resource utilization in NMP systems. To the best of our knowledge, this is the first NMP work that targets mapping of both data and computation.
- A reinforcement learning formulation to explore the vast design space and to train a neural network agent for the memory mapping problem.
- A detailed hardware design and practical implementation in a plug-and-play manner to be applied in various NMP systems.
- A comprehensive set of experimental results which show that the proposed AIMM improves the performance of state-of-the-art NMP systems in single and multi program scenarios up to 55% and 50% respectively.

The rest of the paper is organized as follows. In §II we discuss the background and related work. Next, we state the problem and formulate the proposed approach as a reinforcement learning problem in §III. In §IV, we propose a practical hardware design for AIMM followed by the evaluation methodology in §V. Then, we present and analyze the results in §VI. Finally, we conclude this work in §VII.

II. Background and Related Work

In this section, we introduce the background and related works, including near-memory processing, memory mapping and management, as well as reinforcement learning and its architecture applications.

A. Near-Memory Processing

Recently, near-memory processing (NMP) [7], [8], [11], [9], [10] was revived with the advent of 3D-stacked memory [5], [6]. In an NMP system with 3D memory cubes, the processing capability is in the base logic die under a stack of DRAM layers to utilize the ample internal bandwidth [7]. Later research also proposes *near-bank processing* with logic near to the memory banks in the same DRAM layer to exploit even higher bandwidth [24], [25], such as FIMDRAM [26] announced recently by Samsung. Recent proposals [27], [28], [29], [30], [31], [32] have also explored augmenting traditional DIMMs with computation in the buffer die to provide low-cost bandwidth-limited NMP solutions.

For computation offloading, there are mainly two ways: instruction offloading and kernel offloading. PIM-Enabled Instruction (PEI) [7], for instance, offloads instructions from the CPU to memory using the extended ISA. Other works such as GraphPim [9], Active-Routing [10], FIMDRAM [26], and DIMM NMP solutions [27], [29], [30], [31] also fall in the same category. For kernel offloading, similar to GPU, kernel code blocks are offloaded to the memory through library and low-level drivers, such as Tesseract [8], TOM [11].

We implement Basic NMP (BNMP), following Active-Routing [10] without the in-network computing capability for scheduling each operation in the memory cube. The NMP operation format is considered as `<&dest += &src1 OP &src2>`, where the `&dest` page host cube is considered as the computation point. Each cube has an NMP-Op table to temporarily buffer the source operands. An entry is made in the NMP-Op table at the computation cube and requests are sent to other memory cubes if sources do not belong to the same cube as the destination operand page. Upon receiving responses for the sources, the computation takes place and the NMP-Op table entry is removed once the result is written to the memory read-write queue for writing back to memory. The response is also sent back to the CPU if required. BNMP is considered as the baseline technique for most of the experimentation.

In this work, we study the memory mapping problem and propose AIMM for data and computation placement for NMP systems. We use physical-to-DRAM address mapping to improve data co-location and to reduce off-chip data movement in recent research [11]. However, it is not advisable to adjust DRAM mapping at runtime for adapting to application's memory access behavior as, such adjustment would trigger physical movement for every memory byte and incur prohibitive

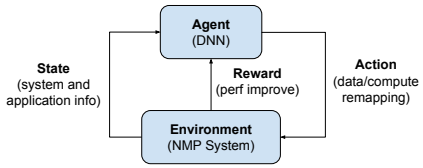


Fig. 2: A typical reinforcement learning framework.

performance overhead. On the other hand, we explore virtual-to-physical mapping through page migration to achieve low-cost dynamic remapping. To explore the missed opportunity of dynamic computation remapping, AIMM co-explores data and computation mapping holistically in NMP to further drive the performance improvement. We showcase with several NMP solutions along with processing-in-logic layers and NMP operations offloading to demonstrate the effectiveness of AIMM. Since our solution is decoupled from the NMP design, it is applicable to various NMP alternatives.

B. Heuristic-based Memory Management

Traditionally, operating systems (including kernels, system libraries, and runtimes) employ a heuristic approach [33], opting for solutions which promote locality [34], [35], [36], [37] and defragmentation [36], [38] for more efficient memory management. An OS's memory management system typically includes page and object allocators (either in-applications or in-kernel) [34], [36], [38], kernel page fault handlers [39], [40], [41], and application garbage collectors [35], [42], [43]. With OSes being oblivious to the underlying hardware, their best effort approaches may lead to sub-optimal performance for many applications. A thread-private allocator like HOARD [34] uses bulk allocation and per-thread free lists to try to ensure the proximity of memory access within one thread. For Non-Uniform Memory Access (NUMA) [44] architecture, Linux assigns physical memory to processes based on CPU affinity [45], and migrates when necessary.

Apart from NUMA, page migration is also proven useful in heterogeneous systems, such a CPU-GPU or multi-GPU shared memory system, where "first-touch" approach [46], [47], [48] can localize memory allocation to the first thread or the first GPU who accesses the memory, but does not guarantee the locality in future computation. Baruah et al. [49] proposes to select pages and migrate them at runtime to the highly predicted GPU. In this work, we co-explore both data movement and computation scheduling to improve resource utilization.

C. Reinforcement Learning (RL)

RL is a machine learning method where an agent explores actions in an environment to maximize the accumulative rewards [50]. In this paper, RL is used to design an agent that explores data and computation remapping decisions (actions) in the NMP system (environment) to maximize the performance (rewards). Figure 2 shows a typical setting of RL, where an agent interacts with the environment $\mathcal{E}$ over a number of discrete time steps. At each time step t, the agent observes an environment state $s_t \in \mathcal{S}$ *(state space)*, and selects an action $a_t \in \mathcal{A}$ *(action space)* to change the environment according to its policy π, which is a mapping from s_t to a_t. In return, it receives a reward r_t and a new state s_{t+1} and continues the same process. The accumulative rewards after time step t can be calculated as

$$R_t = \sum_{t'=t}^{T} \gamma^{t'-t} r_{t'} \tag{1}$$

where $\gamma \in (0,1]$ is the discount factor and T is the time step when the process terminates. The state-action value function $Q_\pi(s,a)$ under policy π can be expressed as

$$Q_\pi(s,a) = \mathbb{E}_\pi[R_t | s_t = s, a_t = a] \tag{2}$$

The objective of the agent is to maximize the expected reward.

In this paper, we use Q-learning [51] that selects the optimal action a^* that obtains the highest state-action value (Q value) $Q^*_\pi(s,a^*) = \max \mathbb{E}_\pi[R_t | s_t = s, a_t = a^*]$ following the *Bellman equation* [50]. The Q value is typically estimated by a function approximator. In this work, we use a deep neural network with parameters θ as the function approximator to predict the optimal Q value $Q(s,a;\theta) \approx Q^*(s,a)$. Given the predicted value $Q(s_t,a_t;\theta)$, the neural network is trained by minimizing the squared loss:

$$L(\theta) = (y - Q(s_t,a_t;\theta))^2, \tag{3}$$

where $y = r_t(s_t,a_t) + \gamma \max_{a'} Q(s_{t+1},a';\theta | s_t,a_t)$ is the target that represents the highest accumulative rewards of the next state s_{t+1} if action a_t is chosen for state s_t.

RL has been widely applied to network-on-chip (NoC) for power management [52], loop placement for routerless NoC [53], arbitration policy [54], and reliability [55]. It has also been used for designing memory systems, such as prefetching [56] and memory controller [57]. Additionally, it has been applied to DNN compilation and mapping optimization [58], [59], [60]. In this work, we use RL for co-exploration of data and computation mapping in NMP systems.

III. Proposed Approach

In this section, we introduce our proposed approach by first presenting the overview and problem formulation. Then we describe the representations of state, action and reward function for AIMM NMP memory mapping, followed by the DNN architecture and training of the RL-based agent.

A. Overview and Problem Formulation

AIMM continuously evaluates the data mapping done by the OS and computes cube decisions made by the MCs. Meanwhile, it provides suggestions to change not only the decision if necessary, but also the degree of the change (such as migration distance) in some cases. RL agent also learns the remapping and migration cost from the system feedback for each of its actions, and decides accordingly in the future (shown in Figure 3 ❶). The problem formulation is a challenging process due to the problem complexity and the lack of straightforward methodical ways. We explore two representations in this research: (1) Dataflow graph representation of accessed pages of an application; (2) Access history of each page along with the associated events (page miss, row-buffer hits, and vault accesses, etc.).

The first one involves costly hardware resources for storing the dataflow graph and expensive Node2Vec embedding [61] for processing the states. So we chose the second one that is more cost-effective. We detail the representation of states, actions, and reward function of our formulation as follows.

1) State Representation: Based on domain knowledge, the state representation (ten parameters) consists of system parameters (four) and page access history (six), as summarized in Table I. The RL agent takes this state information to improve the system performance through dynamic page-frame mapping. System information helps the RL agent to be aware of the system, while page information helps to focus on each page while taking an action. After collecting the required information of variable vector lengths, each of them is flattened into single vector of size 128×8 Bytes (128 64-bit entries). This leads to a vast space with $2^{128\times64} = 2^{8192}$ states in total in our system, making the problem very challenging.

System Information		Page Information	
Parameter Description	Vector Length	Parameter Description	Vector Length
NMP-op tab cccupancy	n cubes	Page access rate	1
Row-buffer hit rate	n cubes	Migration per access	1
MC queue occupancy	m MCs	Hop count, Pkt lat	History length
Global actions	History length	Migration lat, Page action	History length

TABLE I: The state representation of AIMM.

2) Action Representation: The actions are categorized into (1) computation migration, (2) page migration, and (3) training interval, as shown in Table II. In addition, the default action (no change) allows the RL agent to agree with the conventional system. "Near" and "Far" map to a randomly chosen neighboring HMC and the diagonally opposite remote HMC, respectively. Source co-location under page migration allows the system to co-locate NMP operand pages as a special case of page migration. The training interval regulates the epoch length in a range, discussed in §V.

Default	Computation Migration		Page Migration			Training Interval	
No change	Near	Far	Near	Far	Co-locate sources	Increase	Decrease

TABLE II: List of actions sorted categorically.

3) Reward Function: As one of the most important components of the RL system, the reward function draws significant research attention [62], [63], [64] and demands a rigorous process (left for future work). We manually explore several reward functions, including use of magnitude of performance as the reward, which shows a slow or sometimes fluctuating learning curve. Hence, we digitize our reward function that returns a unit of positive (+1) and negative (-1) reward for performance improvement or degradation. Otherwise, a zero reward is returned. We have explored using the communication hop count as a performance metric, but it leads to a local minimum that does not reflect the performance goal. We empirically found that operations per cycle as a direct reflection of performance can achieve a robust learning process.

B. RL Agent

We use the off-policy, value-based deep Q-learning [51] algorithm for the proposed RL-based AIMM. For the state-action value estimation, we use a dueling network as a function approximator. The DNN model in the agent is a simple stack of fully connected layers, as shown in Figure 3 ❸. The agent takes the state and predicts the state-action value for each action. Then we use an ε-greedy Q-learning algorithm [50] to trade off the exploitation and exploration during the search and learning process. The algorithm selects an action randomly with probability ε to explore the decision space, and choose the action with the highest value with probability $1-\varepsilon$ to exploit the knowledge learned by the agent. To train the DNN, we leverage *experience replay* [51] by keeping the past experiences in the replay buffer and randomly draw the samples for training. Therefore, the learning and search process is more robust by consolidating the past experiences into the training process.

IV. Hardware Implementation

A. Information Orchestration

We propose hardware to orchestrate the system and page specific information for providing system and application state as well as rewards to the agent. In each memory cube, we deploy an NMP table for keeping the outstanding NMP operations (NMP-ops). Additionally, registers are used for tracking the NMP table occupancy status and the average row buffer hit rate in each cube. These two pieces of information are communicated to a cube's nearest memory controller (MC) periodically. In each MC, two vectors of system information counters are used to record the NMP table occupancy and average row buffer hit rate of its nearest cubes, respectively. Each counter saves the running average of the received value the MC receives from the corresponding cube. A global history of actions is also tracked in the RL agent.

To maintain the page specific information for applications, a fully associative page information cache is added in each MC to collect the related information. Each entry records the number of page accesses, number of migrations, and four histories, including the communication hop count, packet latency, migration latency, and actions taken for a page. Upon sending NMP-op from MC to memory, accesses and hop count history of the entries of involving pages are updated. If a page does not have a cache entry, the least frequently used policy is used to find one, which is cleared before updating. Different from conventional cache, the content of the victim entry is abandoned. When the MC receives an NMP acknowledgement (ACK), packet latency carried in the ACK is updated in the latency history of involving entries. The migration latency history of an entry is updated after migration finishes if the corresponding page is remapped for migration. Similarly, the action history is updated when the page is selected for the agent for an action. The page access rate and migrations per access are calculated when forming a state for the agent to reduce the overhead.

Upon an agent invocation, the system information is formed by concatenating the global history of actions tracked in the RL agent with the MC queue occupancy and system counter vectors from all the MCs. Meanwhile, the page information of a highly accessed page is selected from one of the MC page information cache, where the MCs take turns to provide the

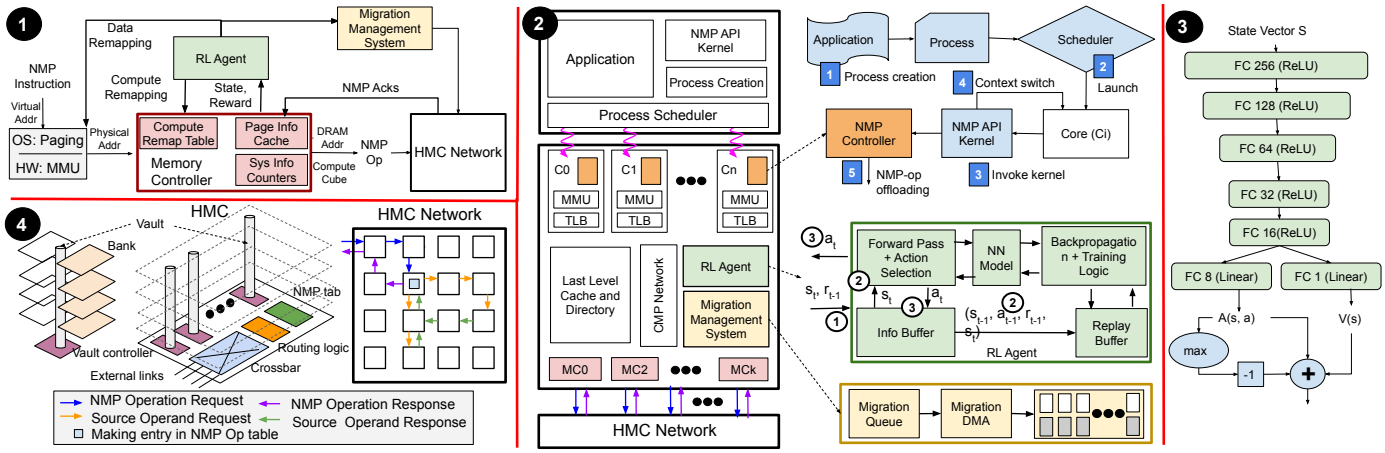


Fig. 3: AIMM reinforcement learning framework and system architecture: (1) overview of AIMM memory mapping for data and computation in NMP systems, (2) AIMM architecture, and (3) Dueling network for RL-based agent. (4) HMC network.

page information in a round-robin fashion. Then both system and page information are provided as a state to the agent for inference. The performance value (operations per cycle) is also collected from all the MCs and compared with the previous one to determine the reward.

B. RL Agent Implementation

We propose to use an accelerator (as shown in Figure 3) for deep Q-learning technique following such accelerators that have been proposed in literature [65], [66]. The agent, running on the accelerator, pulls information from each memory controller. The incoming information includes the new state s_t and a reward r_{t-1} for the last state-action (s_{t-1}, a_{t-1}), are stored in the information buffer (①). The incoming information and the previous state and action in the information buffer form a sample $(s_{t-1}, a_{t-1}, r_{t-1}, s_t)$, which is stored in the replay buffer (②). Meanwhile, the agent infers an action a_t on the input state s_t (②). The generated action a_t is stored back to the information buffer and transmitted back to the MCs which then perform the appropriate operations (③). Upon the training time, the agent draws a set of samples from the replay buffer for training and applies a back propagation algorithm to update the DNN model.

C. Page and Computation Remapping

Actively accessed pages are chosen as candidates to incorporate into state information for the agent to evaluate their fitness in the current location under the current system and application state. The agent may suggest page and computation remapping to adapt to the new application behavior and system state, which are implemented through page migration and NMP-op scheduling, respectively.

1) Page Remapping: It involves OS for page table update and the memory network for page migration to reflect a page remapping, where the virtual page is mapped to a new physical frame belonging to a memory cube suggested by the agent. We provide *blocking* and *non-blocking* modes for pages with *read-write* and *read-only* permissions, respectively. For blocking migration, the page is locked during migration and no access is allowed in order to maintain coherence, which also experiences TLB shootdown overhead, implemented using constant latency. For non-blocking migration, the old page frame can be accessed during the migration to reduce performance overhead. In addition, the TLB is extended with an extra physical address field, which goes through the update process in parallel to physical frame migration [67]. When a page migration is requested by the data remapping decision from the agent, the page number and the new host cube are put into the migration queue of the migration management system. When the migration DMA can process a new request, the OS is consulted to provide a frame belonging to the new host cube and broadcast a message to update the extended slot for the new physical frame location in the TLBs. Then DMA starts generating migration requests that request data from the old frame and transfer it to the new frame in the new host cube. Once migration finishes, a migration acknowledgement is sent from the new host to the migration management system, which then reports the migration latency to the memory controller. Meanwhile, an interrupt is raised to invoke the OS for a page table update. Because the parallel TLB shootdowns have updated the physical address in the TLBs, TLBs are ready to serve translation immediately after migration completion. Then in case of blocking migration, the page is unlocked for accessing, whereas for non-blocking migration, the old frame is put back to the free frame pool when the outstanding accesses finish.

2) Computation Remapping: Computation remapping decouples computation location and the data location for balancing load and improving throughput of the NMP memory network. Computation cube of an NMP-op is determined by the NMP-op scheduler based on the data address. The computation cube is then embedded in the offloaded NMP-op request packet. A compute remap table is used to remap the computation to a different cube suggested by the agent. When a compute remapping decision related to a page is given by the agent, the page number and the suggestion are stored in the compute remap table. Upon scheduling an NMP-op, the NMP-op scheduler consults the compute remap table. If the related

Hardware	Configurations
Chip Multiprocessor (CMP)	16 core, Cahce (32KB/each core), MSHR (16 entries)
Memory Controller (MC)	4, one at each CMP corners, Page Info Cache (128 entries)
Memory Management Unit (MMU)	4-level page table
Migration Management System (MMS)	Migration Quaue (128 entries), DMA (Rx,Tx buffers 128 entries)
Memory Cube	1GB, 32 vaults, 8 banks/vault, Crossbar
Memory Cube Network (MCN)	4×4/ 8 × 8 mesh, 3 stage router, 128 bit link bandwidth
NMP-Op table	512 entries
Hyper-parameters	reply-buffer (1000 entries), minibatch (128), learning rate (0.005)

TABLE III: Hardware configurations.

page of the NMP-op has an entry in the table, the computation cube is decided based on the agent suggestion recorded in the entry. Otherwise, the default scheduling is used.

V. Evaluation Methodology

In this section, we describe the simulation framework and methodology that implements and evaluates several NMP techniques and mapping schemes, respectively, followed by the workloads and analysis of their characteristics.

A. Simulation Framework

We develop a fast and accurate simulation framework (AIMM-sim) to model RL agent and system architecture. The RL agent is functionally modeled using keras-rl [68] and built upon gym [69]. Since we propose to use a hardware accelerator for RL implementation (as discussed in §IV-B), the timing aspect of the hardware accelerator is extracted using the MAESTRO inference model [70], considering training time as 2× of the inference time. The simulation framework takes an event-driven approach to model a cycle-level system architecture with three group of components, namely, (1) Front-end (2) Chip-Multi Processor (CMP) and associated components, and (3) HMC Model and HMC network. The RL agent and the system architecture model are seamlessly integrated in order to achieve high simulation speed. The hardware configurations used in our evaluation are summarized in Table III.

1) Front-end: The front-end of AIMM-sim supports writing micro-kernels using a simple programming interface (equipped with overloaded memory allocation API, memory access API, etc). The trace manger facilitates real application traces and derives NMP operations. The processes that are registered during the initialization phase are launched on their allocated cores at their specified launching time by the process scheduler.

2) CMP and Associated Components: The event-driven implementation of CMP consists of a set of in-order cores, four Memory Controllers (MC), MMU units, and an NMP controller connected through a fixed latency high-bandwidth crossbar (to helps to achieve high simulation speed). In a 64GB unified memory network formed using sixteen 4GB HMCs, MCs are responsible for determining the host cube of a given 36-bit physical address with 4 bits, and the remaining 32 bits are used to address (4GB) in each individual HMC. In addition, MCs create and send packets to respective HMCs, and also host page info caches to record page related information. The CMP, bus and the MCs have their respective queues, which backpressure NMP operation offloading; when they are full, forcing processors to stall fetching. The NMP controller helps create and offload the NMP operations to the HMC after the virtual-to-physical address translation, facilitated by the MMU unit equipped with a functional 4-level page table. The MMU also helps keep track of the migration candidates, and invokes DMA to initiate physical data migration through the memory network. Page faults are realized by employing process stall for a fixed number of cycles.

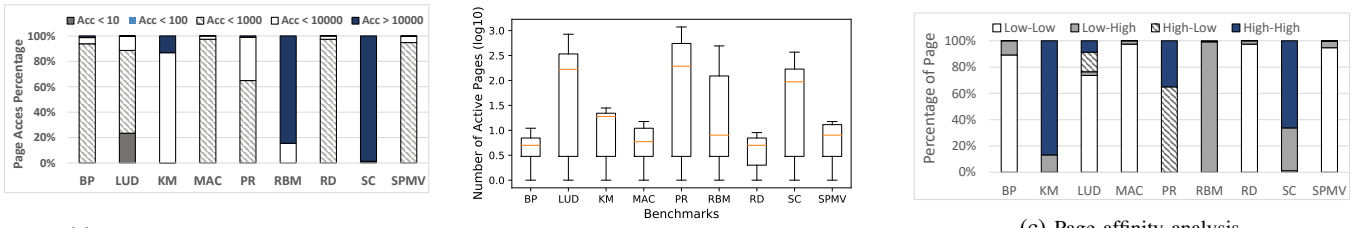
3) HMC Model and HMC network: The cycle accurate HMC network consists of event-driven HMC cubes [71] connected through the NI with the 3-stage pipelined router logic [72], and high bandwidth external SERDES links [73], [74]. The protocol deadlock is avoided using separate virtual channels (VCs) and network deadlock is avoided by using static XY routing. We aim for high-speed network simulation with simple round-robin alocation for the VC and switch. The HMC reflects two different latency situations (row buffer hit and row buffer miss). Each of the banks has a row-buffer and each of the vaults has 2 banks connected in each layer (total 4 layers), constituting a total of 8 banks per vault. Parallel vault (32) accesses are facilitated by their respective vault controllers. NMP operations, are stored in an NMP-op table in each HMC, where each entry in the table connects to a simple Processing Unit (PU). The PUs receive operands either from the vault of the local cube, or from the remote cube through the crossbar that connects all the vaults and the NMP-op table with the external links. We are prepared to make the framework public after the decision is made.

B. Simulation Methodology

AIMM-sim gives a parallel simulation view by running the hardware system and the RL agent in alternating epochs (100 to 250 cycles), where the RL agent recommends on the basis of system states in the last epoch to take action in the current epoch. The majority of the simulations are trace based, where the traces are collected by executing applications with data set-sizes ranging from 80 MB to 0.5 GB and annotating NMP-friendly regions of interest that were identified in previous works [7], [10]. The traces of an application form an episode for the application. AIMM evaluates both single-program and multi-program workloads, for several episodes (5 to 10), clearing the hardware system after each episode. The combinations of multi-program workloads are decided based on the workload analysis (§V-E). Unless otherwise mentioned BNMP is considered as our common baseline technique and NMP operations are marked as non-cacheable [10] (except in PEI, in §V-C2).

C. NMP Techniques and Mapping Schemes

We have implemented (1) three NMP techniques, Basic NMP (BNMP, discussed in §II), Load Balancing NMP (LDB), PIM Enabled Instruction (PEI)[7], (2) one physical address remapping technique, Transparent Offloading and Mapping (TOM) [11], and (3) state-of-the-art page-frame allocation policy HOARD [34]. In addition we also include an unrealistic (Genie) configuration for showing a highly optimistic performance upper-bound. We briefly discuss about each of them as follows.



(a) Page-access based classifications.

(b) Active page distributions.

(c) Page affinity analysis.

Fig. 4: Workload analysis graphs. (a) Classification of pages based on their access volume, (b) Active pages representing the working set, (c) Page affinity showing the interrelation among the pages in an application.

1) Load Balancing NMP (LDB): This is a simple extension of BNMP, based on two observations as follows. (1) Oftentimes, some NMP-Op table receives a disproportionate load based on the applications access pattern. (2) In most of the applications, the number of pages used for sources is significantly higher than the number of pages used for destination operands. Hence we simply change computation points from destination to sources in order to balance the load on the NMP-Op table. However, once the computation is done, the partially computed result must be sent back to the destination memory cube and also to the CPU.

2) PIM Enabled Instruction (PEI): This technique recognizes and tries to simultaneously exploit the benefit of cache memory as well as NMP. In case of a hit in the cache for at least one operand, PEI offloads operation with one source data to another source location in the main memory for computation.

3) Transparent Offloading and Mapping (TOM): This is a physical-to-DRAM address remapping technique, originally used for GPUs to co-locate the required data in the same memory cube for NMP. Before kernel offloading, TOM profiles a small fraction of the data and derives a mapping with best data co-location, which is used as the mapping scheme for that kernel. We imbibe the mapping aspect of TOM and make required adjustments to incorporate it in our context for remapping data in the NMP system. We infer data co-location from data being accessed by NMP-Op traces. Each mapping candidate is evaluated for a thousand cycles with their data co-location information recorded. Then the scheme with best data co-location that incurs the least data movement is used for an epoch.

4) HOARD: We adopted an NMP-aware HOARD [34] allocator as the baseline, heuristic-based OS solution for comparison and also as a foundation for experiment. HOARD is a classic multithreaded page-frame allocator which has inspired many allocator implementations [75], [76], [77] in modern OSes. The original version of HOARD focuses on improving the temporal and spatial locality within a multi-threaded application. HOARD maintains a global free list of larger memory chunks which are then allocated for each thread to serve the memory requests of smaller page frames or objects. Once the thread has finished the usage of the memory space, it chooses to "hoard" the space in a thread-private free list until the space is reused by the same thread or the whole chunk gets freed to the global free list. As a result, HOARD is able to co-locate data that belongs to same thread as much as possible. We adapted the thread-based heuristic of HOARD for each program in our multi-program workload setting. Our HOARD allocator aims for improving the locality within each program, contributing to the physical proximity of data that is expected to be accessed together in the NMP system.

Benchmarks	Description
Backprop (BP) [78]	Widely used algorithm for training feedforward neural networks. It efficiently computes the gradient of the loss function with respect to the weights of the network.
Lower Upper decomposition (LUD) [78]	In numerical analysis factors a matrix as the product of a lower triangular matrix and an upper triangular matrix.
Kmeans (KM) [79]	Kmeans algorithm is an iterative algorithm that tries to partition the data-set into K pre-defined distinct non-overlapping subgroups (clusters) where each data point belongs to only one group.
MAC	multipy-and-accumulate over two sequential vectors.
Pagerank (PR) [2]	PageRank works by counting the number and quality of links to a page to determine a rough estimate of how important the website is.
Restricted Boltzmann Machine (RBM)[1]	RBMs are a variant of Boltzmann machines[80], with the restriction that their neurons must form a bipartite graph.
Reduce (RD)	sum reduction over a sequential vector.
Streamcluster (SC) [81]	It assigns each point of a stream to its nearest center Medium-sized working sets of user-determined size.
Sparse matrix-vector multiply (SPMV) [79]	It finds applications in iterative methods to solve sparse linear systems and information retrieval, among other places.

TABLE IV: List of benchmarks.

5) Genie: For producing an upper bound of the execution time, we build a Genie (with unrealistic assumptions) that magically puts computation in the node with least congestion, and also instantly gets the operand pages in that node for immediate computations without any delay or overhead (not even memory access latency as shown in Figure 5, projects ≈12.5% standard deviation for improvement of Genie over AIMM, across applications.

D. Workloads

We primarily target the long running applications with large memory residency, which repeatedly use their kernels to process and compute on huge numbers of inputs. The machine learning kernels are a natural fit for that as they are widely used to process humongous amounts of data flowing in social media websites, search engines, autonomous driving, online shopping outlets, etc. These kernels are also used in a wide variety of applications such as graph analytics and scientific applications. To mimic realistic scenarios, we create both single and multi-program workloads using these application kernels. Since these are well known kernels, we describe them briefly in Table IV.

E. Workload Analysis

To capture the page-frame mapping related traits of the application, we characterize the workloads in terms of (1) page usage as an indicator of page life-time, (2) number of pages

actively used in an epoch as an indicator of working set, and (3) inter-relation among the pages (page affinity) accessed to compute NMP operations in order to analyze the difficulty level for optimizing their access latency.

1) Page Access Classification: The page usage is an indicator of its scope for learning the access pattern and improving performance after data or computation remapping at runtime. If the number of accesses to pages are very low, the scope for improvement using remapping technique narrows down to a great extent. In Figure 4a, we show that for most of our application kernels, the majority of the pages are moderate to heavily used over the whole application execution, which offers a substantial scope for AIMM.

2) Active Page Distribution: Figure 4b shows the number of pages touched in an epoch of 10000 cycles. We observe low page reuse across epochs, which marginally benefits from using caches. Hence, NMP offloading can save latency and bandwidth usage for these workloads. We can clearly identify two classes of applications. (1) High number of active pages, *LUD, PR, RBM, SC*, and (2) Low or moderate number of active pages, *BP, KM, MAC, RD, SPMV*. This study gives us an indication of the amount of page information, ideally needed to be stored in the page information cache for the training of the agent.

3) Affinity Analysis: In data mining, affinity analysis uncovers the meaningful correlations between different entities according to their co-occurrence in a data set. In our context, we use and define the affinity analysis to reveal the relationship among different pages if they are being accessed for computing the same NMP operation. We track two distinct yet interlinked qualities of page access pattern, (1) the number of pages related with a particular page as the radix for that page, which is similar to radix of the node in a graph, (2) the number of times each pair of connected nodes are accessed as part of the same NMP operation, similar to the weight for an edge. To understand the affinity, we create N number of bins for each of the traits and place the pages in the intersection of both by considering the traits together. So the affinity space is $N(accesses) \times N(radix)$, which is further divided into four quadrants to produce a consolidated result in Figure 4c. Based on our study, a higher affinity indicates a harder problem, which poses greater challenges for finding a near-optimal solution. On the contrary, they also exhibit and offer a higher degree of scope for improvement. Please note that this is only one aspect of the complexities of the problem. Interestingly in our collection, we observe a balanced distribution of workloads in terms of their page affinity.

VI. Experimentation Results

A. Performance

1) Execution Time: Figure 5, shows the execution time for different applications under various system setup and support. It is evident that AIMM is effective at helping the NMP techniques to achieve better performance in almost all cases. We observe up to 55% improvement in execution time. With BNMP processing, the NMP operations are completely on the memory side, both TOM and AIMM boost the performance of BNMP. In general, TOM achieves around 15% to 20% performance improvement. AIMM secures improvement in execution time by around 50% on average across all the benchmarks. However for LDB, TOM did not improve much for most of the benchmarks. With LDB, AIMM improves execution time up to 43%, with no performance degradation observed except minor performance loss for *SC*. In the case of PEI, it is evident that for the majority of benchmarks TOM degrades the performance, whereas AIMM manages to achieve performance benefit around 10% to 20% (up to 42%) on average. For *SPMV* and *MAC*, both TOM and AIMM degrade the performance of PEI. There are several factors that play major roles in our system to drive system performance, such as operation per cycle, learning rate, utilization of migrated pages, path congestion and computation level parallelism. In addition, hop count in the memory network and row buffer hit rate in the memory cube can be considered as primary contributors for performance, depending on the nuances of individual cases. In the following, we discuss each of the techniques to justify their performance.

In the case of *PR* on BNMP, AIMM does not improve over TOM, which can mostly be attributed to the 3× computation distribution achieved by TOM over AIMM as shown on Figure 6, in addition to very low migration page access for *PR* as shown in Figure 8. Figure 4a shows that *PR* has high number of pages that accessed small number of times, justifying low usage of migrated pages. Higher computation distribution improves NMP parallelism at the cost of extra communication if the computation node and operation destination are different. Low accesses to migrated pages diminishes the benefit of migration. On the other hand, AIMM achieves 50% better performance for *SPMV* that is ascribed to significant improvement in average hop count in Figure 6, moderate fraction pages migrated (40%) and they constitute almost 60% of all the accesses as shown in Figure 8. The performance of *SC* with TOM and AIMM allows us to delve into discussion of the trade-off between computation distribution and hop count in the memory network, along with importance of distribution of the right candidate in the right place. Missing one of them may offset the benefit achieved by the other, as the case for *SC* with TOM. On the contrary, AIMM leads to a better performance than TOM with very moderate compute distribution and low hop count as shown in Figure 6. Since LDB and PEI both tend to co-locate the sources belonging to an NMP operation, they leave much lesser chance than BNMP type techniques for further performance improvement using remapping like TOM or AIMM. The performance improvement is mainly achieved by optimizing the location of the destination pages with respect to the source operand pages.

B. Learning Convergence

Similar to Instruction Per Cycle (IPC), in our experimentation for memory operations we coined the term Operation Per Cycle (OPC) as an indicator of the system throughput. In Figure 7, we plot the timeline for OPC to show that AIMM progresses

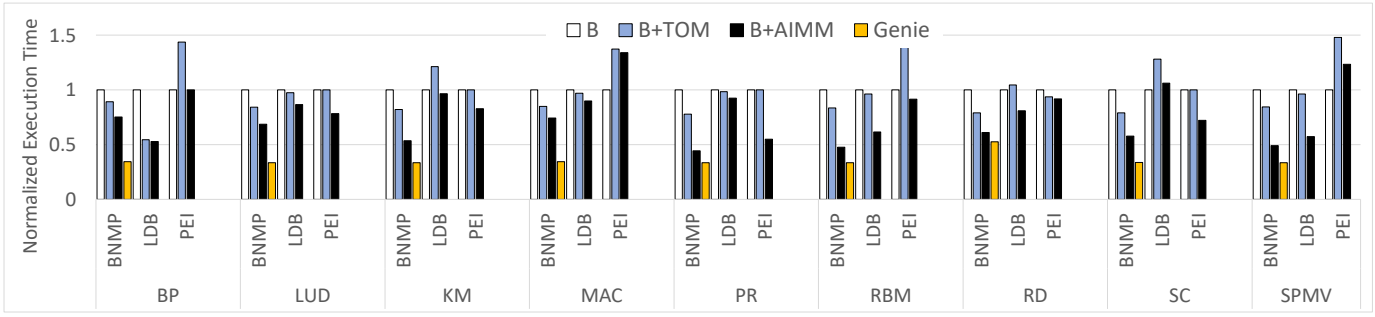


Fig. 5: Execution time for all the benchmarks, normalized individually with their basic techniques BNMP, LDB, and PEI respectively, which does not have any remapping support, and commonly referred as B in the graph. Execution time for the baseline implementations are compared to the system with remapping support, namely, TOM and AIMM, respectively. We have added an unrealistic setup (Genie) result to show a highly optimistic upper-bound.

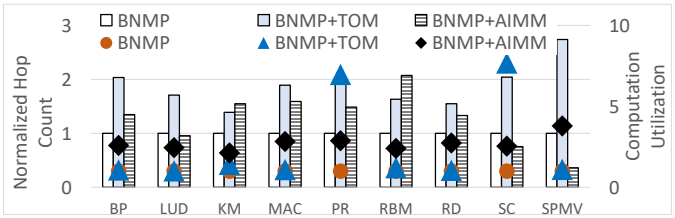
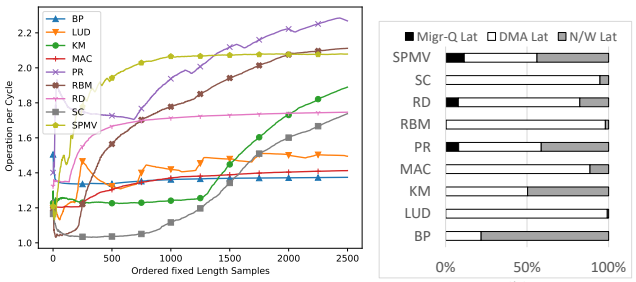


Fig. 6: Average Hop Count and Computation Utilization. Major Y-axis is shown in bars.



(a) (b)

Fig. 7: (a) Operation per cycle timeline. The X-axis is the sampled time and the Y-axis is the value for OPC. The graph is not monotonically increasing as OPC depends on several system parameters at runtime. (b) Migration latency breakdown.

towards the goal of achieving high OPC as the time advances for each of the applications. Since the number of operations are different for each of the applications, number of samples collected for each of the applications are also different. To plot them in the same graph we sampled them to a fixed size while preserving their original order. The convergence signifies that the agent can learn from the system and is able to maintain steady performance once converged. As the system situation keeps changing, we periodically evaluate the system and dynamically remap the page and computation location in the memory network in order to achieve near-optimum performance at any point of time.

C. Migration

In Figure 8, we depict the fraction of pages being migrated for each application on the major Y-axis and the fraction of

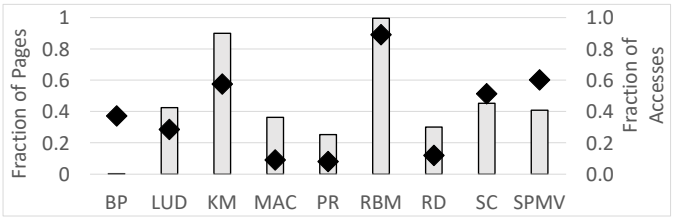


Fig. 8: Migration Stats: On the major axis we show the fraction of pages that are migrated for each of the applications using bars. On the minor axis it projects the fraction of total accesses that are happened on migrated pages, with diamond shaped markers.

total accesses requested that belong to a migrated page on the minor Y-axis. The fraction of pages migrated is an indicator of the migration coverage. For instance, in the case of *RBM* 100% pages are migrated, and almost all the migrated pages get accessed later. Pages in *RBM* are susceptible to experience high volume of migration as (1) small number of pages are accessed most of the execution time, (2) in a small fixed time window almost all the pages are being accessed. On the other hand, *BP* has huge memory residency and relatively small working set, which leads to a low fraction of page migration as compared to the total number of pages. Interestingly, the small number of migrated pages constitute almost 40% of the total accesses, which is a near ideal scenario as low number of page migrations has a small negative impact on performance, and a high number of accesses to the migrated pages can potentially improve the performance, provided the decision accuracy is high. Figure 7b shows migration latency breakdown, where, depending on the application, the migration latency is distributed in different proportions between DMA and HMC network. We observe average migration costs $\approx$ 800 cycles to 2000 cycles, depending on the network congestion. That is why we use non-blocking migration for all of our experiments. The migration/access across all the applications ranges from 0.001% to 0.054%, which can be categorized as low to moderate frequency.

D. Hop Count and Computation Utilization

In terms of system performance, hop count and computation distribution hold a reciprocal relation as reducing hop count improves the communication time, but results in computation

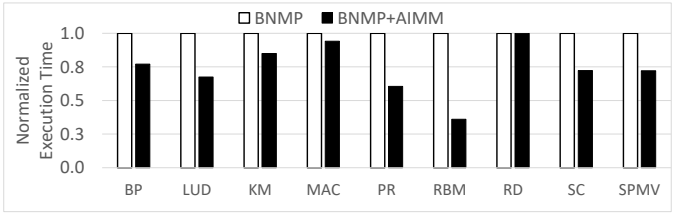


Fig. 9: Normalized execution time for 8x8 mesh.

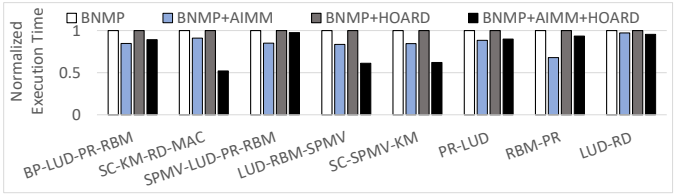


Fig. 10: Multi-process normalized execution time. BNMP and BNMP+HOARD are considered as two separate baselines and used for normalize BNMP+AIMM and BNMP+AIMM+HOARD results, respectively.

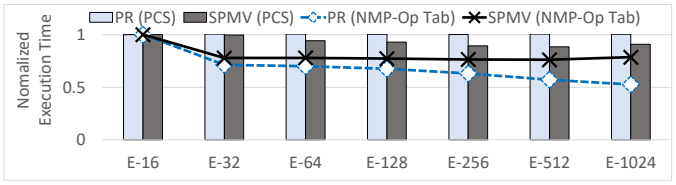


Fig. 11: Sensitivity study: The bar graph shows the sensitivity of the benchmarks for different page-cache sizes (PCS), whereas the line graph show the sensitivity to the NMP-Op table sizes (NMP-Op Tab).

under-utilization due to load imbalance across cubes. On the other hand, computation distribution may result in a high degree of hop count as concerned pages can only be in their respective memory cubes. Hence, a good balance between these factors is the key to achieving a near-optimal solution. Figure 6 shows that AIMM maintains a balance between the hop count and computation utilization. For instance, *PR* and *SC* individually achieves very high computation utilization which also leads to high average hop count. Assuming that the computation distribution decisions and corresponding locations are correct, the benefit gets diminished to 22% and 20% respectively possibly because of high hop count.

E. Scalability Study

In this subsection, we extend our experiments to study the impact of AIMM under a different underlying hardware configuration (8×8 mesh) as well as under highly diverse workloads together (2/3/4-processes). With a larger network, we expect to observe higher network impact on the memory access latency, and intend to show that AIMM can adapt to the changes in the system without any prior training on them. While choosing applications for multi-program workloads, we select diverse applications together based on our workload analysis, so that the RL agent experiences significant variations while trying to train and infer with them.

1) MCN Scaling: We observe that AIMM can sustain the changes in the underlying hardware by continuously evaluating them and without having any prior information. However, the amount of improvements for the applications are different than that in a 4×4 mesh. For instance, as shown in Figure 9, with BNMP+AIMM, *RBM* observes more benefit over BNMP, than it observes in the 4×4 mesh. As we know larger networks are susceptible to higher network latency, however, they also offer higher capacity and potential throughput. In the case of *RBM*, AIMM could sustain throughput, whereas benefits for other benchmarks slightly offset, mostly because of higher network delay. Note that in terms of simulation with larger network size, we did not change the workload size. Tuning hyper parameters is left for future work.

2) Multi-program Workload: Figure 10 shows multi-process execution time. For a continuous learning environment like AIMM, multi-program workloads pose a tremendous challenge on the learning agent as well as on the system. For studying the impact of multi-program workloads, we consider two baselines. (1) BNMP, where the NMP operation tables, page info cache, etc., are shared and contended among all the applications. We leave the study of priority based allocation or partitioning for future study. (2) BNMP+HOARD, where at the page frame allocator level our modified version of HOARD helps to co-locate data for each process, preventing data interleaving across processes. We observe that for several application combinations (*SC-KM-RD-MAC*, *LUD-RBM-SPMV*, *SC-SPMV-KM*), HOARD and AIMM compliment each other to achieve 55% to 60% performance benefits.

F. Sensitivity Study

We study the system performance by varying the sizes of (1) page info cache, whose size is critical for passing system information to the agent and (2) NMP operation table, whose size is important to hold the entries for NMP operations, denial of which affects memory network flow. We choose two representative applications (*PR*, *SPMV*) to study their performance by varying one parameter while keeping the other one to its default value, mentioned in Table III. (3) We also tune the training hyper-parameters for optimum results.

1) Page-info cache size (PCS): Figure 11 shows that *PR* exhibits very minimal sensitivity to page cache size, whereas *SPMV* finds its sweet point while increasing the number of entry from 32 (E-32) to 64 (E-64). As a general trend, applications that get the most benefit from AIMM are more sensitive to the page cache size than others. Based on this study, we empirically decide the number of page cache entry as 256.

2) NMP table size (NMP-Op Tab): NMP table size sensitivity depends on several parameters such as the number of active pages (Figure 4b), computation distribution, etc. In terms of active pages, *SPMV* has around 10 active pages on average in a time window. Figure 6 shows that *SPMV* has the highest computation distribution among the other applications. Combining these two pieces of data, it explains the reason for execution time saturation after 32 entries (E-32) for *SPMV*. On the other hand, *PR* has a very high demand for NMP operation table, as it has high active page count and low reuse rate. That

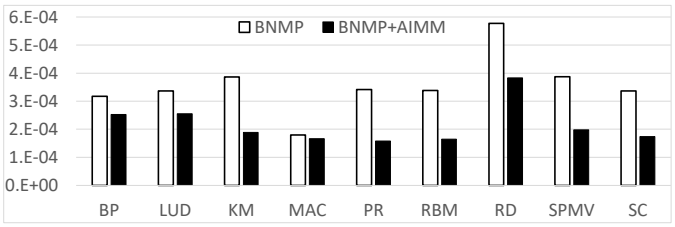


Fig. 12: Energy-delay product (lower is better).

is why *PR* shows monotonic improvement in execution time with the increase in the number of NMP table entries.

3) Training hyper-parameters: We study the sensitivity of the execution time with respect to replay-buffer size, frequency of training and learning rates. The replay-buffer size is varied 500× observing only up to 4% performance loss, which helped to optimize energy and area consumption without hurting performance much. As discussed earlier, training rate is controlled by the agent by its actions (action #6 and #7), we vary the upper and lower bound of it and observe a sweet point (execution time ±0.4% to ±13%). We apply the same strategy for learning rate as well, where we explore the spectrum to find the most suitable point (execution time ±0.1% to ±20%) and set as default for all the applications and experiments.

G. Area and Energy

In this section, we discuss the detailed area and energy aspect of our design. The implementation of the RL engine and migration management unit demands a separate provision in the chip. Additional energy consumption of information storing and propagation also contributes to the total energy consumption. We focus our study in five major design modules added for AIMM and discuss the area and energy aspects for each of them separately. For estimating the area and energy, we model all the buffers and caches using Cacti [82], 45nm technology, since these components contribute to most of the area and energy overhead in the system.

1) Information Orchestration: We estimated the area for hardware registers and page information cache as part of the information orchestration system. Since the hardware registers occupy negligible area, we mostly focus on the page information cache of size 64KB, which occupies 0.23 mm^2 area. The estimated per access energy for page information cache is 0.05nJ, which is consumed every time the cache is updated and read. Since the access volume varies across applications, we observe in the case of *BP*, page information cache consumes significantly higher access energy than that with other applications.

2) Migration: For the migration system, we consider three data storing points as a major contributor for area, namely, NMP buffer (512B, 0.14mm^2), Migration queue (2KB, 0.04mm^2), and DMA buffers (1KB, 0.124mm^2). It is worth noting that, depending on the organization and access method, the buffer and cache peripherals change significantly and so does their area. The per access energy consumption by these components are 0.122nJ, 0.02689nJ, 0.1062nJ, respectively. Page wise energy in the average case is composed of DMA leakage energy (15.51nJ) for waiting 500 cycles and the network cost for the whole page-frame transfer (574.44nJ), in total ≈ 600nJ.

3) RL Agent: For estimating the area and energy consumed by the RL agent, we focus on their major source of energy consumption that can easily be modeled as cache like structures, namely weight matrix (603KB, 2.095mm^2), replay buffer (≈512KB, 3.17mm^2), and state buffer (576B, 0.12mm^2). Their per access energy is estimated as 0.244nJ, 0.316nJ, and 0.106nJ, respectively.

4) Network and Memory: Since the migrations are realized by actually sending pages through the memory network with the help of DMA, we also estimate the network and memory cube energy consumption by assuming 5pJ/bit/hop [83] and 12pJ/bit/access [5] for the network and memory, respectively.

5) Overall Dynamic Energy: In our overall dynamic energy study, we include energy consumed by (1) only additional AIMM hardware, (2) memory network energy, and (3) memory cube energy, as major contributors to energy consumption in our framework. In Figure 12 we project Energy-Delay Product (EDP) as an overhead estimation metric, comparing the baseline and AIMM setup across the benchmarks. The EDP is roughly equivalent to the reciprocal of $MIPS^2$/Watt [84], where MIPS stands for Million Instructions per second and Watt (Joul/second) is the unit of power. In our case we replace instructions with NMP operations. The delay is the runtime, which is converted to seconds, assuming 2.66 GHz processor clock frequency. Overall EDP shows that, even though AIMM has some energy overhead over the baseline, it is still beneficial, as (except *MAC*) we observe that all the benchmarks' EDP is significantly lower than baseline.

VII. Conclusions

Careful articulation of data placement in the physical memory cube network (MCN) becomes imperative with the advent of Near-Memory Processing (NMP) in the big data era. In addition, scheduling computation for both resource utilization and data co-location in large-scale NMP systems is even more challenging than ever before. We propose AIMM, which is proven to be effective in assisting the existing NMP techniques mapped on MCN, by remapping their computation and data for improving resource utilization and optimizing communication overhead. Driven by the application's dynamic memory access behavior and the intractable size of data mapping decision space, AIMM uses Reinforcement Learning techniques as an approximate solution for optimization of the data and computation mapping problem. We project our technique as a plug-and-play module to be integrated with diverse NMP systems. The comprehensive experimentation shows significant performance improvement with up to 55% speedup for single-program workloads and up to 50% for multi-program workloads over baseline NMP. For broader application, AIMM can also facilitate data mapping in other near-data processing systems, such as processing in cache, memory, and storage.

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