

**ĐẠI HỌC QUỐC GIA TP.HỒ CHÍ MINH  
ĐẠI HỌC BÁCH KHOA  
NGÀNH KỸ THUẬT ĐIỆN TỬ**

# **Chapter 4**

# **Logic Synthesis**

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# Using DC Tool In Command Mode

Applications Places System Thu Mar 28, 2:57 PM phamdanglam

lampham@lampham:~/Work/02\_DC\_example

File Edit View Terminal Help

```
/home/lampham/Work/02_DC_example
```

```
dc_command.src design
```

```
[lampham@lampham 02_DC_example]$ tree
```

```
.
|-- dc_command.src
`-- design
    |-- examp1_and_gate.v
```

```
1 directory, 2 files
```

```
[lampham@lampham 02_DC_example]$
```

The Directory





## Set Library

## Analyze & Elaborate

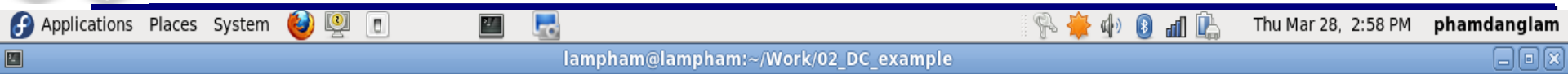
## Setup the Constraints

## Reports





# Using DC Tool In Command Mode



File Edit View Terminal Help

```
/home/lampham/Work/02_DC_example  
dc_command.src design  
[lampham@lampham 02_DC_example]$ tree
```

```
.  
|-- dc_command.src  
`-- design  
    |-- exampl_and_gate.v
```

```
1 directory, 2 files
```

```
[lampham@lampham 02_DC_example]$ getlicense
```

**Get License**



# Using DC Tool In Command Mode

```
Applications Places System [system icons] Thu Mar 28, 2:58 PM phamdanglam
lampham@lampham:~/Work/02_DC_example
File Edit View Terminal Help

Users of ALTGEN2: (Uncounted, node-locked)

Users of amat-calib_all: (Uncounted, node-locked)

Users of amga: (Uncounted, node-locked)

Users of amps: (Uncounted, node-locked)

Users of amps/cso: (Uncounted, node-locked)

Users of amps/pfx: (Uncounted, node-locked)

Users of amps/tr: (Uncounted, node-locked)

Users of AN-Impl3D_all: (Uncounted, node-locked)

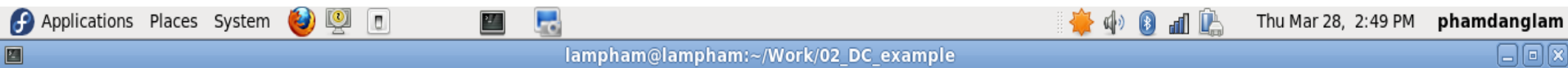
Users of any_technology: (Uncounted, node-locked)

[lampham@lampham 02_DC_example]$
```

General Neural\_Network NoC Other 7



# Using DC Tool In Command Mode



File Edit View Terminal Help

/home/lampham/Work/02\_DC\_example

dc command.src design

[lampham@lampham 02\_DC\_example]\$ dc\_shell

**Access DC Environment**



lampham@lampham:...

General

Neural\_Network

NoC

Other





# Using DC Tool In Command Mode

Applications Places System Thu Mar 28, 2:59 PM phamdanglam

lampham@lampham:~/Work/02\_DC\_example

File Edit View Terminal Help

```
Power Compiler (TM)
DesignWare (R)
DC Expert (TM)
Design Vision (TM)
HDL Compiler (TM)
VHDL Compiler (TM)
DFT Compiler
Library Compiler (TM)
Design Compiler(R)
```

**DC Command mode environment**

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Initializing.  
dc shell>

lampham@lampham:...

General Neural\_Network NoC Other 9



# Using DC Tool In Command Mode

Applications Places System Thu Mar 28, 3:05 PM phamdanglam

lampham@lampham:~/Work/02\_DC\_example

File Edit View Terminal Help

```
Power Compiler (TM)
DesignWare (R)
DC Expert (TM)
Design Vision (TM)
HDL Compiler (TM)
VHDL Compiler (TM)
DFT Compiler
Library Compiler (TM)
Design Compiler(R)

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Initializing...
dc_shell> source dc_command.src
```

**Run DC commands**

General Neural\_Network NoC Other

10



# Using DC Tool In Command Mode

```
Applications Places System [system icons] Thu Mar 28, 3:09 PM phamdanglam
lampham@lampham:~/Work/02_DC_example
File Edit View Terminal Help
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Initializing...
dc_shell> source dc_command.src
Running PRESTO HDLC
Compiling source file /home/lampham/Work/02_DC_example/design/examp1_and_gate.v
Presto compilation completed successfully.
Loading db file '/home/lampham/synopsys/library/TSMC_65nm/aci/sc-ad12/synopsys/
scadv12_cln65lp_hvt_ff_1p32v_0c.db'
Loading db file '/home/lampham/synopsys/DC-2012.06-SP2/libraries/syn/gtech.db'
Loading db file '/home/lampham/synopsys/DC-2012.06-SP2/libraries/syn/standard.s
ldb'
Loading link library 'scadv12_cln65lp_hvt_ff_1p32v_0c'
Loading link library 'gtech'
Running PRESTO HDLC

Inferred memory devices in process
in routine examp1_and_gate line 35 in file
'/home/lampham/Work/02_DC_example/design/examp1_and_gate.v'.
[taskbar icons] lampham@lampham:... General Neural_Network NoC Other
```



# Using DC Tool In Command Mode

Applications Places System Thu Mar 28, 3:10 PM phamdanglam

lampham@lampham:~/Work/02\_DC\_example

File Edit View Terminal Help

Report : area  
Design : exampl\_and\_gate  
Version: G-2012.06-SP2  
Date : Thu Mar 28 15:09:08 2013  
\*\*\*\*\*

Information: Updating design information... (UID-85)  
Library(s) Used:

scadv12\_cln65lp\_hvt\_ff\_1p32v\_0c (File: /home/lampham/synopsys/library/TSMC\_65nm/aci/sc-ad12/synopsys/scadv12\_cln65lp\_hvt\_ff\_1p32v\_0c.db)

Number of ports:	26
Number of nets:	35
Number of cells:	17
Number of combinational cells:	9
Number of sequential cells:	8
Number of macros:	0
Number of buf/inv:	1
Number of references:	3

Combinational area:	24.480001
Buf/Inv area:	1.440000
Noncombinational area:	96.000000
Net Interconnect area:	undefined (No wire load specified)

Total cell area:	120.480001
Total area:	undefined

report\_area

General Neural\_Network NoC Other



# Using DC Tool In Command Mode

Applications Places System Thu Mar 28, 3:11 PM phamdanglam

lampham@lampham:~/Work/02\_DC\_example

File Edit View Terminal Help

```
*****
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : exampl_and_gate
Version: G-2012.06-SP2
Date   : Thu Mar 28 15:09:52 2013
*****
```

Operating Conditions: ff\_1p32v\_0c Library: scadv12\_cln65lp\_hvt\_ff\_1p32v\_0c  
Wire Load Model Mode: top

Startpoint: data\_out\_and\_gate\_reg[0]  
(rising edge-triggered flip-flop clocked by clk)  
Endpoint: data\_out\_and\_gate[0]  
(output port clocked by clk)  
Path Group: clk  
Path Type: max

Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
data_out_and_gate_reg[0]/CK (DFFRPQX1MA12TH)	0.00	0.00 r
data_out_and_gate_reg[0]/Q (DFFRPQX1MA12TH)	0.15	0.15 f
data_out_and_gate[0] (out)	0.00	0.15 f
data arrival time		0.15

lampham@lampham:...

General Neural\_Network NoC Other

report\_timing



# Using DC Tool In Command Mode

Applications Places System Thu Mar 28, 3:11 PM phamdanglam

lampham@lampham:~/Work/02\_DC\_example

File Edit View Terminal Help

```
-delay max
-max_paths 1
Design : exampl_and_gate
Version: G-2012.06-SP2
Date   : Thu Mar 28 15:09:52 2013
*****

Operating Conditions: ff_1p32v_0c   Library: scadv12_cln65lp_hvt_ff_1p32v_0c
Wire Load Model Mode: top

Startpoint: data_out_and_gate_reg[0]
            (rising edge-triggered flip-flop clocked by clk)
Endpoint:   data_out_and_gate[0]
            (output port clocked by clk)
Path Group: clk
Path Type:  max

Point                                     Incr      Path
-----
clock clk (rise edge)                    0.00      0.00
clock network delay (ideal)               0.00      0.00
data_out_and_gate_reg[0]/CK (DFFRPQX1MA12TH) 0.00      0.00 r
data_out_and_gate_reg[0]/Q (DFFRPQX1MA12TH) 0.15      0.15 f
data_out_and_gate[0] (out)                0.00      0.15 f
data arrival time                         0.15

clock clk (rise edge)                    2.00      2.00
clock network delay (ideal)               0.00      2.00
output external delay                     -1.00      1.00
data required time                        1.00
data arrival time                         -0.15
-----
slack (MET)                              0.85
```

lampham@lampham:...

General Neural\_Network NoC Other



# DC Tools

Applications Places System Thu Mar 28, 3:13 PM phamdanglam  
lampham@lampham:~/Work/02\_DC\_example

File Edit View Terminal Help

/home/lampham/Work/02\_DC\_example

```
command.log      design      exampl_and_gate.sdf      new_exampl_and_gate.v
dc_command.src   exampl_and_gate.ddc     exampl_and_gate-verilog.pvl
default.svf      EXAMP1_AND_GATE.mr      exampl_and_gate-verilog.syn
[lampham@lampham 02_DC_example]$ ll
```

total 244

```
-rw-rw-r--. 1 lampham lampham 176245 Mar 28 15:13 command.log
-rwxrwxr-x. 1 lampham lampham   762 Mar 28 15:12 dc_command.src
-rw-rw-r--. 1 lampham lampham   9216 Mar 28 15:13 default.svf
drwxrwxr-x. 2 lampham lampham   4096 Mar 28 14:40 design
-rw-rw-r--. 1 lampham lampham  22528 Mar 28 15:13 exampl_and_gate.ddc
-rw-rw-r--. 1 lampham lampham    23 Mar 28 15:13 EXAMP1_AND_GATE.mr
-rw-rw-r--. 1 lampham lampham  12231 Mar 28 15:13 exampl_and_gate.sdf
-rw-rw-r--. 1 lampham lampham   3700 Mar 28 15:13 exampl_and_gate-verilog.pvl
-rw-rw-r--. 1 lampham lampham    340 Mar 28 15:13 exampl_and_gate-verilog.syn
-rw-rw-r--. 1 lampham lampham   2321 Mar 28 15:13 new_exampl_and_gate.v
```

```
[lampham@lampham 02_DC_example]$
```

**Netlist file**





# DC Tools

```
module examp1_and_gate ( system_clock, system_rst_n, fist_data_in,  
    second_data_in, data_out_and_gate );  
input [7:0] fist_data_in;  
input [7:0] second_data_in;  
output [7:0] data_out_and_gate;  
input system_clock, system_rst_n;  
wire n1;  
wire [7:0] pre_data_out_and_gate;
```

**DFF cell**

```
DFFRPQX1MA12TH \data_out_and_gate_reg[7] ( .D(pre_data_out_and_gate[7]),  
    .CK(system_clock), .R(n1), .Q(data_out_and_gate[7]) );  
DFFRPQX1MA12TH \data_out_and_gate_reg[6] ( .D(pre_data_out_and_gate[6]),  
    .CK(system_clock), .R(n1), .Q(data_out_and_gate[6]) );  
DFFRPQX1MA12TH \data_out_and_gate_reg[5] ( .D(pre_data_out_and_gate[5]),  
    .CK(system_clock), .R(n1), .Q(data_out_and_gate[5]) );  
DFFRPQX1MA12TH \data_out_and_gate_reg[4] ( .D(pre_data_out_and_gate[4]),  
    .CK(system_clock), .R(n1), .Q(data_out_and_gate[4]) );  
DFFRPQX1MA12TH \data_out_and_gate_reg[3] ( .D(pre_data_out_and_gate[3]),  
    .CK(system_clock), .R(n1), .Q(data_out_and_gate[3]) );  
DFFRPQX1MA12TH \data_out_and_gate_reg[2] ( .D(pre_data_out_and_gate[2]),  
    .CK(system_clock), .R(n1), .Q(data_out_and_gate[2]) );
```

"new\_examp1\_and\_gate.v" 45L, 2321C

18,1

Top





# Using DC Tool In Command Mode

Applications Places System Thu Mar 28, 3:13 PM phamdanglam  
lampham@lampham:~/Work/02\_DC\_example

File Edit View Terminal Help

/home/lampham/Work/02\_DC\_example

```
command.log      design      exampl_and_gate.sdf      new_exampl_and_gate.v
dc_command.src   exampl_and_gate.ddc     exampl_and_gate-verilog.pvl
default.svf      EXAMP1_AND_GATE.mr      exampl_and_gate-verilog.syn
```

[lampham@lampham 02\_DC\_example]\$ ll

total 244

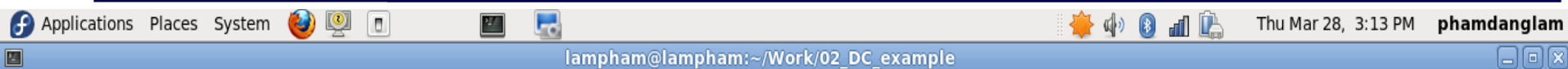
```
-rw-rw-r--. 1 lampham lampham 176245 Mar 28 15:13 command.log
-rwxrwxr-x. 1 lampham lampham    762 Mar 28 15:12 dc_command.src
-rw-rw-r--. 1 lampham lampham   9216 Mar 28 15:13 default.svf
drwxrwxr-x. 2 lampham lampham   4096 Mar 28 14:40 design
-rw-rw-r--. 1 lampham lampham  22528 Mar 28 15:13 exampl_and_gate.ddc
-rw-rw-r--. 1 lampham lampham    23 Mar 28 15:13 EXAMP1_AND_GATE.mr
-rw-rw-r--. 1 lampham lampham  12231 Mar 28 15:13 exampl_and_gate.sdf
-rw-rw-r--. 1 lampham lampham   3700 Mar 28 15:13 exampl_and_gate-verilog.pvl
-rw-rw-r--. 1 lampham lampham    340 Mar 28 15:13 exampl_and_gate-verilog.syn
-rw-rw-r--. 1 lampham lampham   2321 Mar 28 15:13 new_exampl_and_gate.v
```

**SDF file**

[lampham@lampham 02\_DC\_example]\$



# Using DC Tool In Command Mode



File Edit View Terminal Help

```
(DELAYFILmp1_and_gate.sdf
(SDFVERSION "0VI 2.1")
(DESIGN "examp1_and_gate")
(DATE "Thu Mar 28 15:13:15 2013")
(VENDOR "scadv12_cln65lp_hvt_ff_1p32v_0c")
(PROGRAM "Synopsys Design Compiler cmos")
(VERSION "G-2012.06-SP2")
```

```
(DIVIDER /)
(VOLTAGE 1.32:1.32:1.32)
(PROCESS "ff_1p32v_0c")
(TEMPERATURE 0.00:0.00:0.00)
(TIMESCALE 1ns)
```

```
(CELL
 (CELLTYPE "examp1_and_gate")
 (INSTANCE)
 (DELAY
  (ABSOLUTE
```

```
(INTERCONNECT system_rst_n U20/A (0.000:0.000:0.000))
(INTERCONNECT second_data_in[7] U19/A (0.000:0.000:0.000))
(INTERCONNECT first_data_in[7] U19/B (0.000:0.000:0.000))
(INTERCONNECT second_data_in[6] U18/A (0.000:0.000:0.000))
(INTERCONNECT first_data_in[6] U18/B (0.000:0.000:0.000))
```

-- INSERT --

1,26

Top



# Using DC Tool In Command Mode

Applications Places System Thu Mar 28, 3:13 PM phamdanglam

lampham@lampham:~/Work/02\_DC\_example

File Edit View Terminal Help

```
)  
(CELL  
  (CELLTYPE "INVX1BA12TH")  
  (INSTANCE U20)  
  (DELAY  
    (ABSOLUTE  
      (IOPATH A Y (0.056:0.056:0.056) (0.054:0.054:0.054))  
    )  
  )  
)  
(CELL  
  (CELLTYPE "AND2X1MA12TH")  
  (INSTANCE U19)  
  (DELAY  
    (ABSOLUTE  
      (IOPATH A Y (0.047:0.047:0.047) (0.045:0.045:0.045))  
      (IOPATH B Y (0.049:0.049:0.049) (0.047:0.047:0.047))  
    )  
  )  
)  
(CELL  
  (CELLTYPE "AND2X1MA12TH")  
  -- INSERT --
```

**INVERTER & AND Timing**

61,1 19%

General Neural\_Network NoC Other



# Using DC Tool In Command Mode

Applications Places System Thu Mar 28, 3:14 PM phamdanglam

lampham@lampham:~/Work/02\_DC\_example

File Edit View Terminal Help

```
)  
(CELL  
  (CELLTYPE "DFFRPQX1MA12TH")  
  (INSTANCE data_out_and_gate_reg\[1\])  
  (DELAY  
    (ABSOLUTE  
      (IOPATH (posedge CK) Q (0.140:0.140:0.140) (0.149:0.149:0.149))  
      (COND D == 1'b0 && CK == 1'b0 (IOPATH (posedge R) Q ( ) (0.105:0.105:0.105)))  
      (COND D == 1'b1 && CK == 1'b0 (IOPATH (posedge R) Q ( ) (0.104:0.104:0.104)))  
      (COND D == 1'b0 && CK == 1'b1 (IOPATH (posedge R) Q ( ) (0.092:0.092:0.092)))  
      (COND D == 1'b1 && CK == 1'b1 (IOPATH (posedge R) Q ( ) (0.092:0.092:0.092)))  
    )  
  )  
  (TIMINGCHECK  
    (PERIOD CK (1.000:1.000:1.000))  
    (SETUP (posedge D) (posedge CK) (0.041:0.041:0.041))  
    (SETUP (negedge D) (posedge CK) (0.021:0.021:0.021))  
    (HOLD (posedge D) (posedge CK) (-0.021:-0.021:-0.021))  
    (HOLD (negedge D) (posedge CK) (0.002:0.002:0.002))  
    (SETUP (negedge R) (posedge CK) (0.027:0.027:0.027))  
    (HOLD (negedge R) (posedge CK) (0.020:0.020:0.020))  
  )  
-- INSERT --
```

**DFF timing**

172,1 56%

General Neural\_Network NoC Other



# Using DC Tool In GUI Mode

Applications Places System Thu Mar 28, 2:49 PM phamdanglam  
lampham@lampham:~/Work/02\_DC\_example

File Edit View Terminal Help

/home/lampham/Work/02\_DC\_example

dc\_command.src design

[lampham@lampham 02\_DC\_example]\$ dc\_shell

Access DC Environment



# Using DC Tool In GUI Mode

Applications Places System Thu Mar 28, 2:49 PM phamdanglam

lampham@lampham:~/Work/02\_DC\_example

File Edit View Terminal Help

```
Design Compiler Graphical
DC Ultra (TM)
DFTMAX (TM)
Power Compiler (TM)
DesignWare (R)
DC Expert (TM)
Design Vision (TM)
HDL Compiler (TM)
VHDL Compiler (TM)
DFT Compiler
Library Compiler (TM)
Design Compiler(R)
```

## DC Environment

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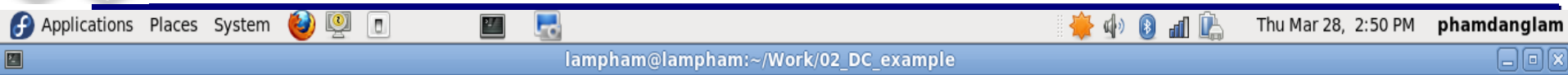
Initializing...  
dc\_shell> █

lampham@lampham:...

General Neural\_Network NoC Other



# Using DC Tool In GUI Mode



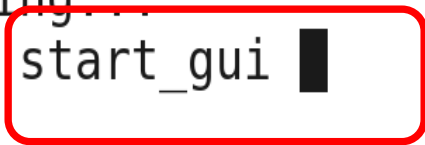
```
Version F-2011.09-SP3 for linux -- Jan 26, 2012  
Copyright (c) 1988-2011 Synopsys, Inc.
```

```
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```

```
Initializing...
```

```
dc_shell> start_gui █
```

**Start GUI Mode**





# Using DC Tool In GUI Mode

Applications Places System Thu Mar 28, 2:50 PM phamdanglam

Design Vision - TopLevel.1

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help

Hier.1

Logical Hie Cells (Hierarchical)

Cell Name	Ref Name	Cell Path	D
-----------	----------	-----------	---

```
dc_shell> start_gui
dc_shell>
```

**GUI Environment**

Log History

dc\_shell:

Ready

lampham@lampham:... Design Vision

General Neural\_Network NoC Other





# Using DC Tool In GUI Mode

Applications Places System Thu Mar 28, 2:50 PM phamdanglam

Design Vision - TopLevel.1

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help

Hier.1

Logical Hie Cells (Hierarchical)

Cell Name	Ref Name	Cell Path	Di
-----------	----------	-----------	----

dc\_shell> start\_gui  
dc\_shell>

Log History Options: ▾

dc\_shell> **source dc\_command.src**

Ready

lampham@lampham:... Design Vision

General Neural\_Network NoC Other

**Call The DC Commands**



# Using DC Tool In GUI Mode

Applications Places System Thu Mar 28, 2:51 PM phamdanglam

Design Vision - TopLevel.1 (examp1\_and\_gate)

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help

Hier.1

Logical Hie Cells (Hierarchical)

Cell Name	Ref Name	Cell Path	D
-----------	----------	-----------	---

Design Vision

Exit Design Vision ?

Cancel OK

Constraint	Cost
max_transition	0.00 (MET)
max_capacitance	0.00 (MET)
max_delay/setup	0.00 (MET)
critical_range	0.00 (MET)

Log History

dc\_shell>

Repopulating List ...

General Neural\_Network NoC Other

Report



# Using DC Tool In GUI Mode

Applications Places System Thu Mar 28, 2:51 PM phamdanglam

Design Vision - TopLevel.1 (examp1\_and\_gate)

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help

examp1\_and\_gate

Hier.1

Logical Hie

Cells (Hierarchical)

Cell Name	Ref Name	Cell Path	Di
-----------	----------	-----------	----

Create Design Schematic

max\_delay/setup 0.00 (MET)  
critical\_range 0.00 (MET)

Current design is 'examp1\_and\_gate'.  
dc\_shell>

Log History Options: ▾

dc\_shell>

Create Design Schematic of currently selected hierarchical cells

lampham@lampham:... Design Vision

General Neural\_Network NoC Other

**Review The Schematic (Gate Level)**



# Using DC Tool In GUI Mode

Applications Places System Thu Mar 28, 2:51 PM phamdanglam

Design Vision - TopLevel.1 (examp1\_and\_gate)

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help

examp1\_and\_gate

Hier.1

Logical Hie

Cell Name	Ref Name	Cell Path
-----------	----------	-----------

Schematic.1 examp1\_and\_gate

Hier.1 Schematic.1 examp1\_and\_gate

Current design is 'examp1\_and\_gate'.  
dc\_shell>  
Current design is 'examp1\_and\_gate'.  
Loading db file '/home/lampham/synopsys/DesignCompilerF-2011.09-SP3/libraries/syn/generic.sdb'

Log History Options:▼

dc\_shell>

Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)

lampham@lampham:... Design Vision

General Neural\_Network NoC Other

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# Using DC Tool In GUI Mode

Design Vision - TopLevel.1 (examp1\_and\_gate) - [Schematic.1 examp1\_and\_gate]

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help

examp1\_and\_gate

second\_data\_in[0] A U12 AND2X1MA12TH Y pr data\_out\_and\_gate[0] D data\_out\_and\_gate\_reg[0] DFFRPQX1MA12TH CK R Q

first\_data\_in[0] B U13 AND2X1MA12TH Y system\_clock n1 data\_out\_and\_gate\_reg[1]

Hier.1 Schematic.1 examp1\_and\_gate

Constraint	Cost
max_transition	0.00 (MET)
max_capacitance	0.00 (MET)

Log History

dc\_shell>

Options: ▾

Specify zoom out box (Click opposite corners or drag)

Net first\_data\_in[0]

General Neural\_Network NoC Other

29



# Using DC Tool In GUI Mode

Applications Places System Thu Mar 28, 2:52 PM phamdanglam

Design Vision - TopLevel.1 (examp1\_and\_gate)

File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help

examp1\_and\_gate

Hier.1

Logical Hie

Cells (Hierarchical)

Cell Name	Ref Name	Cell Path
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Schematic.1 examp1\_and\_gate

Hier.1 Schematic.1 examp1\_and\_gate

Current design is 'examp1\_and\_gate'.  
dc\_shell>  
Current design is 'examp1\_and\_gate'.  
Loading db file '/home/lampham/synopsys/DesignCompilerF-2011.09-SP3/libraries/syn/generic.sdb'

Log History

dc\_shell> **report\_timing**

Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)

lampham@lampham:... Design Vision

General Neural\_Network NoC Other

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# Q & A