ĐẠI HỌC QUỐC GIA TP.HỒ CHÍ MINH
ĐẠI HỌC BÁCH KHOA
NGÀNH KỸ THUẬT ĐIỆN TỬ

Chapter 4
Logic Synthesis

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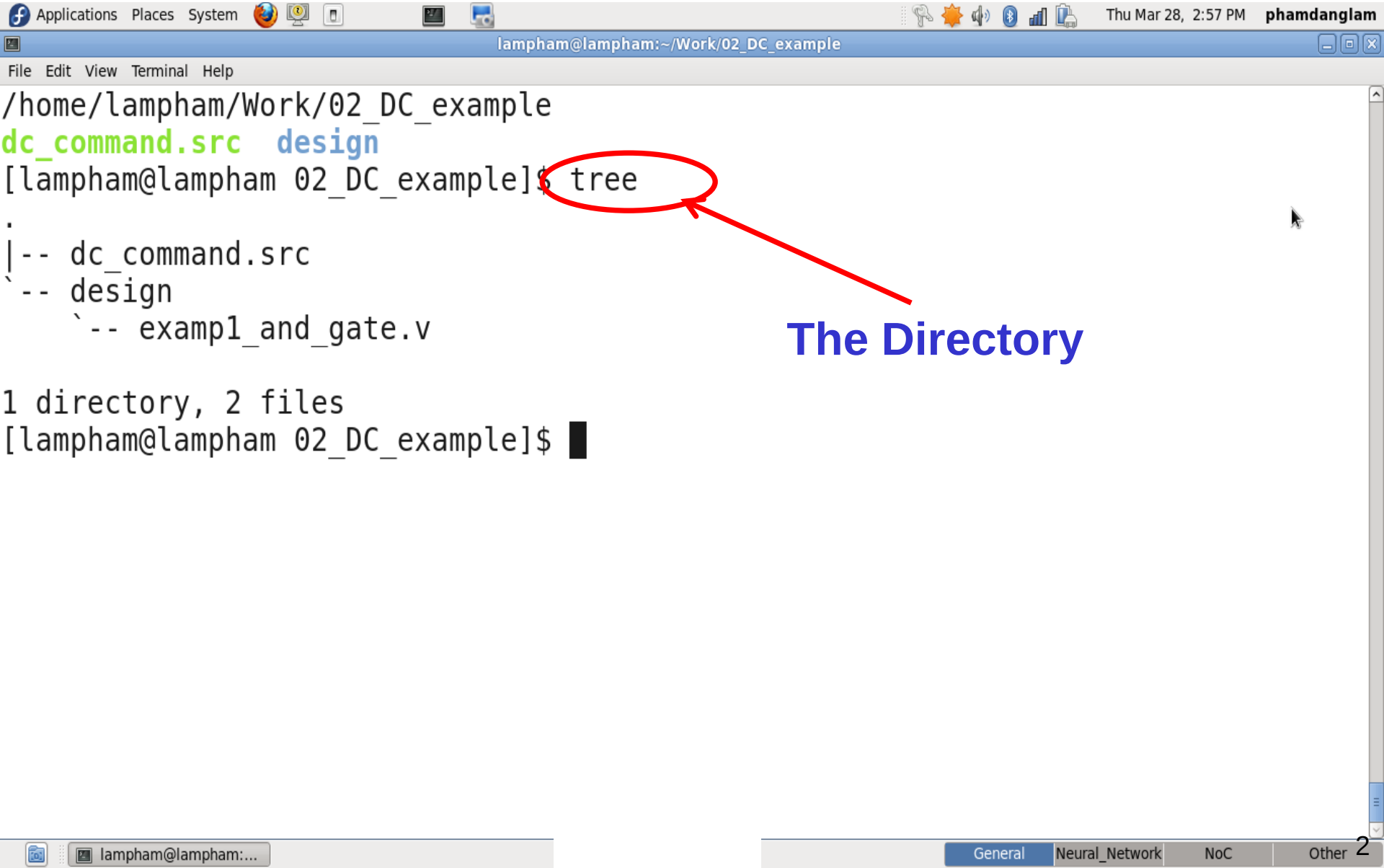
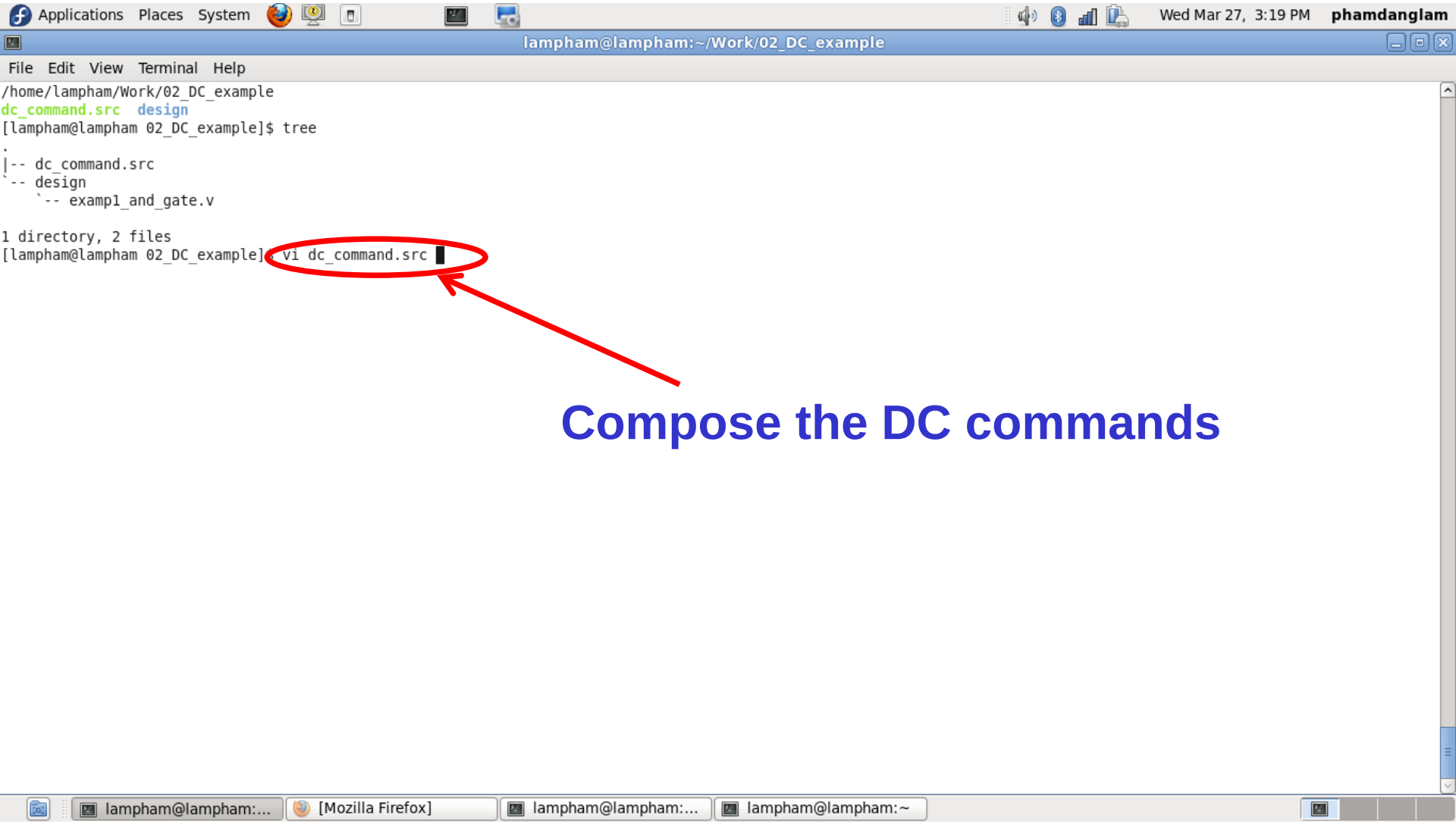
Using DC Tool In Command Mode

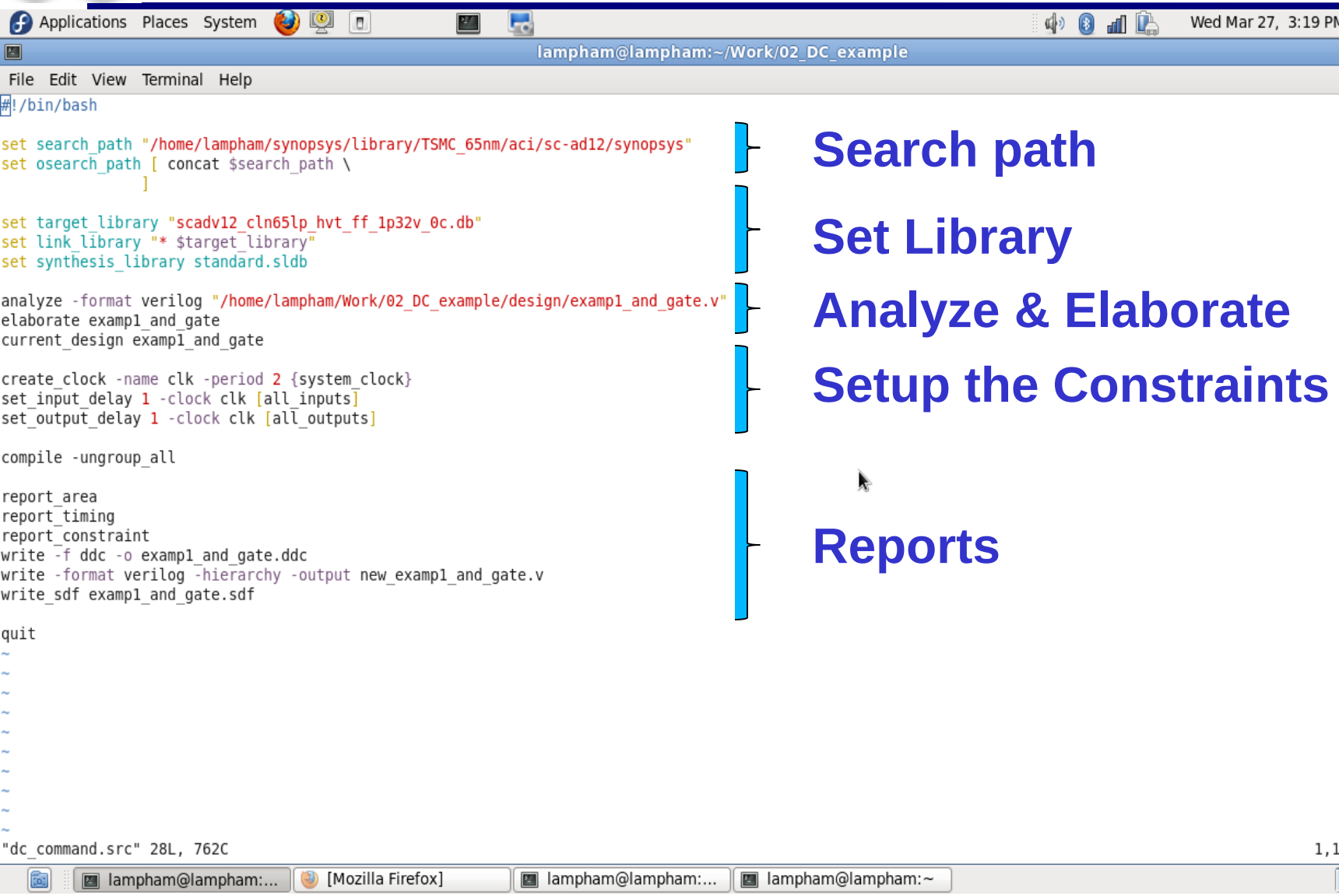


Using DC Tool In Command Mode



Compose the DC commands

Using DC Tool In Command Mode



Search path

Set Library

Analyze & Elaborate

Setup the Constraints

Reports

Using DC Tool In Command Mode

Applications Places System Wed Mar 27, 3:20 PM phamdanglam

lampham@lampham:~/Work/02_DC_example

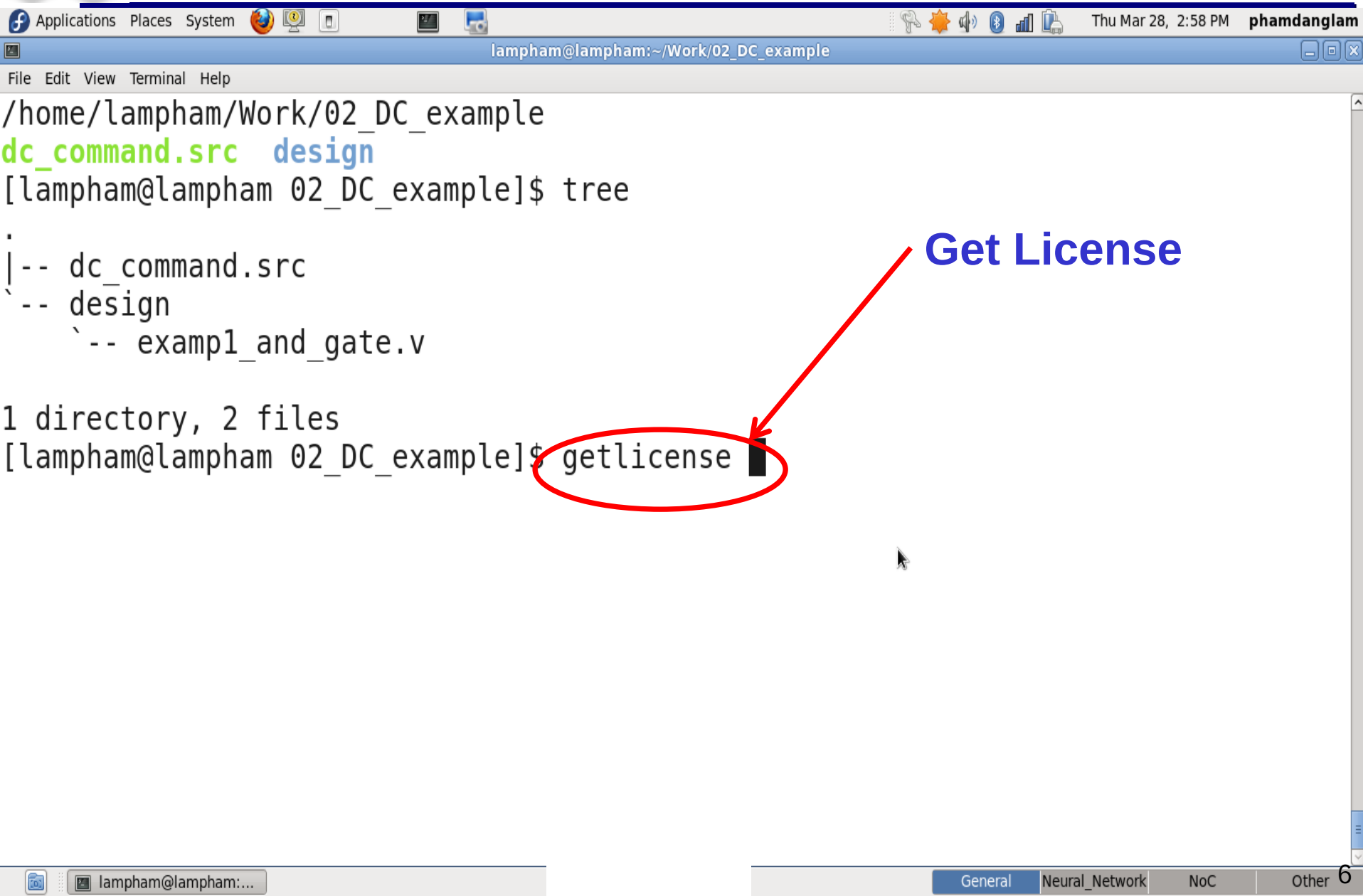
File Edit View Terminal Help

```
#!/bin/bash

set search_path "/home/lampham/synopsys/library/TSMC_65nm/aci/sc-ad12/synopsys"
set osearch_path [ concat $search_path \
                 ]

set target_library "scadv12_cln65lp_hvt_ff_1p32v_0c.db"
set link_library "* $target_library"
set synthesis_library standard.sldb

analyze -format verilog "/home/lampham/Work/02_DC_example/design/examp1_and_gate.v"
elaborate examp1_and_gate
current_design examp1_and_gate

create_clock -name clk -period 2 {system_clock}
set_input_delay 1 -clock clk [all_inputs]
set_output_delay 1 -clock clk [all_outputs]

compile -ungroup_all

report_area
report_timing
report_constraint
write -f ddc -o examp1_and_gate.ddc
write -format verilog -hierarchy -output new_examp1_and_gate.v
write_sdf examp1_and_gate.sdf

quit
~
~
~
~
~
~
~
~
~
~
:wq
```

Save & Quit

lampham@lampham:... [Mozilla Firefox] lampham@lampham:... lampham@lampham:~

Using DC Tool In Command Mode



Using DC Tool In Command Mode

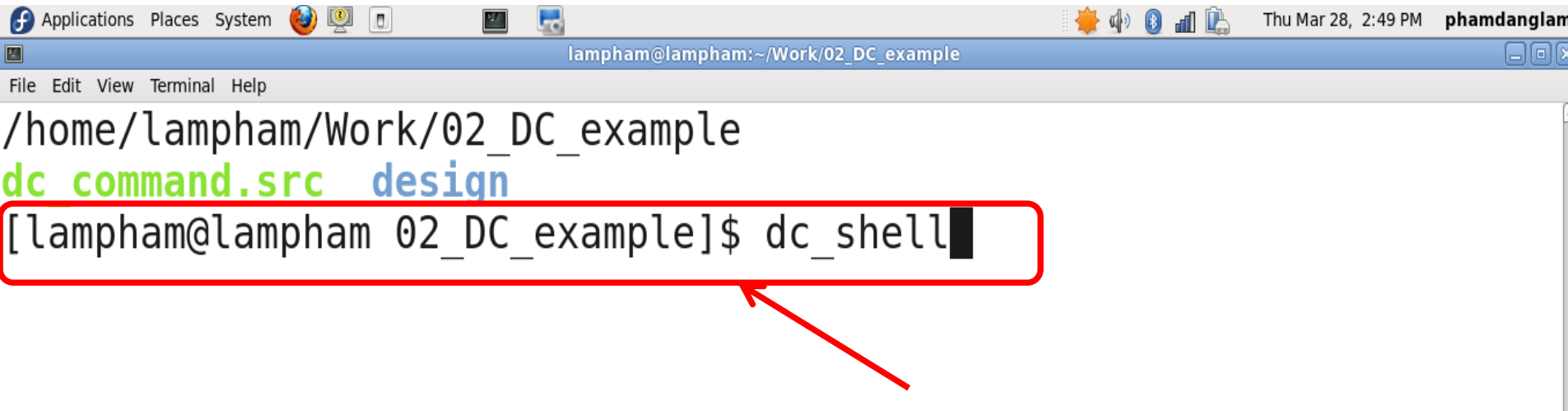
Applications Places System Thu Mar 28, 2:58 PM phamdanglam

lampham@lampham:~/Work/02_DC_example

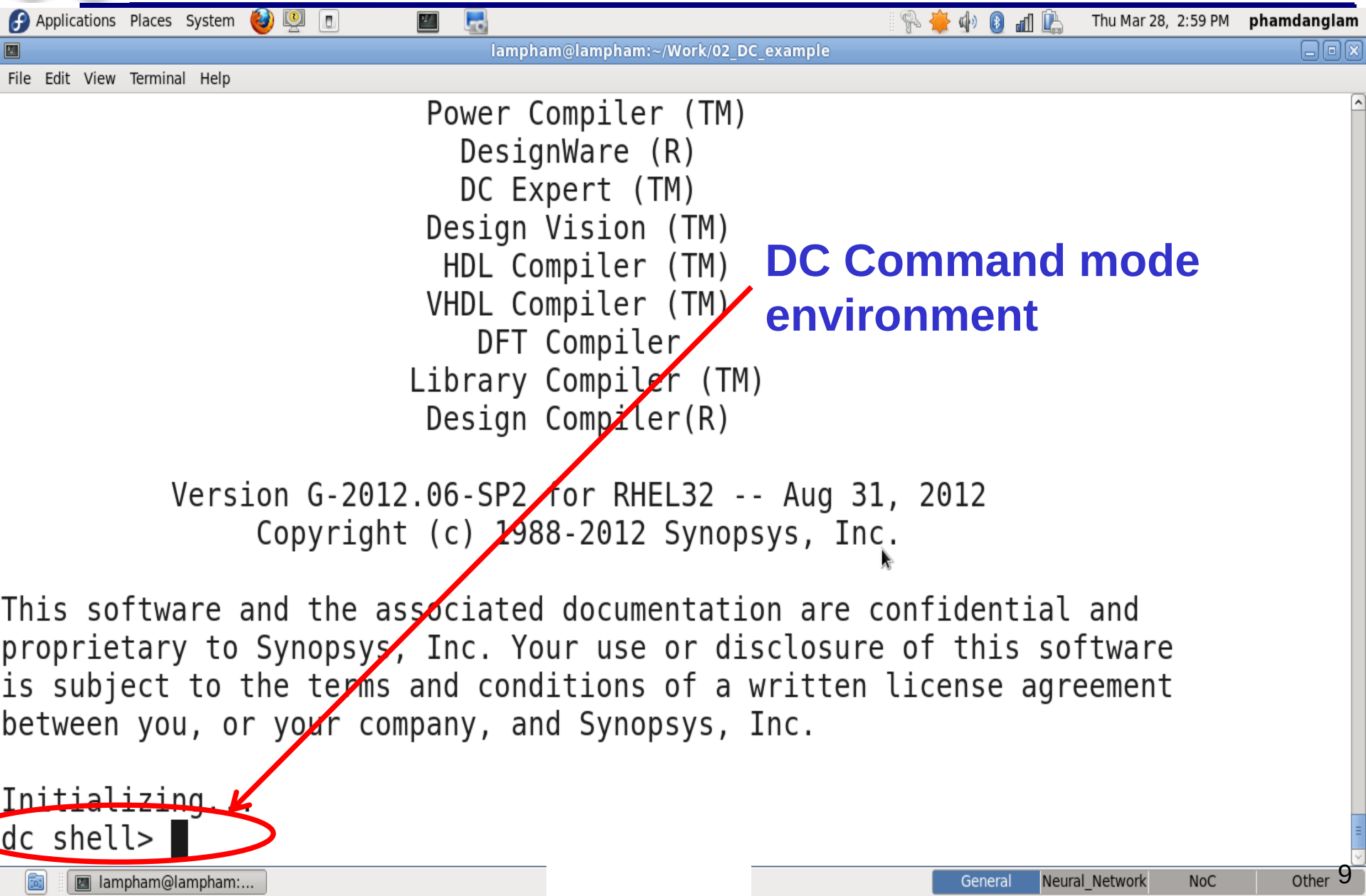
File Edit View Terminal Help

```
Users of ALTGEN2:  (Uncounted, node-locked)

Users of amat-calib_all:  (Uncounted, node-locked)

Users of amga:  (Uncounted, node-locked)

Users of amps:  (Uncounted, node-locked)

Users of amps/cso:  (Uncounted, node-locked)

Users of amps/pfx:  (Uncounted, node-locked)

Users of amps/tr:  (Uncounted, node-locked)

Users of AN-Impl3D_all:  (Uncounted, node-locked)

Users of any_technology:  (Uncounted, node-locked)

[lampham@lampham 02_DC_example]$
```

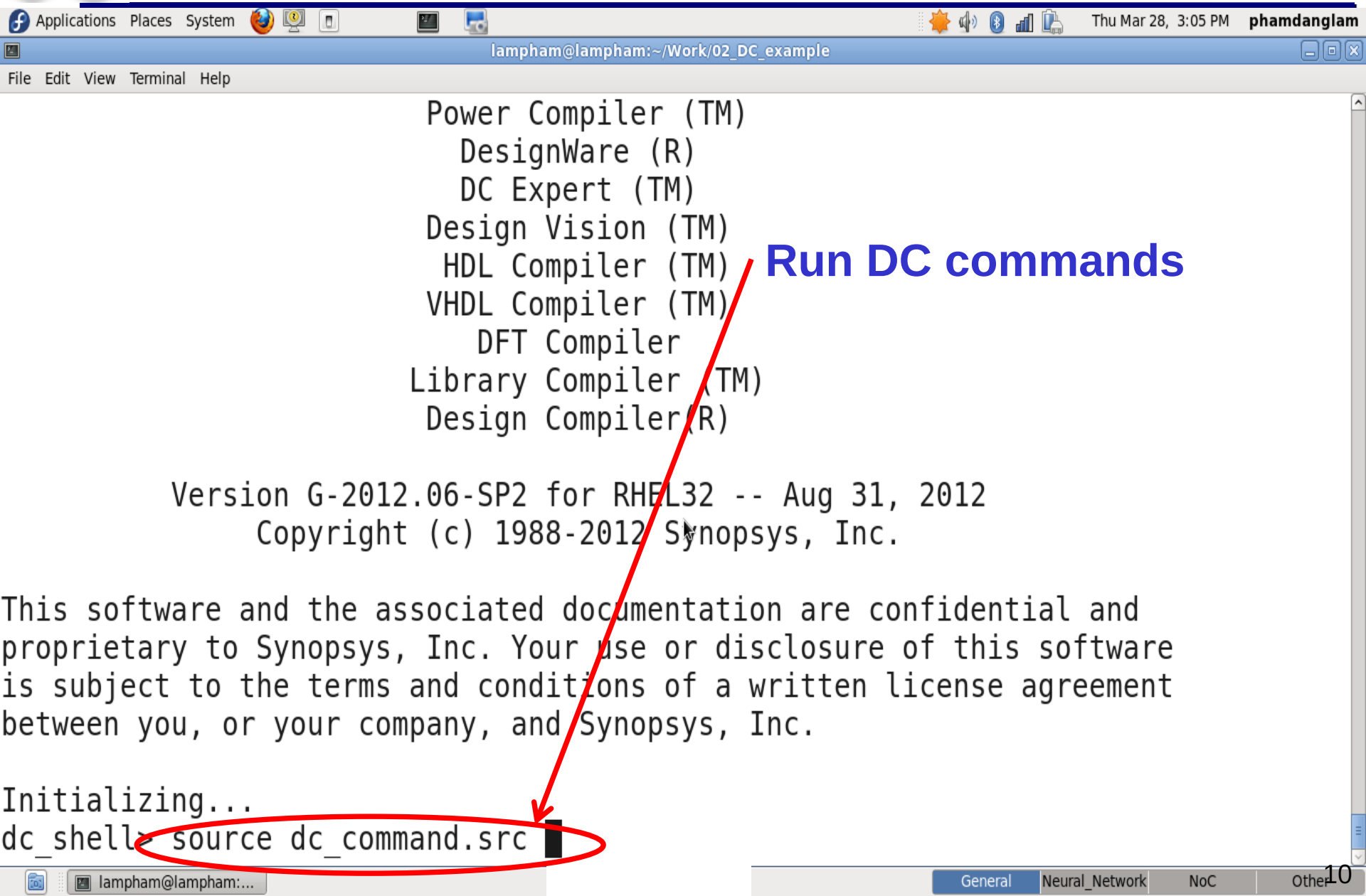
Using DC Tool In Command Mode



Using DC Tool In Command Mode



Using DC Tool In Command Mode



Using DC Tool In Command Mode

Applications Places System Thu Mar 28, 3:09 PM phamdanglam

lampham@lampham:~/Work/02_DC_example

File Edit View Terminal Help

```
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between you, or your company, and Synopsys, Inc.

Initializing...
dc_shell> source dc_command.src
Running PRESTO HDLC
Compiling source file /home/lampham/Work/02_DC_example/design/examp1_and_gate.v
Presto compilation completed successfully.
Loading db file '/home/lampham/synopsys/library/TSMC_65nm/aci/sc-ad12/synopsys/
scadv12_cln65lp_hvt_ff_1p32v_0c.db'
Loading db file '/home/lampham/synopsys/DC-2012.06-SP2/libraries/syn/gtech.db'
Loading db file '/home/lampham/synopsys/DC-2012.06-SP2/libraries/syn/standard.s
ldb'
  Loading link library 'scadv12_cln65lp_hvt_ff_1p32v_0c'
  Loading link library 'gtech'
Running PRESTO HDLC

Inferred memory devices in process
        in routine examp1_and_gate line 35 in file
                '/home/lampham/Work/02_DC_example/design/examp1_and_gate.v'.
```

lampham@lampham:... General Neural_Network NoC Other

Using DC Tool In Command Mode

Applications Places System Thu Mar 28, 3:10 PM phamdanglam

lampham@lampham:~/Work/02_DC_example

File Edit View Terminal Help

report_area

```
Report : area
Design : examp1_and_gate
Version: G-2012.06-SP2
Date   : Thu Mar 28 15:09:08 2013
********************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    scadv12_cln65lp_hvt_ff_1p32v_0c (File: /home/lampham/synopsys/library/TSMC_
65nm/aci/sc-ad12/synopsys/scadv12_cln65lp_hvt_ff_1p32v_0c.db)

Number of ports:                           26
Number of nets:                            35
Number of cells:                           17
Number of combinational cells:              9
Number of sequential cells:                 8
Number of macros:                           0
Number of buf/inv:                          1
Number of references:                       3

Combinational area:         24.480001
Buf/Inv area:                1.440000
Noncombinational area:      96.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:           120.480001
Total area:                 undefined
```

lampham@lampham:... General Neural_Network NoC Other

Using DC Tool In Command Mode

Applications Places System — Thu Mar 28, 3:11 PM — phamdanglam

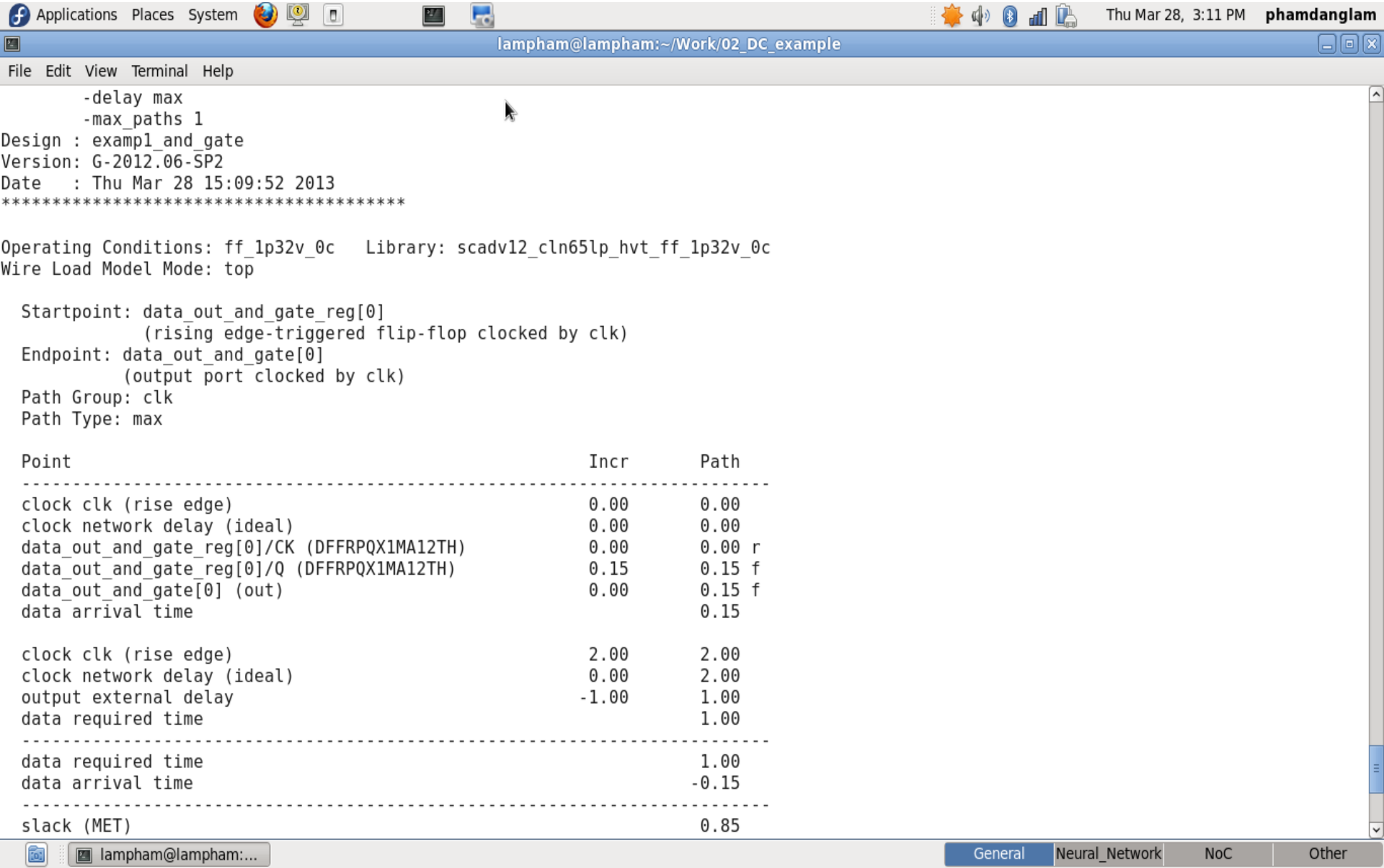
lampham@lampham:~/Work/02_DC_example

File Edit View Terminal Help

```
****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
Design : examp1_and_gate
Version: G-2012.06-SP2
Date   : Thu Mar 28 15:09:52 2013
****************************************

Operating Conditions: ff_1p32v_0c   Library: scadv12_cln65lp_hvt_ff_1p32v_0c
Wire Load Model Mode: top

  Startpoint: data_out_and_gate_reg[0]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: data_out_and_gate[0]
            (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                                    Incr       Path
  -----------------------------------------------------------------------------
  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              0.00       0.00
  data_out_and_gate_reg[0]/CK (DFFRPQX1MA12TH)             0.00       0.00 r
  data_out_and_gate_reg[0]/Q (DFFRPQX1MA12TH)              0.15       0.15 f
  data_out_and_gate[0] (out)                               0.00       0.15 f
  data arrival time                                                   0.15
```

report_timing

Using DC Tool In Command Mode



DC Tools

Applications Places System Thu Mar 28, 3:13 PM phamdanglam

lampham@lampham:~/Work/02_DC_example

File Edit View Terminal Help

```
/home/lampham/Work/02_DC_example
command.log      design                examp1_and_gate.sdf          new_examp1_and_gate.v
dc_command.src   examp1_and_gate.ddc   examp1_and_gate-verilog.pvl
default.svf      EXAMP1_AND_GATE.mr    examp1_and_gate-verilog.syn
[lampham@lampham 02_DC_example]$ ll
total 244
-rw-rw-r--. 1 lampham lampham 176245 Mar 28 15:13 command.log
-rwxrwxr-x. 1 lampham lampham    762 Mar 28 15:12 dc_command.src
-rw-rw-r--. 1 lampham lampham   9216 Mar 28 15:13 default.svf
drwxrwxr-x. 2 lampham lampham   4096 Mar 28 14:40 design
-rw-rw-r--. 1 lampham lampham  22528 Mar 28 15:13 examp1_and_gate.ddc
-rw-rw-r--. 1 lampham lampham     23 Mar 28 15:13 EXAMP1_AND_GATE.mr
-rw-rw-r--. 1 lampham lampham  12231 Mar 28 15:13 examp1_and_gate.sdf
-rw-rw-r--. 1 lampham lampham   3700 Mar 28 15:13 examp1_and_gate-verilog.pvl
-rw-rw-r--. 1 lampham lampham    340 Mar 28 15:13 examp1_and_gate-verilog.syn
-rw-rw-r--. 1 lampham lampham   2321 Mar 28 15:13 new_examp1_and_gate.v
[lampham@lampham 02_DC_example]$
```

Netlist file

lampham@lampham:...

General Neural_Network NoC Other

DC Tools

Applications Places System Thu Mar 28, 3:14 PM phamdanglam

lampham@lampham:~/Work/02_DC_example

File Edit View Terminal Help

```
module examp1_and_gate ( system_clock, system_rst_n, fist_data_in,
        second_data_in, data_out_and_gate );
  input [7:0] fist_data_in;
  input [7:0] second_data_in;
  output [7:0] data_out_and_gate;
  input system_clock, system_rst_n;
  wire   n1;
  wire   [7:0] pre_data_out_and_gate;

  DFFRPQX1MA12TH \data_out_and_gate_reg[7]  ( .D(pre_data_out_and_gate[7]),
        .CK(system_clock), .R(n1), .Q(data_out_and_gate[7]) );
  DFFRPQX1MA12TH \data_out_and_gate_reg[6]  ( .D(pre_data_out_and_gate[6]),
        .CK(system_clock), .R(n1), .Q(data_out_and_gate[6]) );
  DFFRPQX1MA12TH \data_out_and_gate_reg[5]  ( .D(pre_data_out_and_gate[5]),
        .CK(system_clock), .R(n1), .Q(data_out_and_gate[5]) );
  DFFRPQX1MA12TH \data_out_and_gate_reg[4]  ( .D(pre_data_out_and_gate[4]),
        .CK(system_clock), .R(n1), .Q(data_out_and_gate[4]) );
  DFFRPQX1MA12TH \data_out_and_gate_reg[3]  ( .D(pre_data_out_and_gate[3]),
        .CK(system_clock), .R(n1), .Q(data_out_and_gate[3]) );
  DFFRPQX1MA12TH \data_out_and_gate_reg[2]  ( .D(pre_data_out_and_gate[2]),
        .CK(system_clock), .R(n1), .Q(data_out_and_gate[2]) );
"new_examp1_and_gate.v" 45L, 2321C                          18,1          Top
```

DFF cell

lampham@lampham:...

General Neural_Network NoC Other

Using DC Tool In Command Mode

Applications Places System Thu Mar 28, 3:13 PM phamdanglam

lampham@lampham:~/Work/02_DC_example

File Edit View Terminal Help

```
/home/lampham/Work/02_DC_example
command.log      design                examp1_and_gate.sdf          new_examp1_and_gate.v
dc_command.src   examp1_and_gate.ddc   examp1_and_gate-verilog.pvl
default.svf      EXAMP1_AND_GATE.mr    examp1_and_gate-verilog.syn
[lampham@lampham 02_DC_example]$ ll
total 244
-rw-rw-r--. 1 lampham lampham 176245 Mar 28 15:13 command.log
-rwxrwxr-x. 1 lampham lampham    762 Mar 28 15:12 dc_command.src
-rw-rw-r--. 1 lampham lampham   9216 Mar 28 15:13 default.svf
drwxrwxr-x. 2 lampham lampham   4096 Mar 28 14:40 design
-rw-rw-r--. 1 lampham lampham  22528 Mar 28 15:13 examp1_and_gate.ddc
-rw-rw-r--. 1 lampham lampham     23 Mar 28 15:13 EXAMP1_AND_GATE.mr
-rw-rw-r--. 1 lampham lampham  12231 Mar 28 15:13 examp1_and_gate.sdf
-rw-rw-r--. 1 lampham lampham   3700 Mar 28 15:13 examp1_and_gate-verilog.pvl
-rw-rw-r--. 1 lampham lampham    340 Mar 28 15:13 examp1_and_gate-verilog.syn
-rw-rw-r--. 1 lampham lampham   2321 Mar 28 15:13 new_examp1_and_gate.v
[lampham@lampham 02_DC_example]$
```

SDF file

lampham@lampham:...

General Neural_Network NoC Other

Using DC Tool In Command Mode

Applications Places System Thu Mar 28, 3:13 PM phamdanglam

lampham@lampham:~/Work/02_DC_example

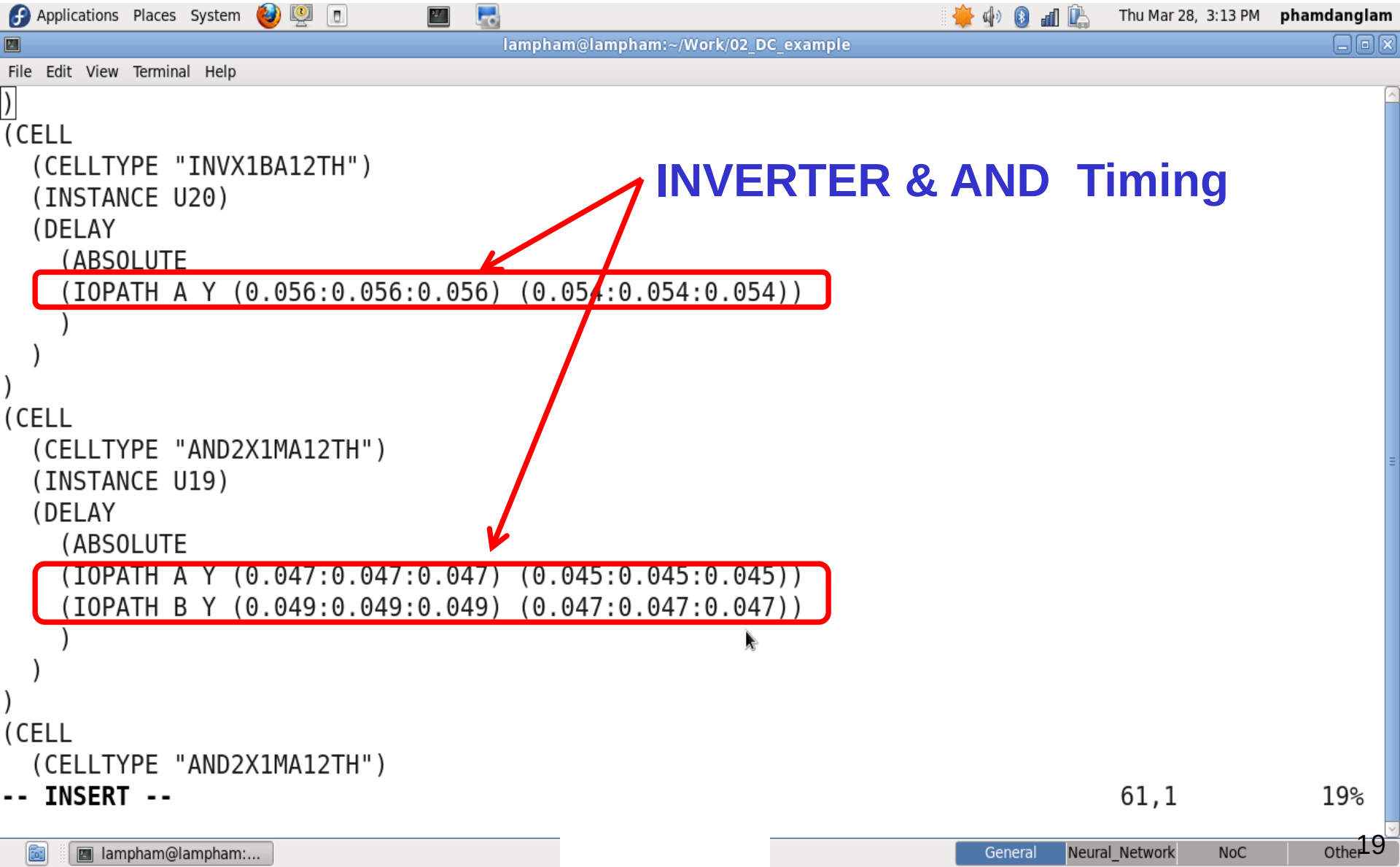
File Edit View Terminal Help

```
(DELAYFILmp1_and_gate.sdf
(SDFVERSION "OVI 2.1")
(DESIGN "examp1_and_gate")
(DATE "Thu Mar 28 15:13:15 2013")
(VENDOR "scadv12_cln65lp_hvt_ff_1p32v_0c")
(PROGRAM "Synopsys Design Compiler cmos")
(VERSION "G-2012.06-SP2")
(DIVIDER /)
(VOLTAGE 1.32:1.32:1.32)
(PROCESS "ff_1p32v_0c")
(TEMPERATURE 0.00:0.00:0.00)
(TIMESCALE 1ns)
(CELL
  (CELLTYPE "examp1_and_gate")
  (INSTANCE)
  (DELAY
    (ABSOLUTE
    (INTERCONNECT system_rst_n U20/A (0.000:0.000:0.000))
    (INTERCONNECT second_data_in[7] U19/A (0.000:0.000:0.000))
    (INTERCONNECT fist_data_in[7] U19/B (0.000:0.000:0.000))
    (INTERCONNECT second_data_in[6] U18/A (0.000:0.000:0.000))
    (INTERCONNECT fist_data_in[6] U18/B (0.000:0.000:0.000))
-- INSERT --                                              1,26          Top
```

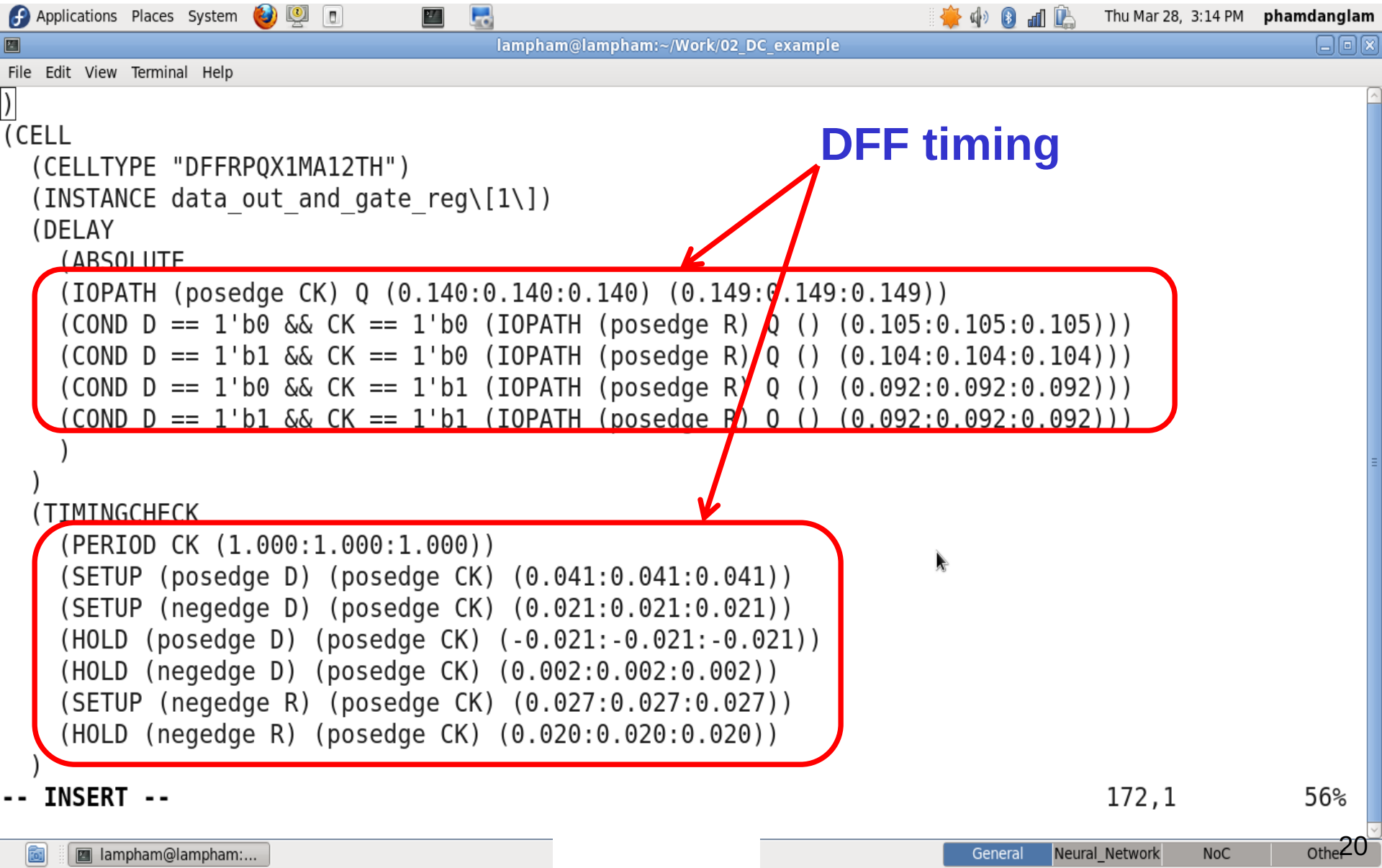
Interconnect

lampham@lampham:... General Neural_Network NoC Other

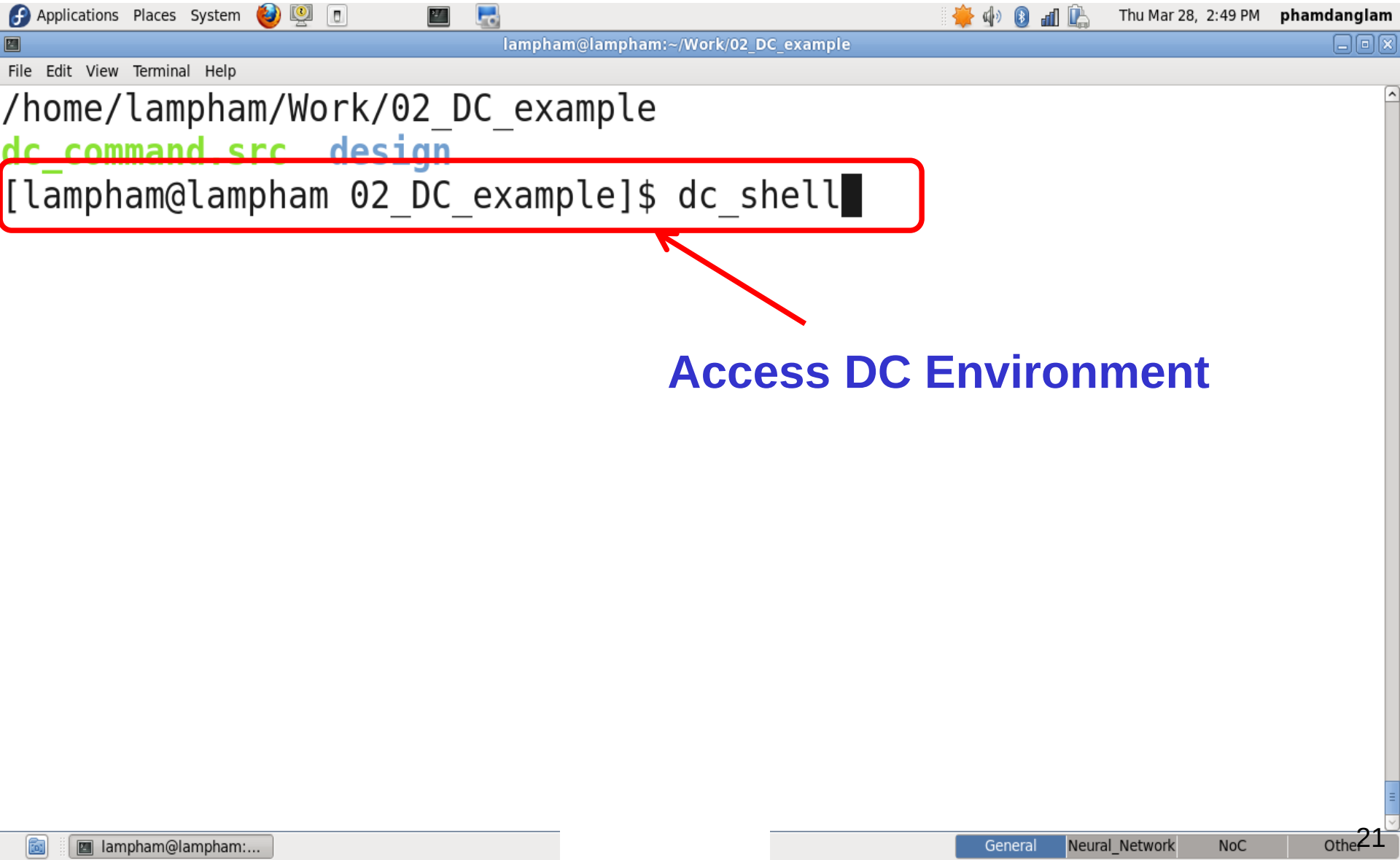
Using DC Tool In Command Mode



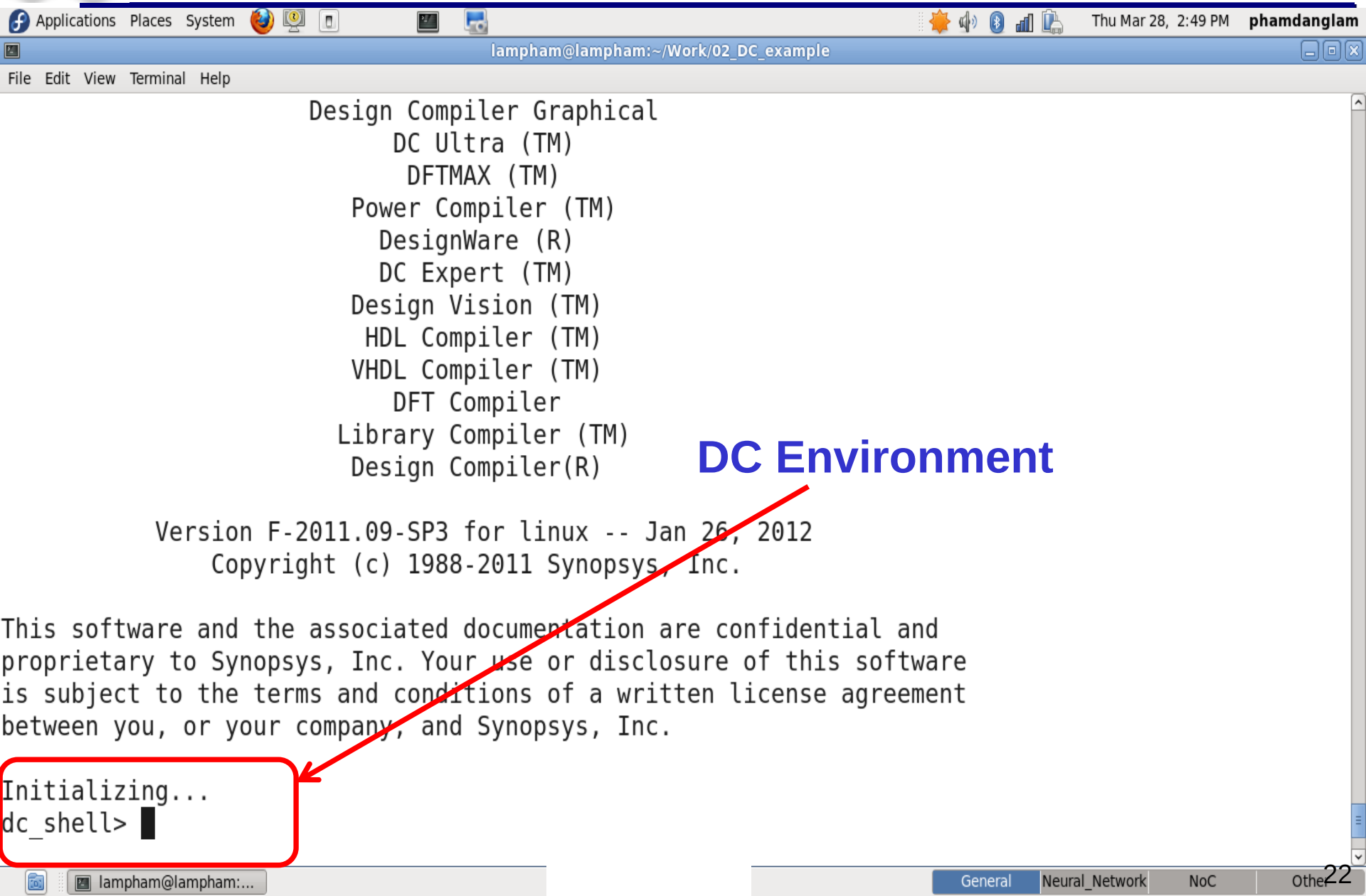
Using DC Tool In Command Mode



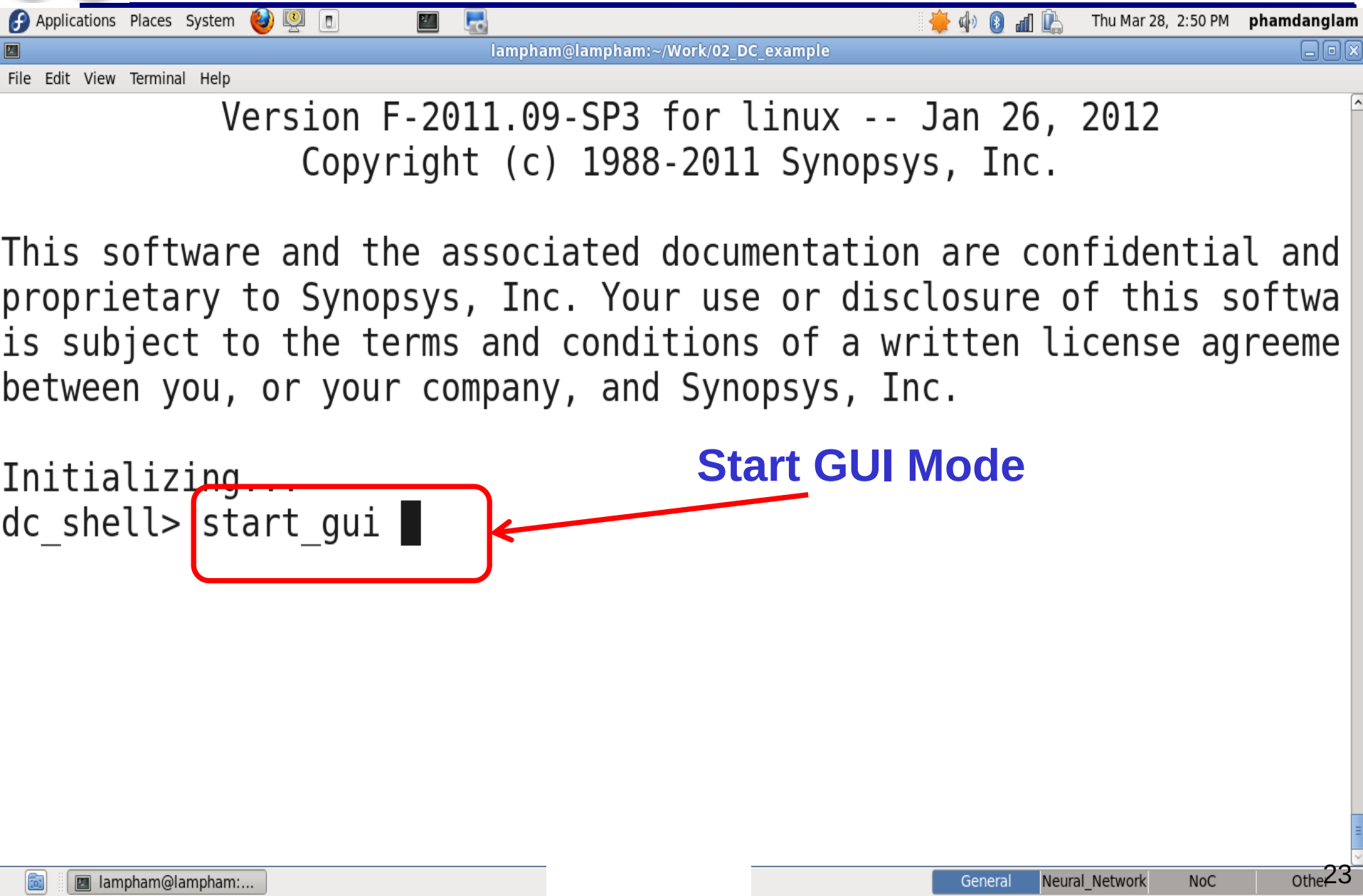
Using DC Tool In GUI Mode



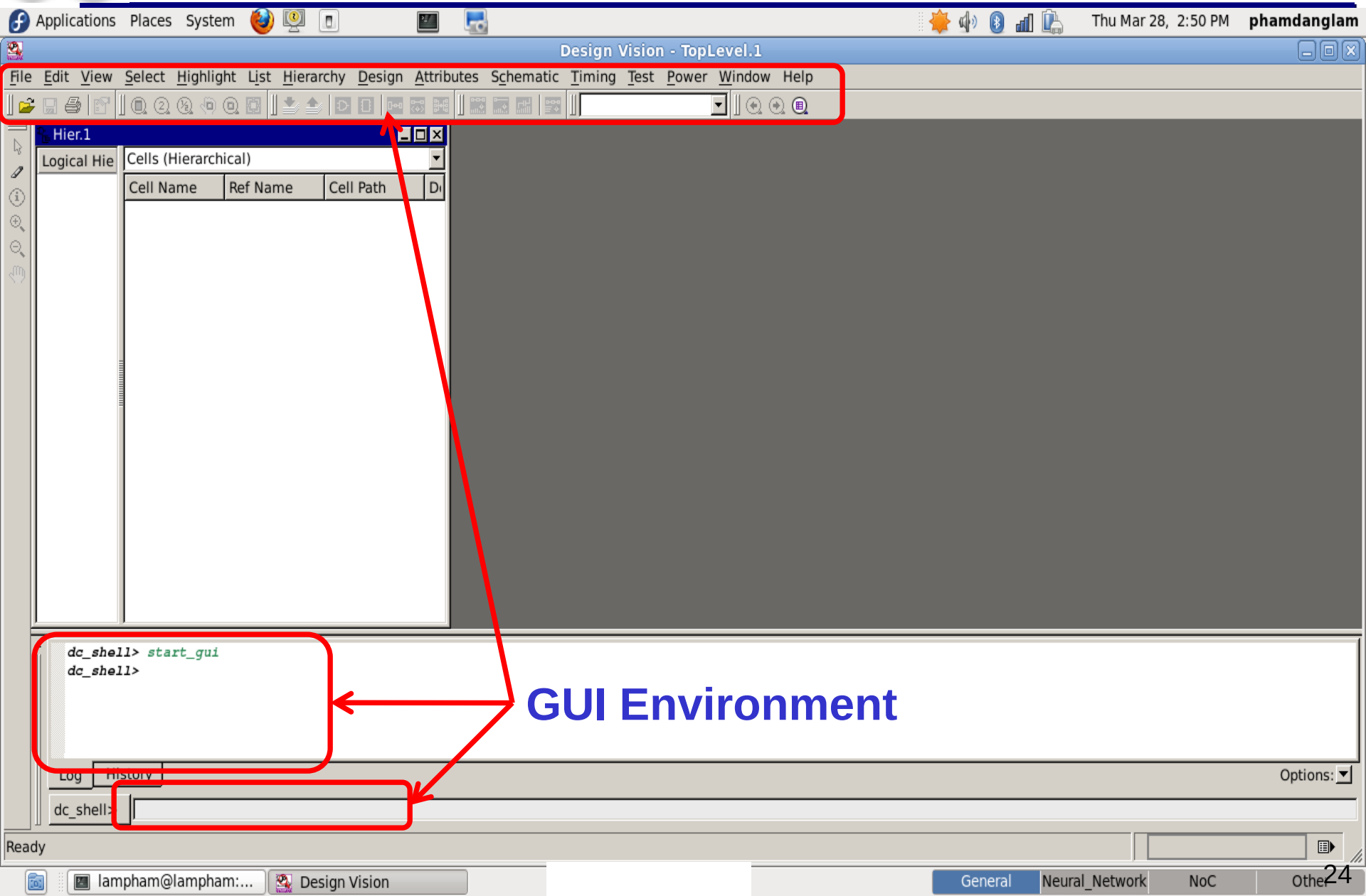
Using DC Tool In GUI Mode



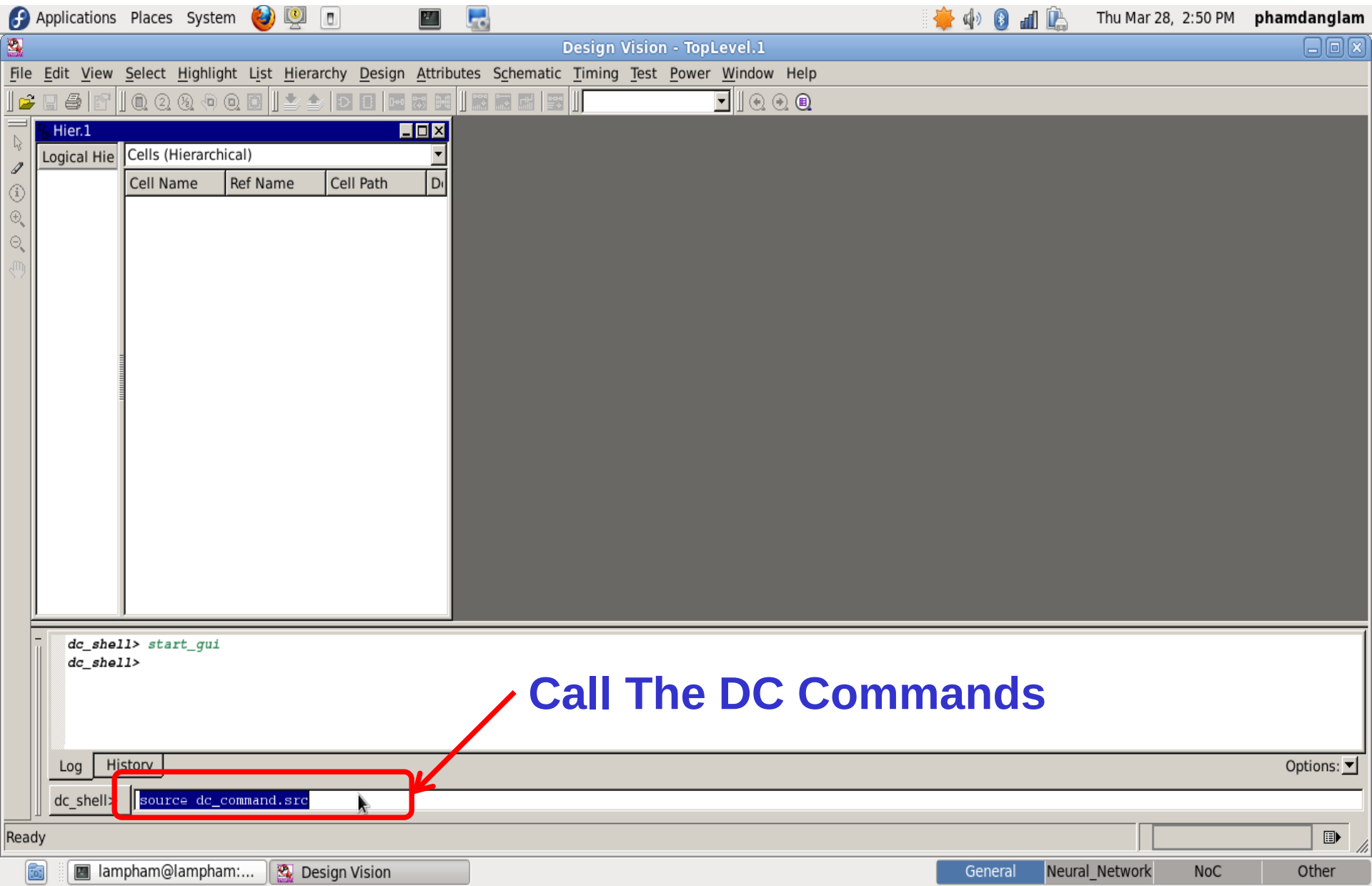
Using DC Tool In GUI Mode



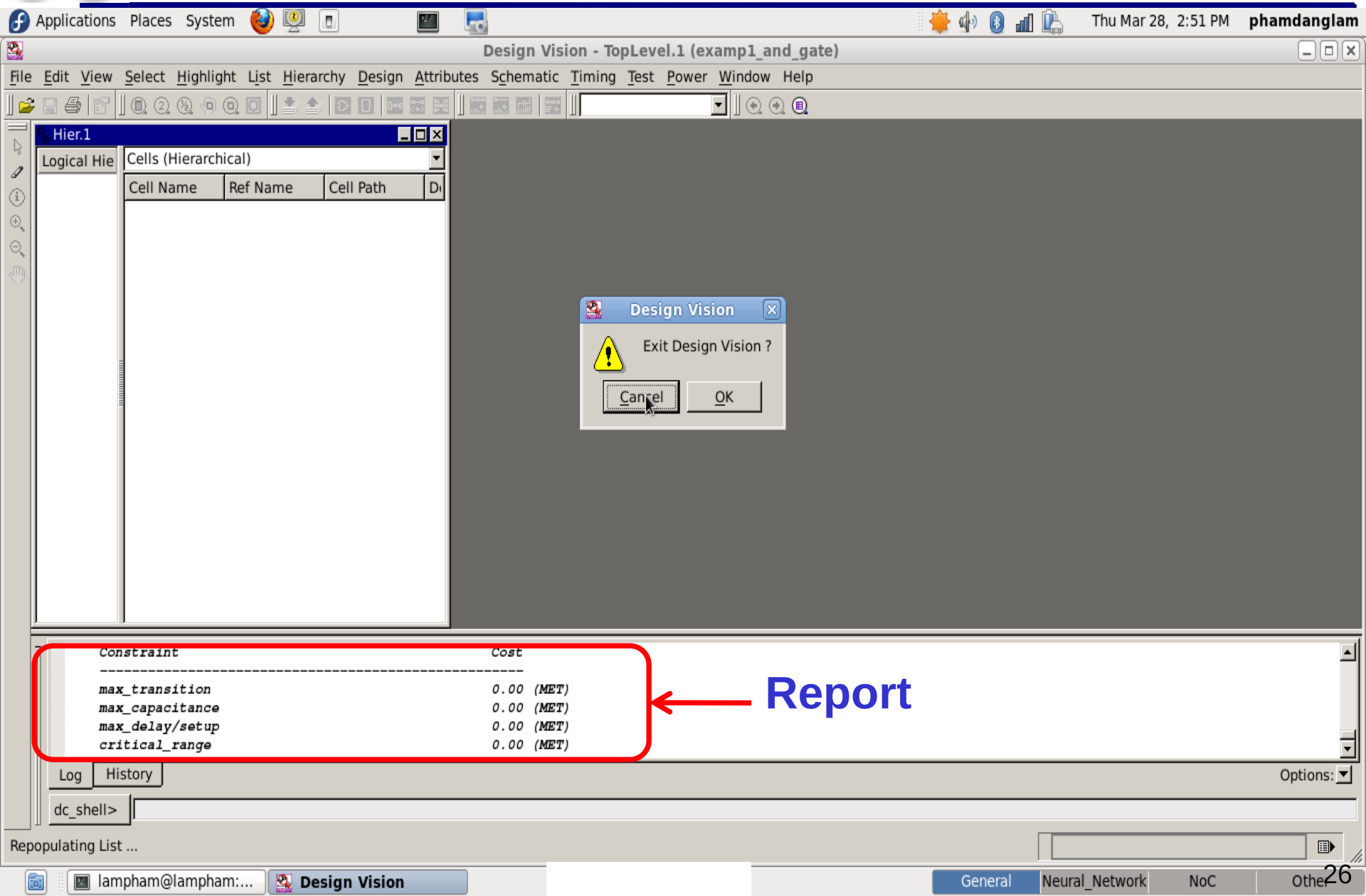
Using DC Tool In GUI Mode



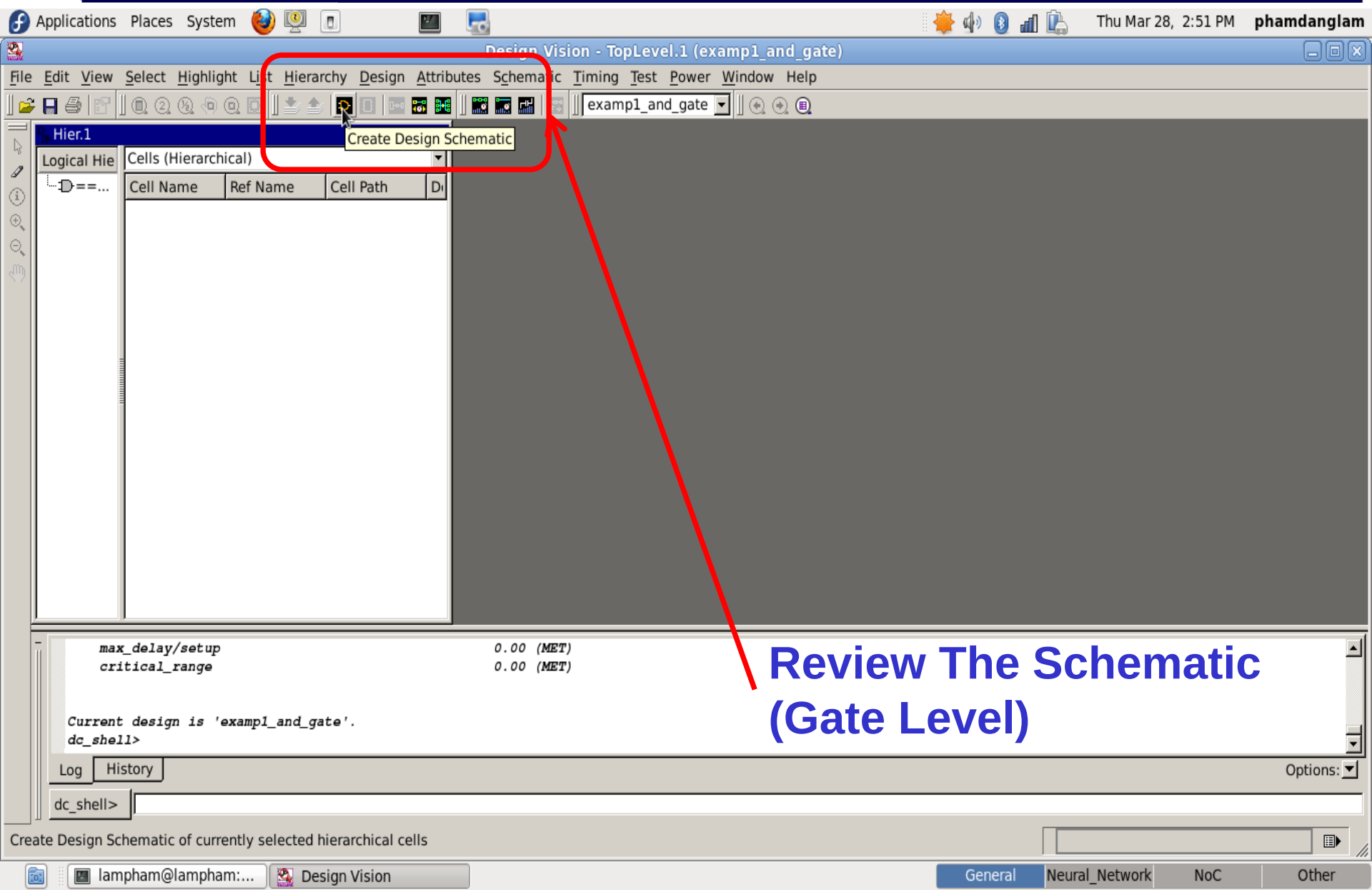
Using DC Tool In GUI Mode



Using DC Tool In GUI Mode

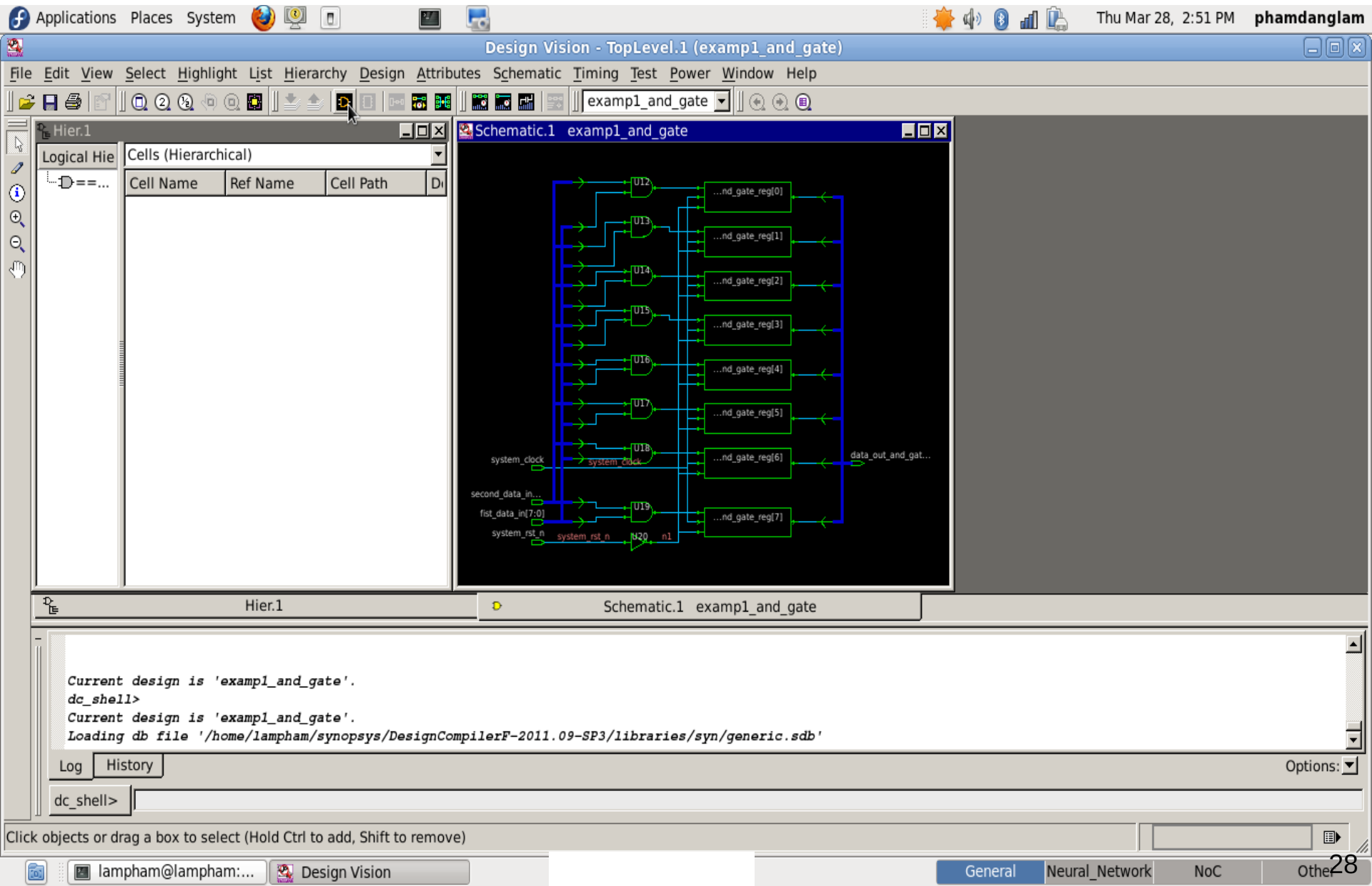


Using DC Tool In GUI Mode

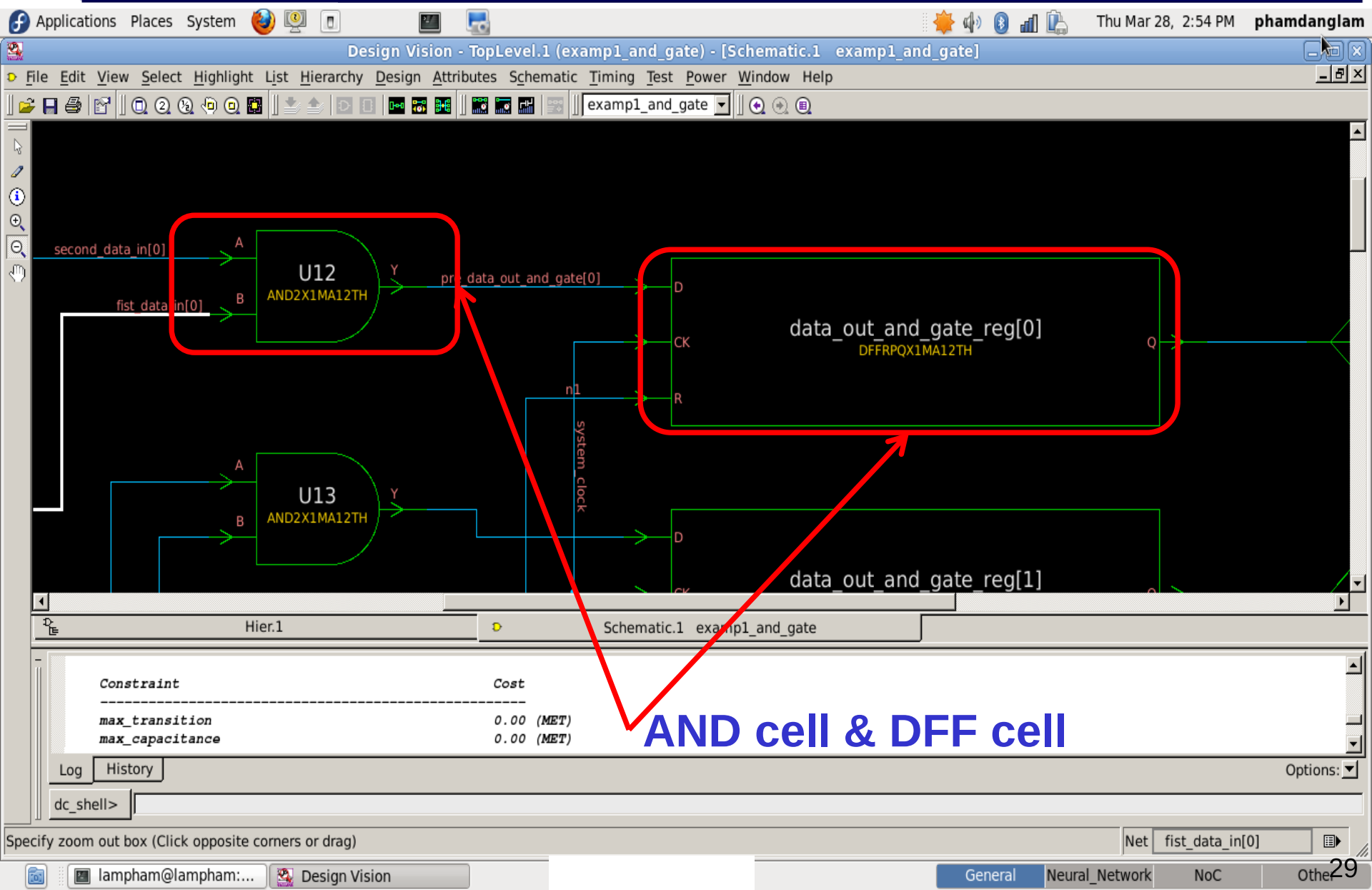


Review The Schematic (Gate Level)

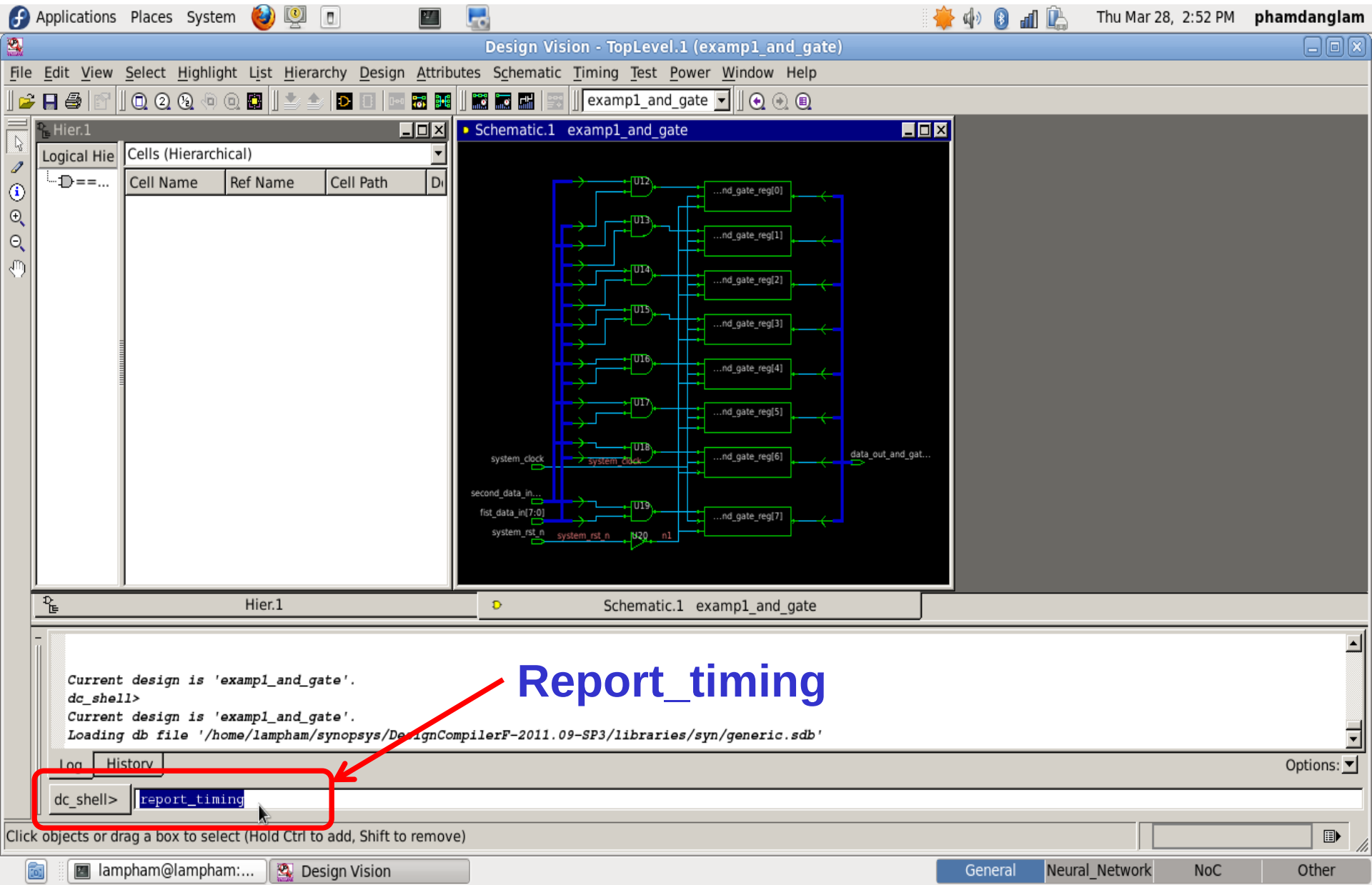
Using DC Tool In GUI Mode



Using DC Tool In GUI Mode



Using DC Tool In GUI Mode



Q & A