Lab 5: Verilog Language

1/ Read the following structures from Exercises carefully

2/ Using Verilog to implement all Exercises

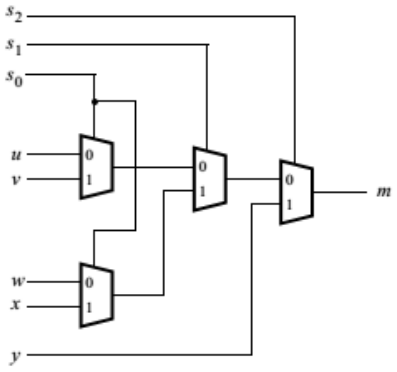
3/ Compose testbench as unit tests to cover main functions for every Exercise

- ➔ **Note: At least 20 test cases for every structures**
- ➔ **Note: Exercise 06 and 07 only need one test case → Endeavor presenting waveform**

4/ Students can refer three examples firstly to master how to compose source code, testbench as well as simulated environment

Exercise 01

1. **Requirement**: Develop the following hardware (for every figure) with Verilog HDL



a) Circuit

s_2	s_1	s_0	m
0	0	0	u
0	0	1	v
0	1	0	w
0	1	1	x
1	0	0	y
1	0	1	y
1	1	0	y
1	1	1	y

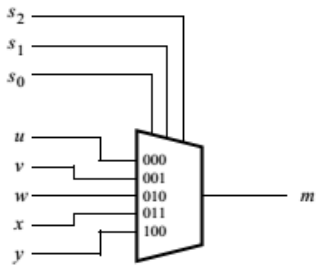


Figure 1.1 Multiplexer 5-1

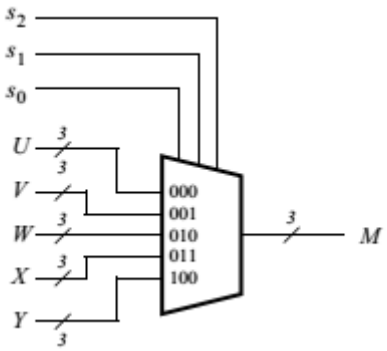


Figure 1.2 Ex_01 Design

Exercise 02

1. **Requirement**: Develop the following hardware with Verilog HDL

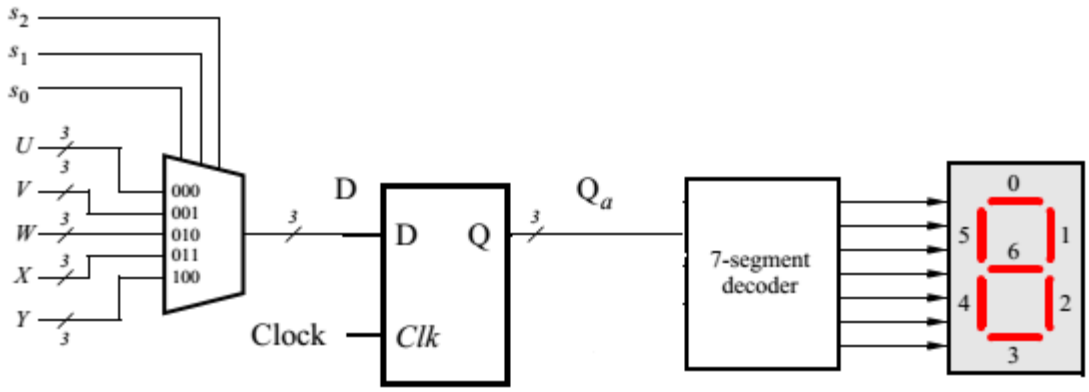


Figure 2.1 Ex_02 Design

Exercise 03

1. **Requirement**: Develop the following hardware with Verilog HDL

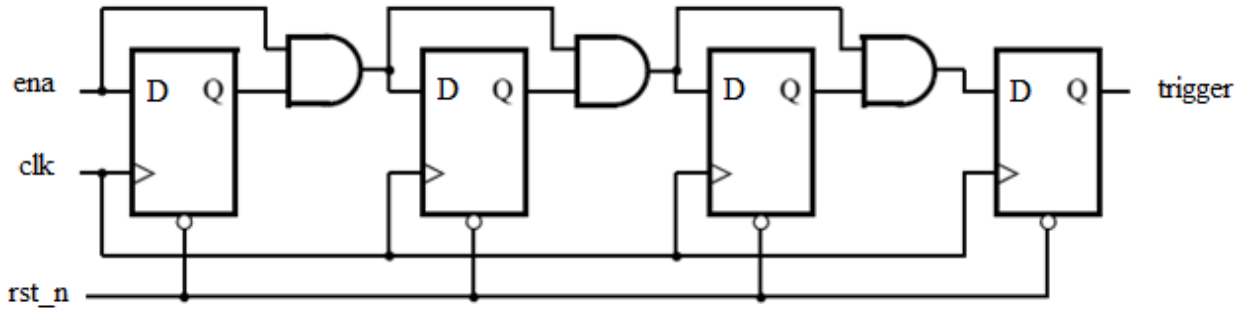


Figure 3.1 Ex_03 Design

Input: ena, clk, rst_n

Output: trigger

Exercise 04

1. **Requirement**: Develop the following hardware (4 bit Addition) with Verilog HDL

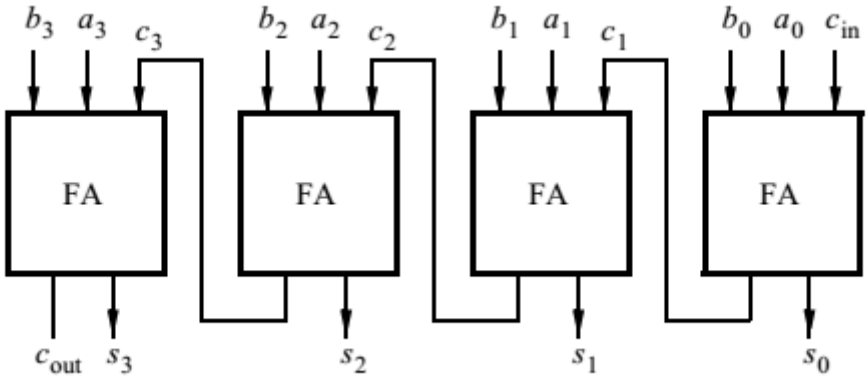


Figure 4.1 Ex_04 Design

Exercise 05

1. **Requirement**: Develop the following hardware (4 bit Multiplier) with Verilog HDL

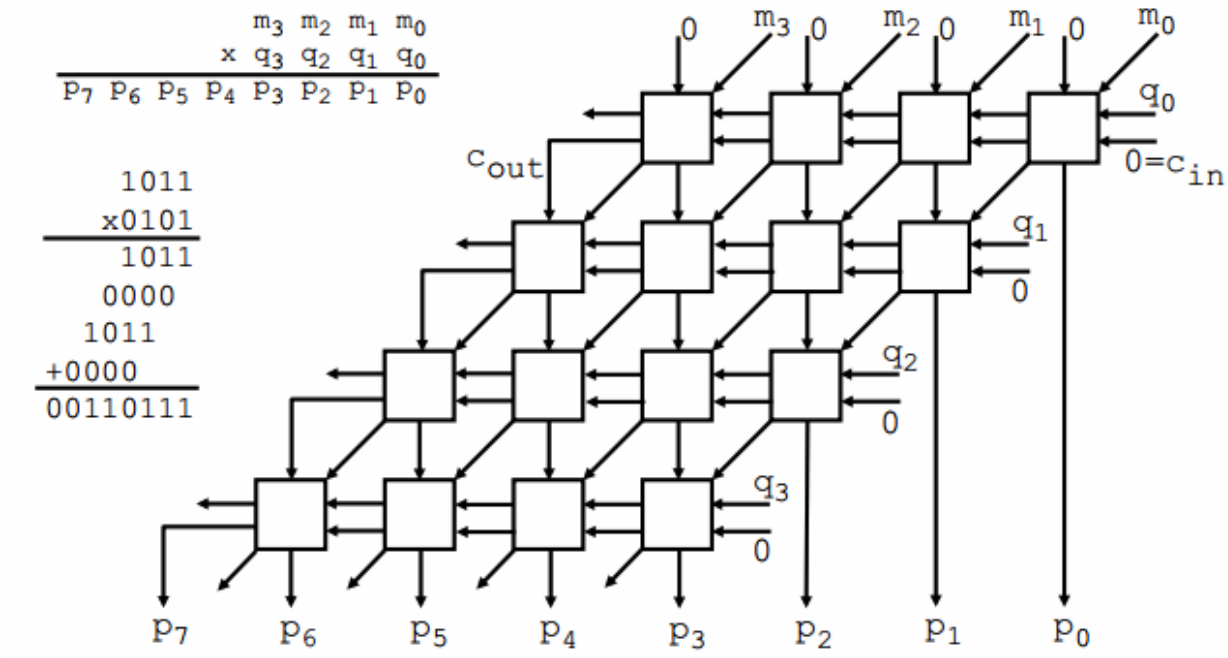


Figure 5.1 Ex_05 Design

Exercise 06

1. **Requirement**: Develop the following hardware (Simple State Machine) with Verilog HDL

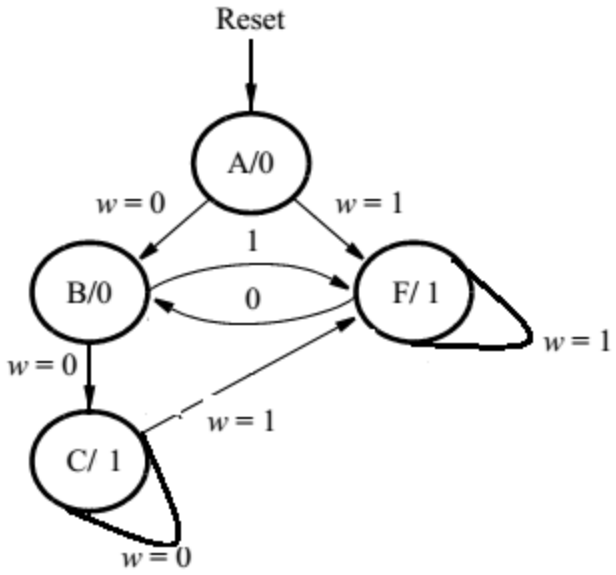


Figure 6.1 Ex_06 Design

Exercise 07

1. **Requirement**: Develop the following hardware (Complicated State Machine) with Verilog HDL

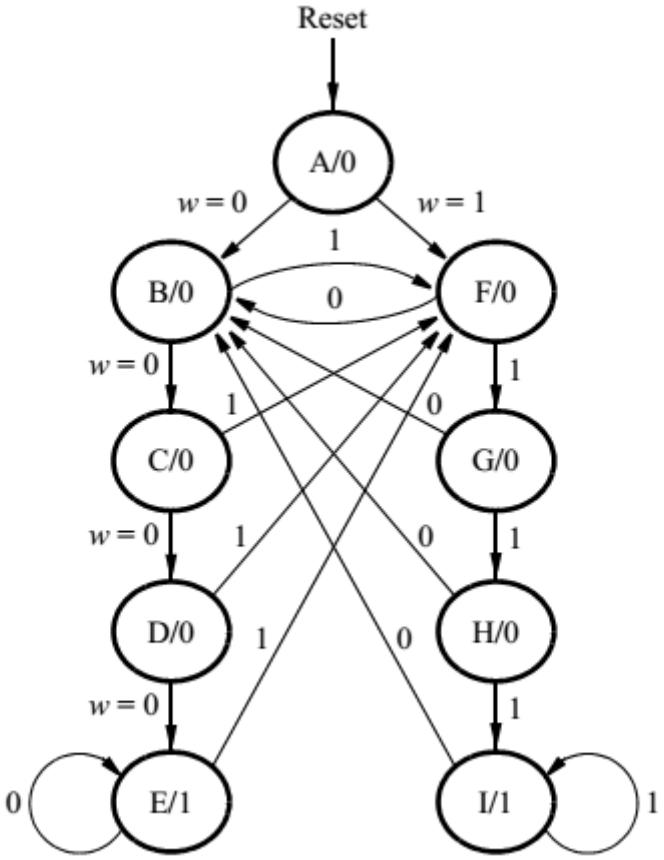


Figure 7.1 Ex_07 Design