Image Display Control

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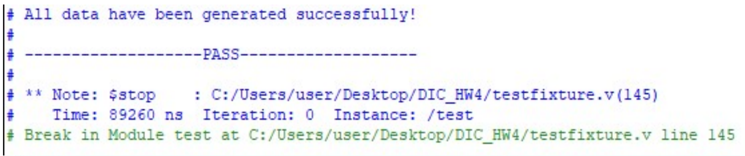
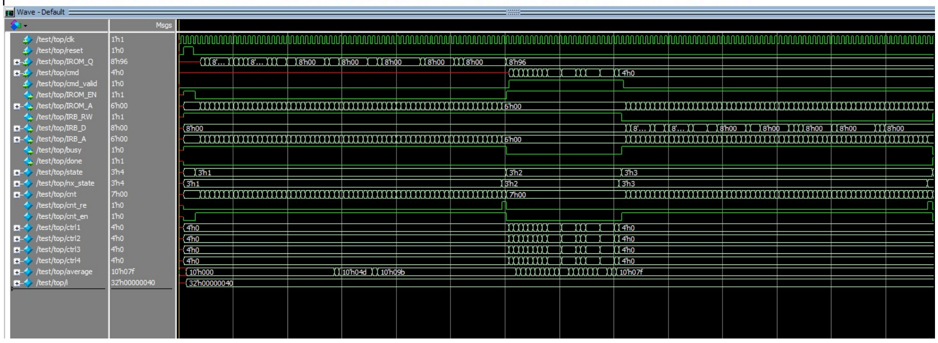
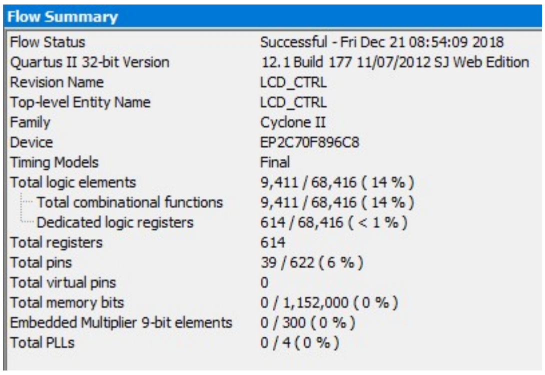
Pre-simulation(tb2):



```
# All data have been generated successfully!
#
# -------------------PASS-------------------
#
# ** Note: $stop    : C:/Users/user/Desktop/DIC_HW4/testfixture.v(145)
#    Time: 89260 ns  Iteration: 0  Instance: /test
# Break in Module test at C:/Users/user/Desktop/DIC_HW4/testfixture.v line 145
```

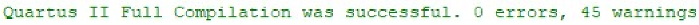


Synthesis by Quartus(tb2):



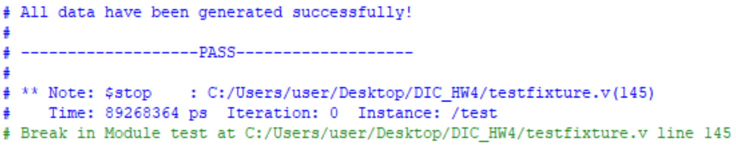
Flow Summary

Flow Status	Successful - Fri Dec 21 08:54:09 2018
Quartus II 32-bit Version	12.1 Build 177 11/07/2012 SJ Web Edition
Revision Name	LCD_CTRL
Top-level Entity Name	LCD_CTRL
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	9,411 / 68,416 (14 %)
Total combinational functions	9,411 / 68,416 (14 %)
Dedicated logic registers	614 / 68,416 (< 1 %)
Total registers	614
Total pins	39 / 622 (6 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

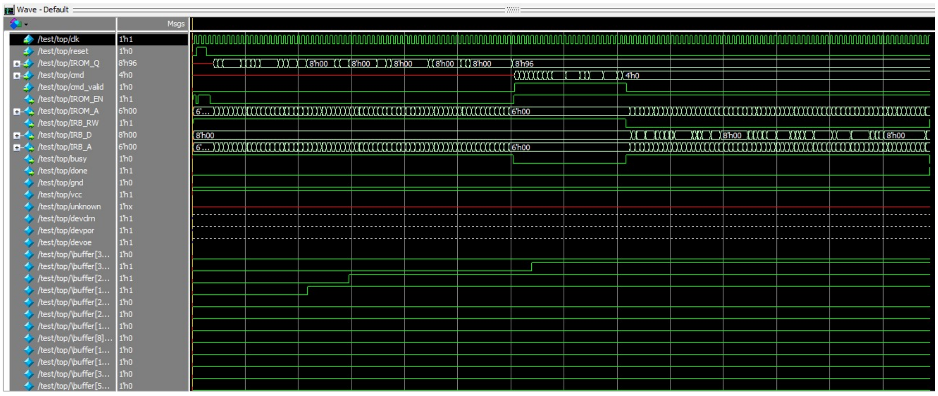


```
Quartus II Full Compilation was successful. 0 errors, 45 warnings
```

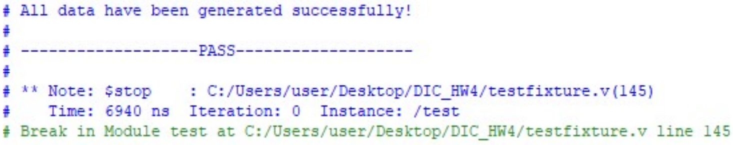
Post-simulation (tb2, cycle= 45):



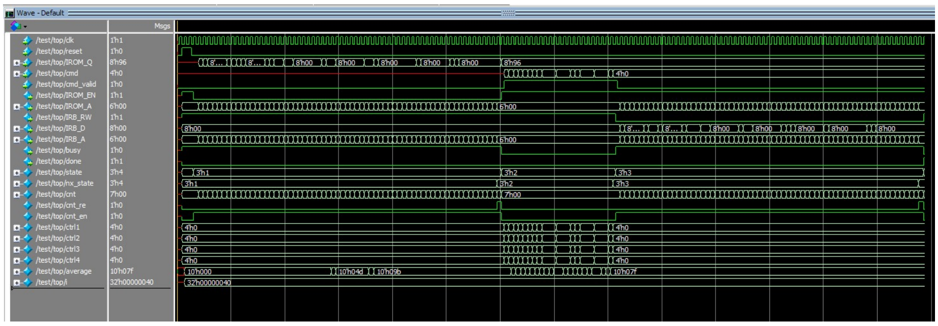
```
# All data have been generated successfully!
#
# -------------------PASS-------------------
#
# ** Note: $stop    : C:/Users/user/Desktop/DIC_HW4/testfixture.v(145)
#    Time: 89268364 ps  Iteration: 0  Instance: /test
# Break in Module test at C:/Users/user/Desktop/DIC_HW4/testfixture.v line 145
```



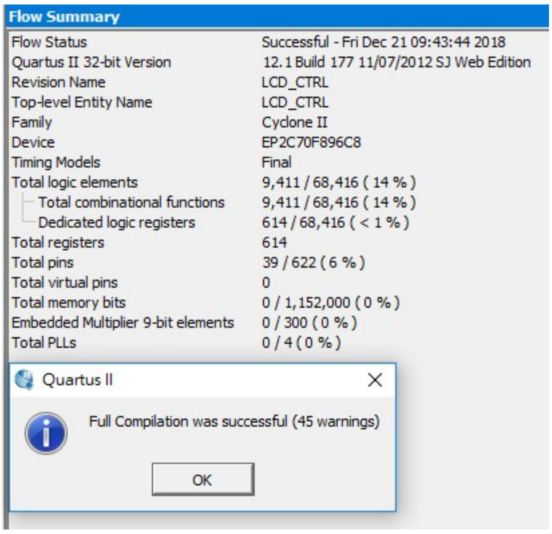
Pre-simulation(tb3):



```
# All data have been generated successfully!
#
# -------------------PASS-------------------
#
# ** Note: $stop    : C:/Users/user/Desktop/DIC_HW4/testfixture.v(145)
#    Time: 6940 ns  Iteration: 0  Instance: /test
# Break in Module test at C:/Users/user/Desktop/DIC_HW4/testfixture.v line 145
```



Synthesis by Quartus(tb3):



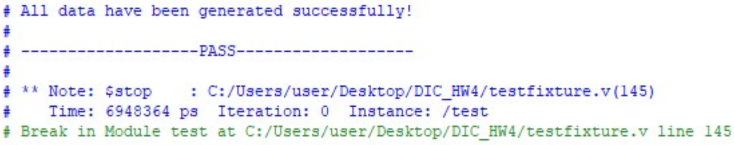
Flow Summary

Flow Status	Successful - Fri Dec 21 09:43:44 2018
Quartus II 32-bit Version	12.1 Build 177 11/07/2012 SJ Web Edition
Revision Name	LCD_CTRL
Top-level Entity Name	LCD_CTRL
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	9,411 / 68,416 (14 %)
Total combinational functions	9,411 / 68,416 (14 %)
Dedicated logic registers	614 / 68,416 (< 1 %)
Total registers	614
Total pins	39 / 622 (6 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

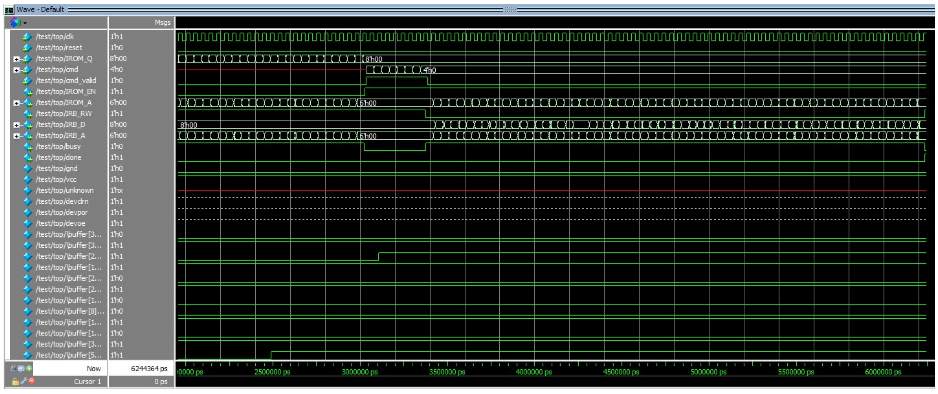
Quartus II

Full Compilation was successful (45 warnings)

Post-simulation (tb3, cycle= 45):



```
# All data have been generated successfully!
#
# -------------------PASS-------------------
#
# ** Note: $stop    : C:/Users/user/Desktop/DIC_HW4/testfixture.v(145)
#    Time: 6948364 ps  Iteration: 0  Instance: /test
# Break in Module test at C:/Users/user/Desktop/DIC_HW4/testfixture.v line 145
```



Clarification:

The results of all tb1, tb2 and tb3 are right, though I only put down the result images of tb2 and tb3.

Algorithm Explanation:

1. I implement the idea of finite state machine: 2c1s(2 combinational circuits and 1 sequential circuit), to describe the behaviour of controlling the transformation between different processes. There are five states in my design: initialization, read, operation, write and the end. Then, I describe the signals of six outputs in the combinational circuit of different states.
2. I use a counter during "read" and "write" states, and then let the address equal to the [5:0] bits of the counter. The sequence of data written out (IRB_D) is also depended on the number of counter.
3. Afterwards, I use 1 combinational circuit to assign different signals to the according command(cmd); two sequential circuits to fulfill the commands of moving the control point position ad dealing with the data inside the buffers.
4. 64 buffers are used to place the data read in for later use in the writing process.
5. It's said that the main design problem in this homework is the design of "shifting". However, I cannot come up with a better idea than using a multiplexor of 64 options, so I guess the area of my circuit will be very large.
6. Also, it's worth mentioning the problem of signed bit and unsigned bit, as this caused me some issues during the function of "decrease". Therefore, it's wiser to present the value in its full bits: 8 as 4'b1000.
7. Lastly, I got into some serious problem when I assigned the value of one signal in two or more always block. This even forced stop the ModelSim. Therefore, I believe this issue is the most precious lesson I learnt from this homework.

tags: `IC Design` `Image Display Control` `verilog` `finite state machine`