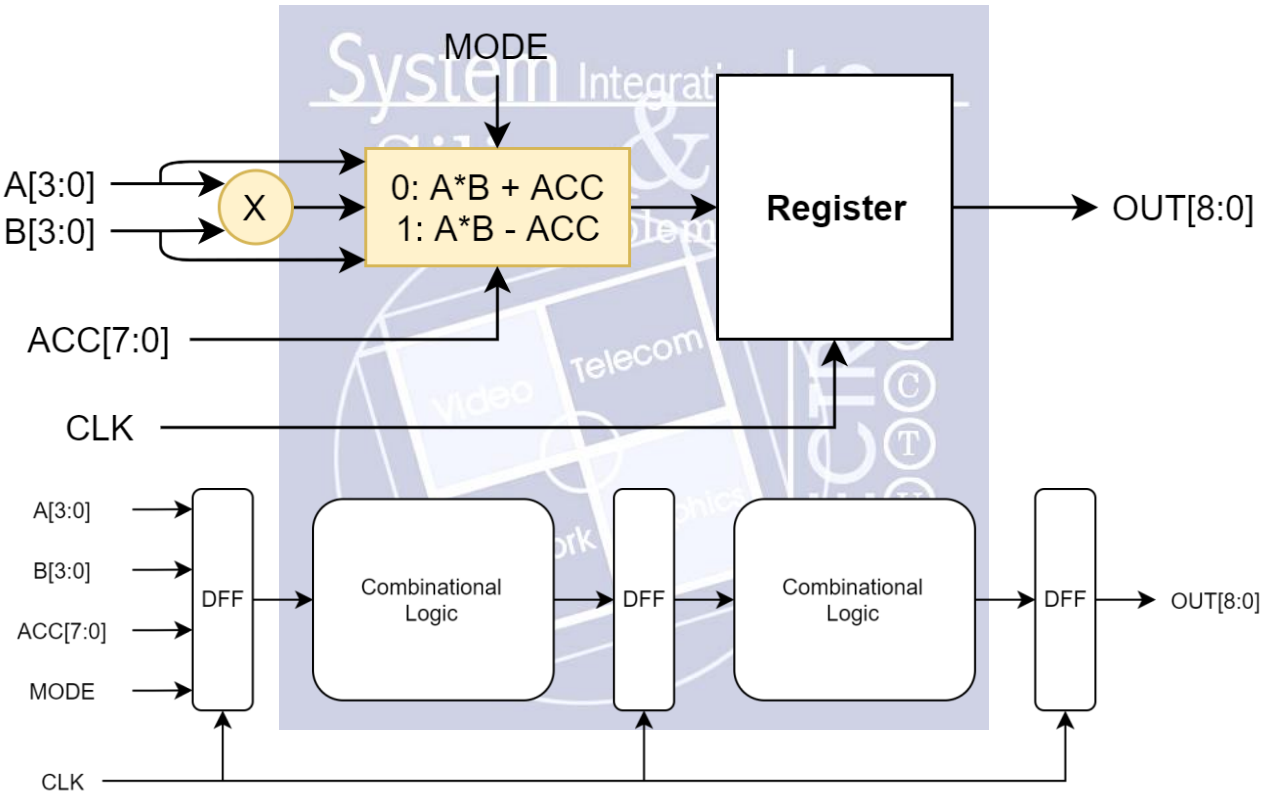
EE_VLSI_2019

Final Project: Full-Custom Design of a 4-bit Multiplier and Accumulator with Two-Mode

Due date: December 31st, 2019, 23:55 P.M.

I. Abstract

In this lab, you require designing a **4-bit MAC** with Two-Mode in full custom design. This document includes the specification and requirement of your design, and grading policy.



II. Specification

You should follow the names listed here.

* File name : **MAC4.sp**
* Subckt name : **MAC4**
* Input ports (signed) : **A[3:0], B[3:0], ACC[7:0], MODE, CLK**
* Output ports (signed) : **OUT[8:0]**

III. Requirement

a. You have to design your circuit through SPICE before layout at first. After successfully self-testing, you have to layout according to this spice code.

b. You should pass pre-simulation, DRC, LVS, and post-layout simulation successfully when you demo

c. You can employ all kinds of architectures to accomplish your design.

d. Inputs "A" and "B" are both of 4-bit **signed** numbers, "ACC" is 8-bit **signed** number and output "OUT" is 9-bit **signed** number.

e. HSPICE

1. Output loading of OUT[8:0] is 10fF
2. Supply voltage is 1.8 V
3. You may use your own working frequency (clock period can be adjusted by yourself).

f. LAYOUT

1. Design area is defined as the smallest rectangle which includes all layout, and the rectangle ratio must be requested between 2 ~ 0.5.
2. The metal width of **VDD & GND rails** should be designed as the same consideration of Midterm Project.

g. VERILOG (bonus)

1. You are asked to do a GATE LEVEL design. Behavior descriptions are NOT ALLOWED. The gate delay information is shown as Table I. The maximal input number to a gate is up to 4.

Table I

Gate Delay	Delay time (Tpr = Tpf)			
	1-input	**2-input**	**3-input**	**4-input**
NOT	0.3ns	-	-	-
AND	-	0.6ns	0.7ns	0.8ns
NAND	-	0.5ns	0.6ns	0.7ns
OR	-	0.6ns	0.7ns	0.8ns
NOR	-	0.5ns	0.6ns	0.7ns
XOR	-	0.7ns	0.8ns	0.9ns
XNOR	-	0.7ns	0.8ns	0.9ns

2. For convenience and error-prevention, TA has already constructed the gates with delay information in the file, "GATE_LIB.v." so you won't have to add the delay yourself. You should include GATE_LIB.v in your design and you can only use these gates from the table. The module name and its ports of the gates are listed in Table II.

Tabel II

Gate	Module Name	Port List
NOT	**VLSI_NOT**	(.OUT( ), .IN( ));
2-input AND	**VLSI_AND2**	(.OUT( ), .INA( ), .INB( ));
3-input AND	**VLSI_AND3**	(.OUT( ), .INA( ), .INB( ), INC( ));
4-input AND	**VLSI_AND4**	(.OUT( ), .INA( ), .INB( ), .INC( ), .IND( ));
2-input NAND	**VLSI_NAND2**	(.OUT( ), .INA( ), .INB( ));

…	**…**	…
2-input OR	**VLSI_OR2**	(.OUT( ), .INA( ), .INB( ));
…	**…**	…
2-input NOR	**VLSI_NOR2**	(.OUT( ), .INA( ), .INB( ));
…	**…**	…
2-input XOR	**VLSI_XOR2**	(.OUT( ), .INA( ), .INB( ));
…	**…**	…
2-input XNOR	**VLSI_XNOR2**	(.OUT( ), .INA( ), .INB( ));
…	**…**	…

Ex: call gate instance (C = A and B)

Syntax: VLSI_AND2 AandB(.OUT(C), .INA(A), INB(B));

Note: AandB is just an instance name. You can change the name to be any word except keywords.

3. The critical delay should not be longer than 20ns.
4. Type “ncverilog MAC4.v” to compile and “ncverilog +access+r TESTBED.v” to run simulation.

IV. Grading Policy

- Pre-sim with correct function (HSPICE)：15 %
- Layout：20 % (partial scoring)
- DRC：5 %
- LVS：5 %
- Post-sim with correct function (HSPICE)：10%
- Performance ranking：30 %
  - Speed (Pre-sim & Post-sim)：20%
  - Area (with correct DRC and LVS)：10%
- Report：15% (less than 10 pages)
  - Summary of your structure
  - Discussion about worst case pattern
  - Layout photo
  - Discussion
  - Your thoughts of this final project and course.
- Bonus：25%
  - Hand in VERILOG model of your design, and the critical path should not be longer than 20ns. You should write a short report to illustrate the characterization process and discuss the results. (20%)
  - Performance (5%)

V. Note

a. **This project is group project, the maximum member in each group is two**

b. Copy files from TA “tar xvf ~vlsita01/Final_Proj_2019.tar”

c. Enjoy the fun from this assigned work.

d. You need to hand in the following files

1. studentID_MAC4.gds
2. studentID_MAC4.sp (pre-sim design)
3. studentID_period.txt (list your pre-sim clock period and post-sim clock period)
4. report_studentID.pdf
5. studentID_MAC4.v (optional)