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EXPERIMENT NO.3

In this report, we will explore the creation of XOR and XNOR gates using Cadence, a software tool for designing integrated circuits. These gates are important building blocks in digital circuit design, used in arithmetic and data processing operations. We will use Cadence's schematic editor to design the gates and its layout editor to create a layout. The gates' functionality will be verified using Cadence's simulation tools. This project aims to deepen our understanding of the gates' operations, while also gaining hands-on experience in using Cadence Virtuoso for digital circuit design.

1. Compound gate $Y = \overline{(A \cdot B) + (C \cdot D)}$

This function is sometimes called AND-OR-INVERT-22. To create this circuit, we need to create pull up and pull-down circuits. The pull up circuit uses pmos, when the output is high, this circuit works. The pull-down circuit uses nmos, works when the output is low.

Assume that $Y = \overline{(A \cdot B) + (C \cdot D)} = 1$. Then $\bar{Y} = \overline{\overline{(A \cdot B) + (C \cdot D)}} = 0$. Thus: $\bar{Y} = (A \cdot B) + (C \cdot D) = 0$. So, we have the following circuit:

(a)   (b)

Since the components of the circuit include the multiplication of A by B, the A and B inputs must be in series. Same for inputs C and D. AB and CD are the results of addition. Therefore, must be connected in parallel (based on the design principle in section 1.4.3). So, we connect the circuit as shown above. This is a pull-down circuit because it works when the output is low.
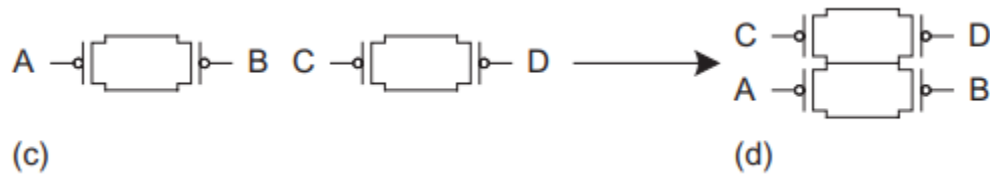
Similarly for output when high, we will design pull up circuit. According to de morgan's principle, the output will be rewritten as:

$Y = \overline{(A \cdot B) + (C \cdot D)} = 1$

$$\rightarrow Y = \overline{(A \cdot B)} \cdot \overline{(C \cdot D)}$$

$$\rightarrow Y = \overline{(A + B)} \cdot \overline{(C + D)}$$

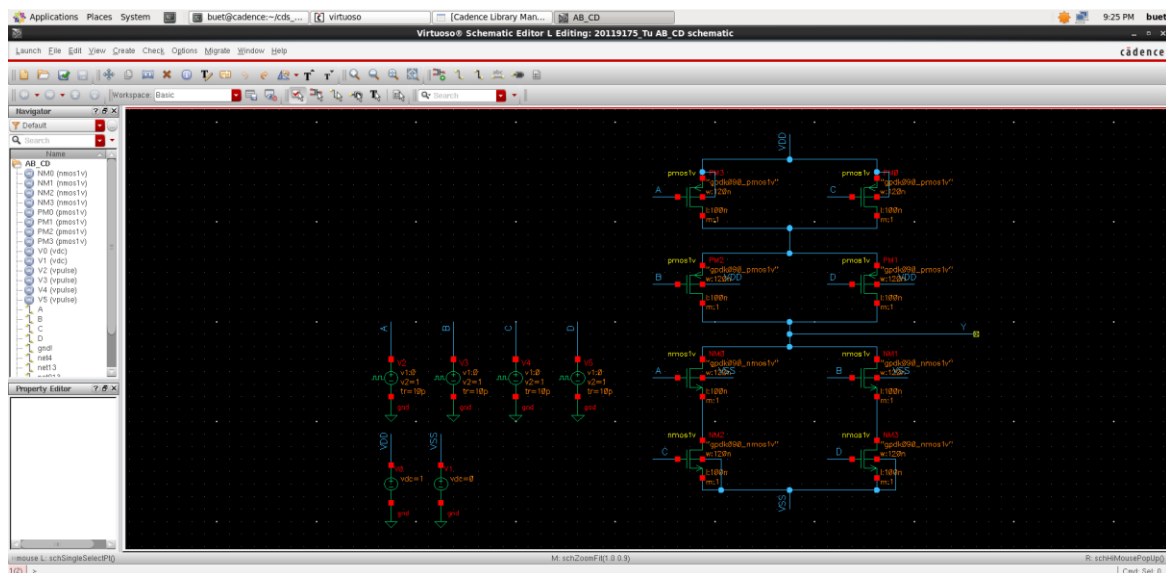So, we have the following circuit:

(c)   (d)

This will be a pull up circuit, active when the output is high. Connecting the above two circuits together, we have the following circuit:
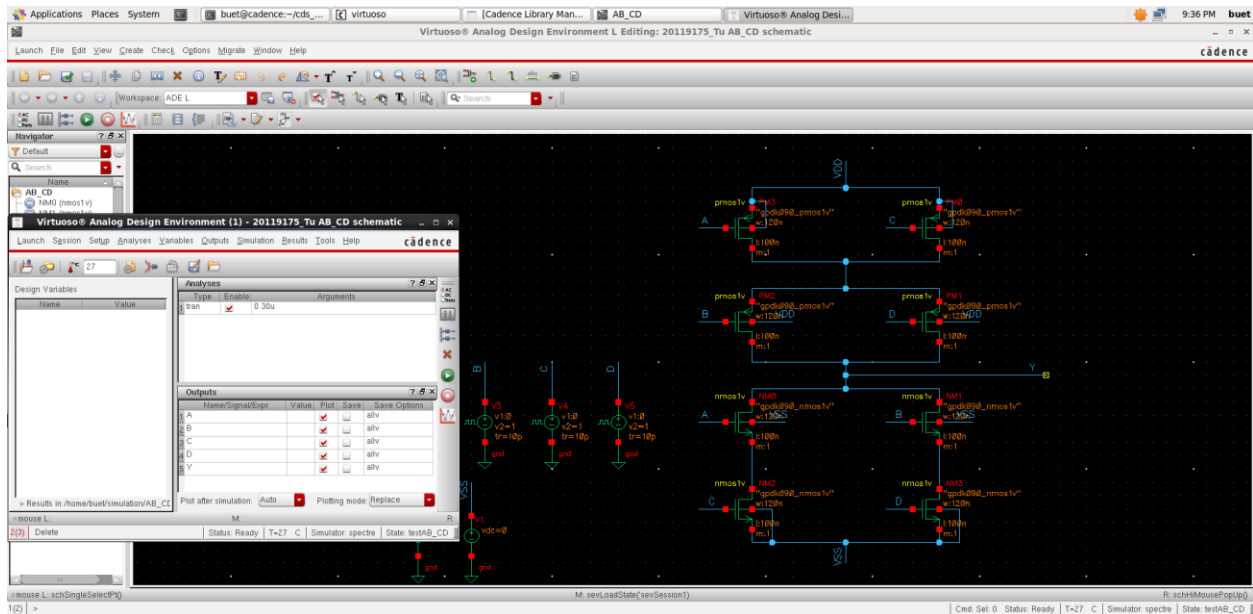

(e)   (f)

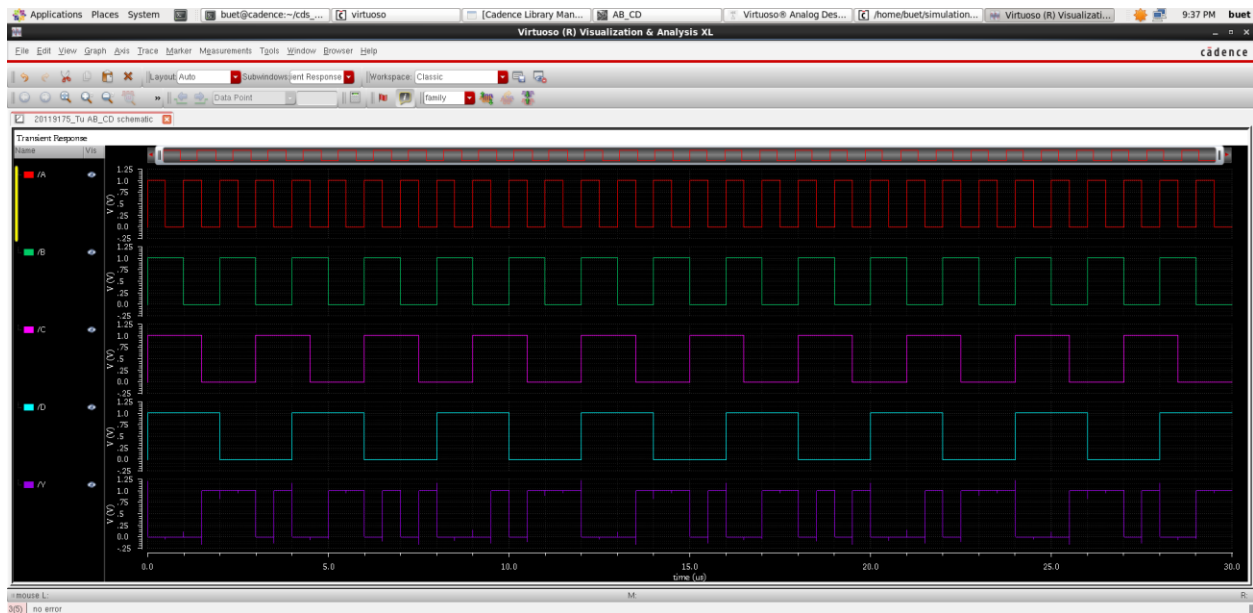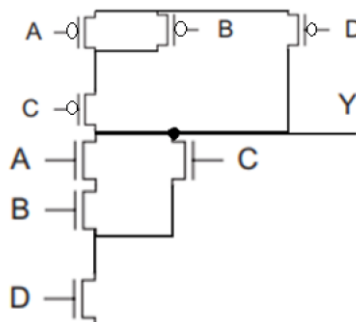**FIGURE 1.18** CMOS compound gate for function $Y = \overline{(A \cdot B) + (C \cdot D)}$

This is compound gate of $Y = \overline{(A \cdot B) + (C \cdot D)}$. After that, we conduct simulation on cadence virtuoso software. The circuit will look like this:

You proceed to create pulses as instructed in experiment 1, then conduct simulation. To complete 16 input states, we need to simulate with longer time.

And here is the simulation result:

2. **Compound gate Y** $= \overline{(A \cdot B + C) \cdot D))}$

Assume that $Y = \overline{(A \cdot B + C) \cdot D))} = 1$.

Then $\bar{Y} = \overline{\overline{(A \cdot B + C) \cdot D))}} = 0$. Thus: $\bar{Y} = (A \cdot B + C) \cdot D)) = 0$. So, we have the following circuit:

Similarly for output when high, we will design pull up circuit. According to de morgan's principle, the output will be rewritten as:

$Y = \overline{(A \cdot B + C) \cdot D))}$

$\rightarrow Y = \overline{(A \cdot B + C)} + \bar{D}))$

$\rightarrow Y = \overline{(\bar{A} + \bar{B} \cdot \bar{C})} + \bar{D}))$
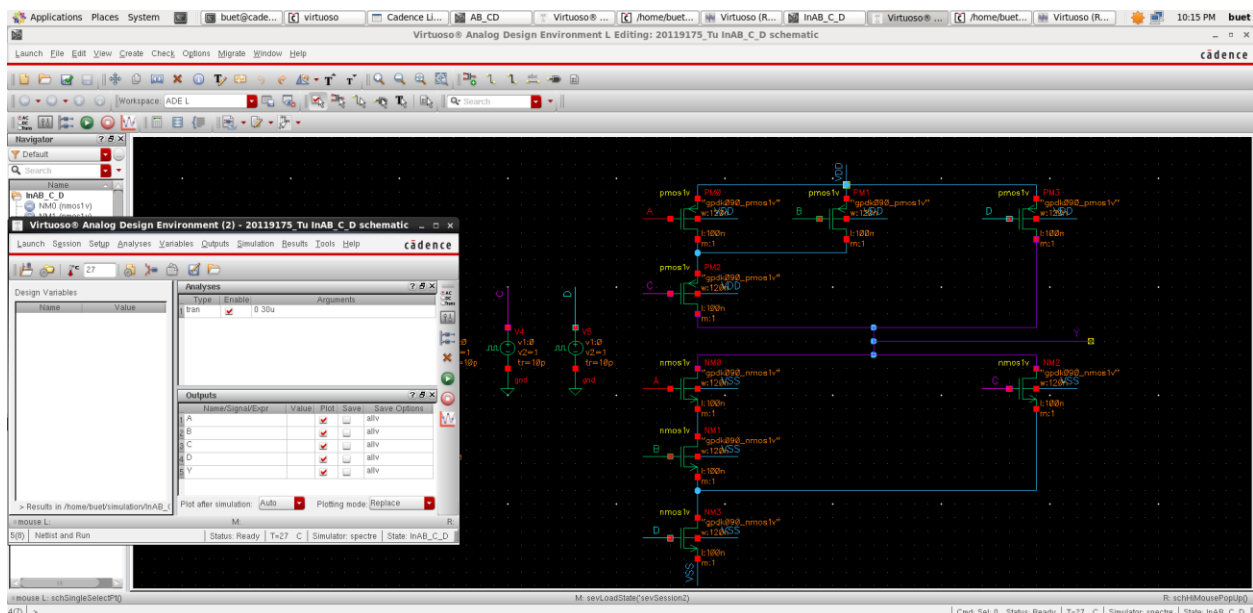
So, we have the following circuit:

This will be a pull up circuit, active when the output is high. Connecting the above two circuits together, we have the following circuit:
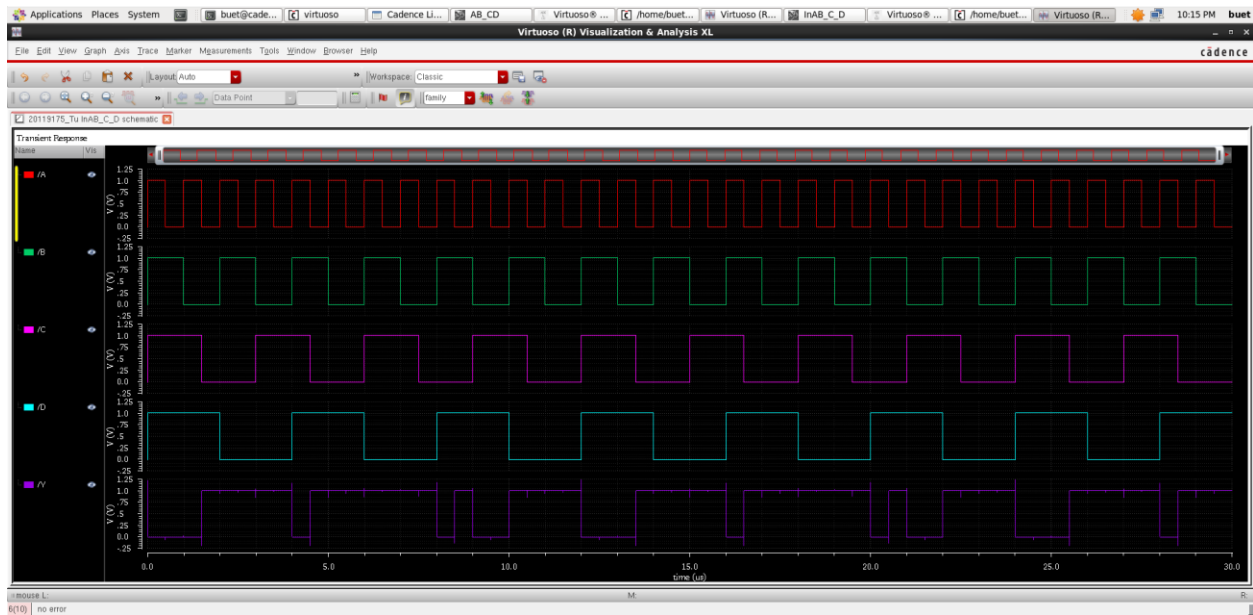
This is compound gate of $Y = \overline{(A \cdot B + C) \cdot D))}$. After that, we conduct simulation on cadence virtuoso software. The circuit will look like this:
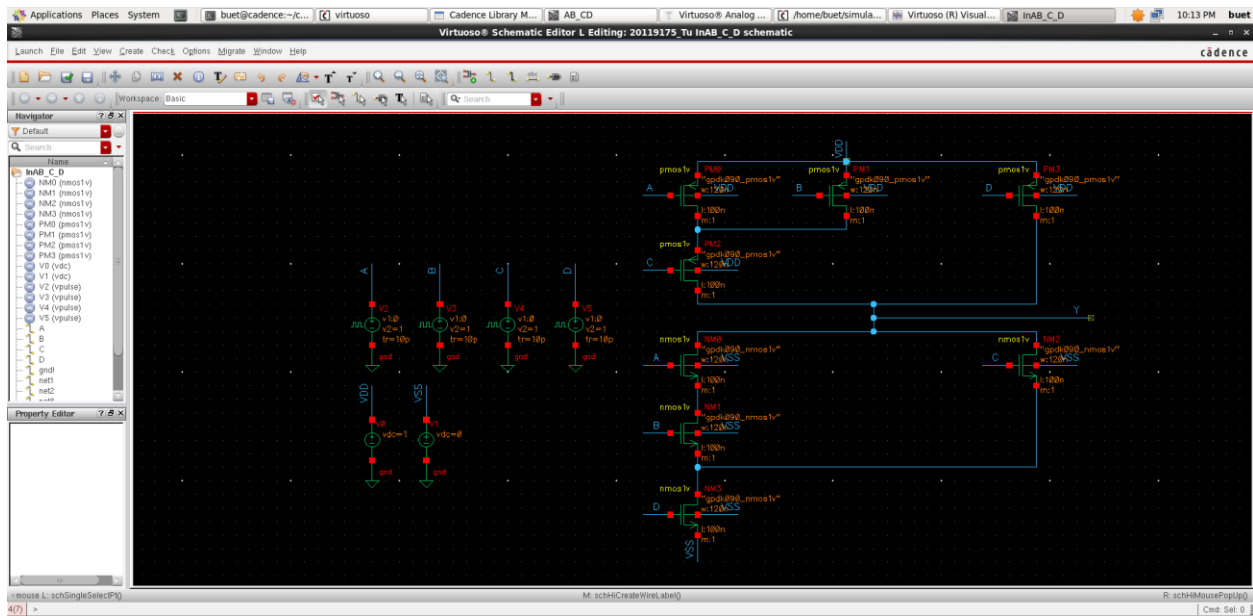
You proceed to create pulses, then conduct simulation. To complete 16 input states, we need to simulate with longer time.

And here is the simulation result:

3. XOR and XNOR Gates:

a. XOR Gate

To design an XOR gate, you need to know about the XOR boolean expression:

In there:

$$A \oplus B = A\bar{B} + \bar{A}B$$

So, we have to design a compound gate whose boolean expression is:
$\mathbf{Y} = (\mathbf{A} \cdot \overline{\mathbf{B}}) + (\overline{\mathbf{A}} \cdot \mathbf{B})$. The following will be the truth table of the XOR gate:

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

Assume that $Y = (A \cdot \overline{B}) + (\overline{A} \cdot B) = 1.$

Then $\overline{Y} = \overline{(A \cdot \overline{B}) + (\overline{A} \cdot B)} = 0$. According to de morgan's principle, the output will be rewritten as:

$$\overline{Y} = \overline{(A \cdot \overline{B})} \cdot \overline{(\overline{A} \cdot B)} = 0$$

$$\overline{Y} = (\overline{A} + B) \cdot (A + \overline{B}) = 0$$

Therefore, we can create the pull-down circuit like this:

Easy for pull up circuit:
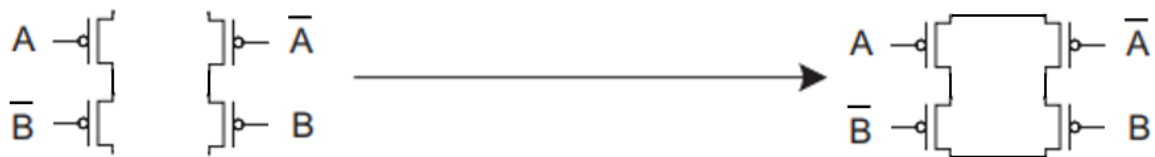
Connecting the above two circuits together, we have the following circuit:
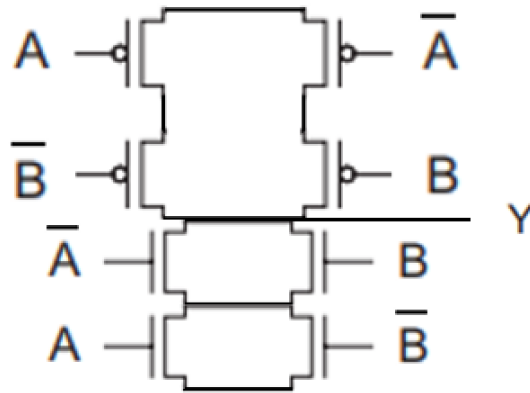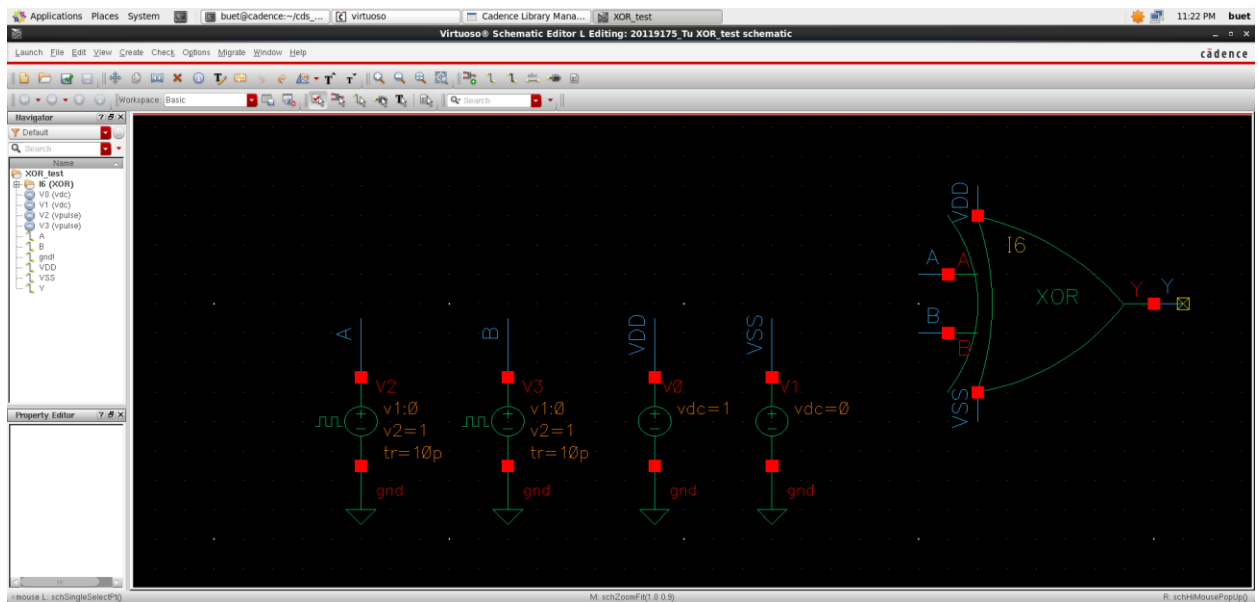
After that, we conduct simulation on cadence virtuoso software. I use the inverter to make the offset state of A and do the same for B. The circuit will look like this:
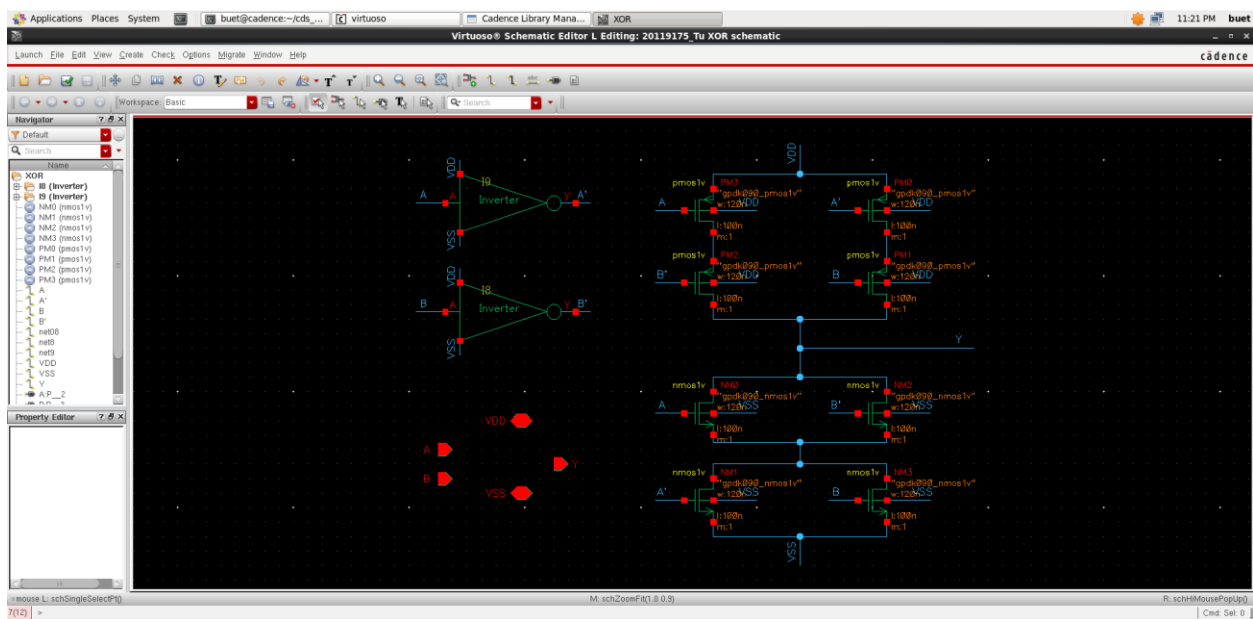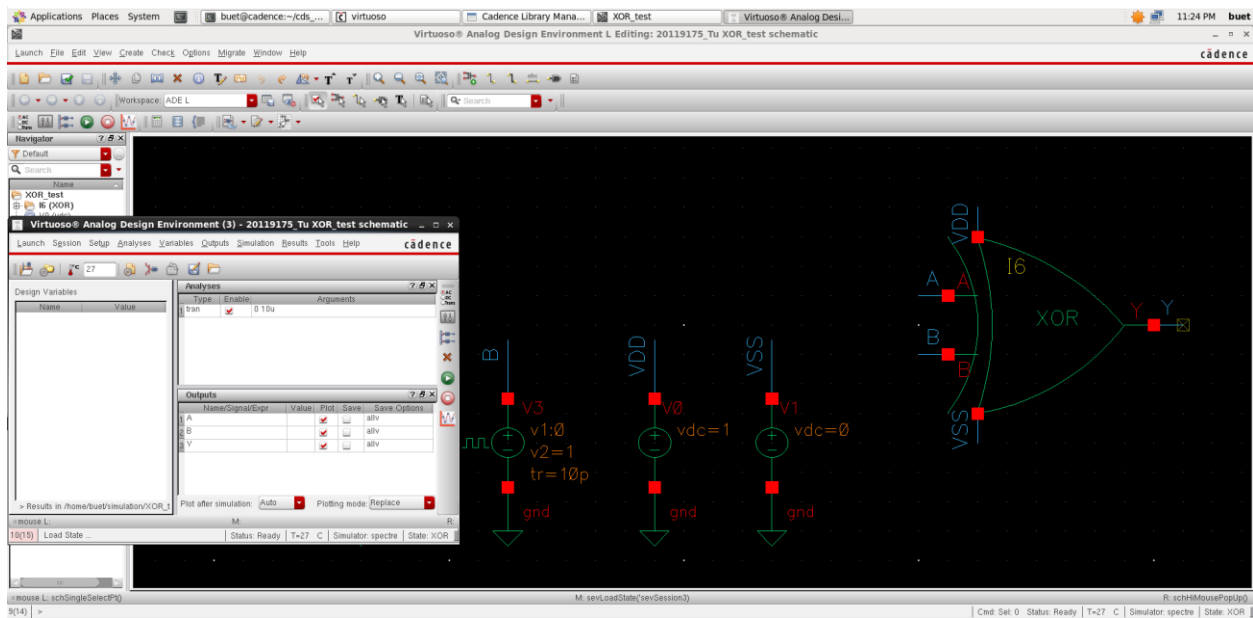

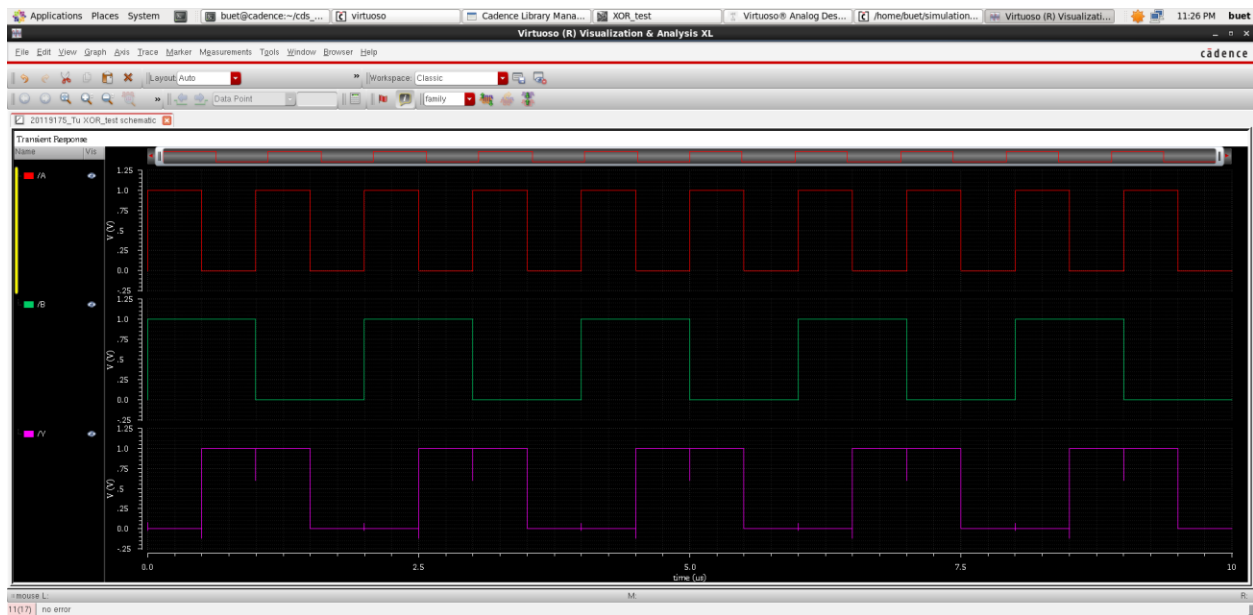Then, create the symbol like this:
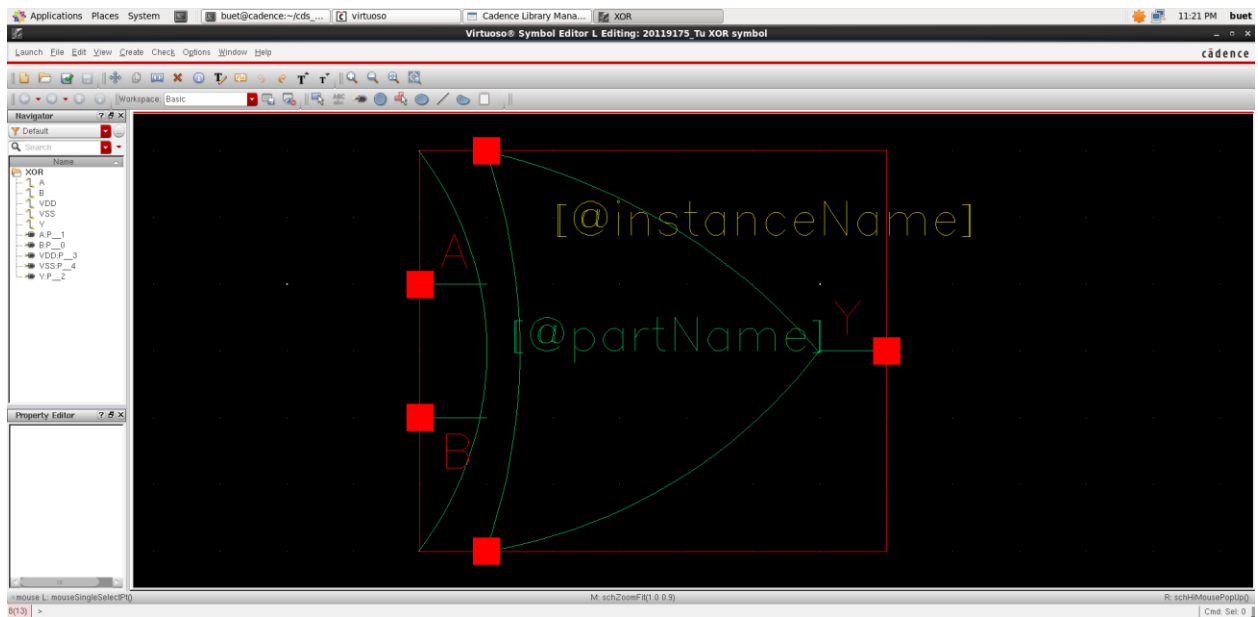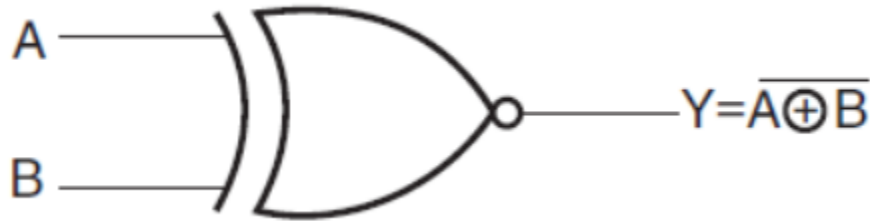
Then, conduct circuit simulation:

And here is the simulation result:

b. *XNOR Gate*

Similar to XOR gate, you need to know about the XNOR boolean expression if you want to design an XNOR gate in Cadence Virtuoso:

In there:

$$Y = (\overline{A \oplus B}) = (A.B + \overline{A}.\overline{B})$$

So, we have to design a compound gate whose boolean expression is: $Y = (A \cdot B) + \overline{(A \cdot B)}$. The following will be the truth table of the XNOR gate:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Assume that $Y = (A \cdot B) + \overline{(A \cdot B)} = 1$.

Then $\overline{Y} = \overline{(A \cdot B) + \overline{(A \cdot B)}} = 0$. According to de morgan's principle, the output will be rewritten as:
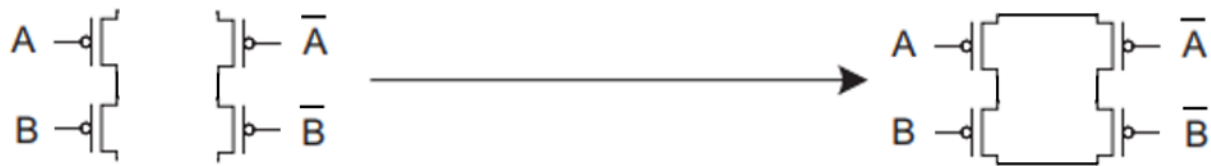
$$\overline{Y} = \overline{(A \cdot B)} \cdot (A \cdot B) = 0$$

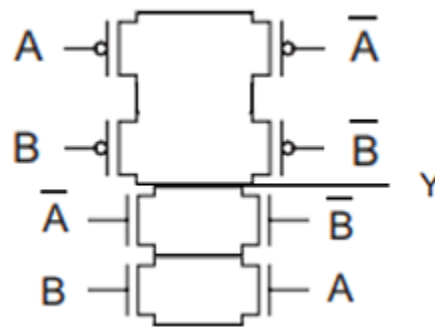$$\overline{Y} = \overline{(A + B)} \cdot (A \cdot B) = 0$$

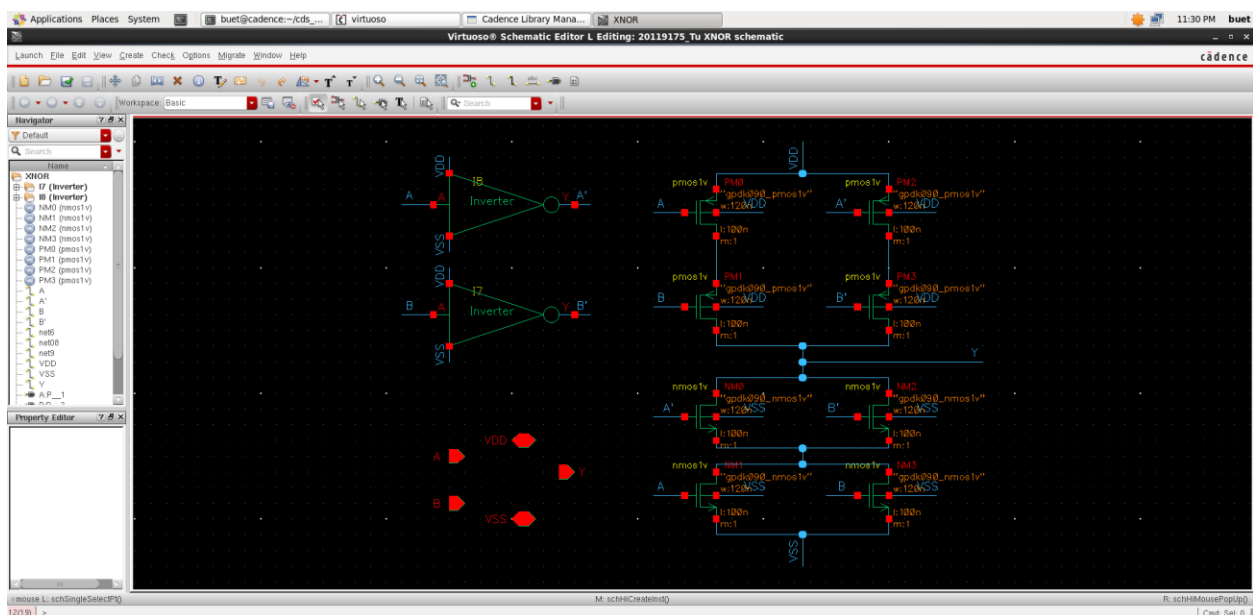Therefore, we can create the pull-down circuit like this:
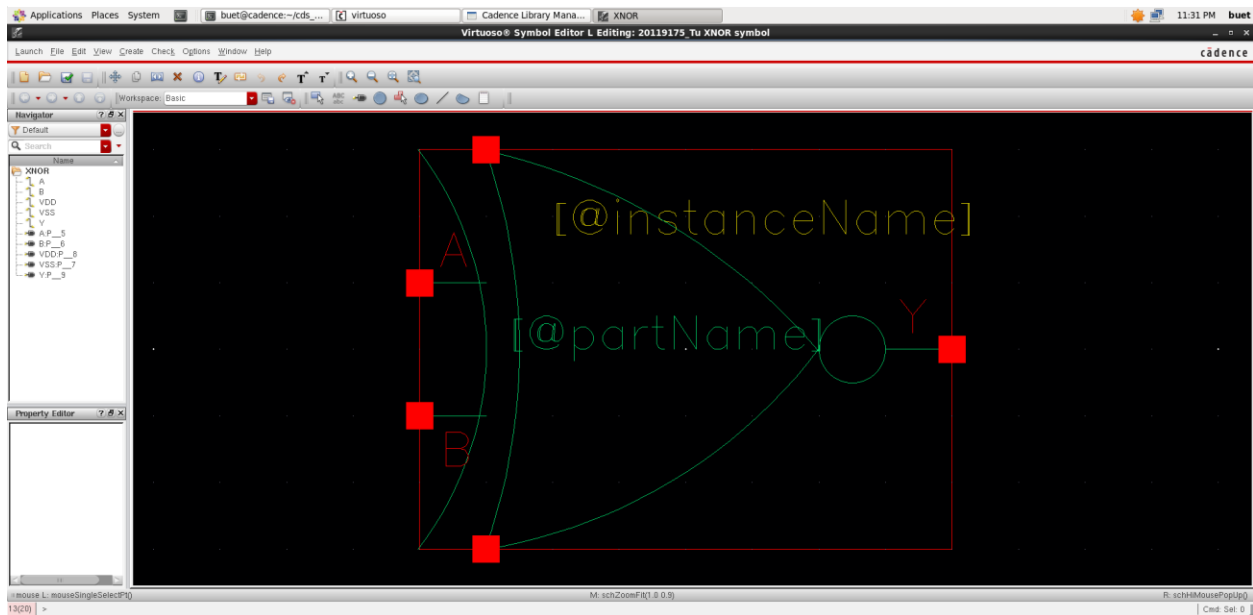
And for pull up circuit:

Connecting the above two circuits together, we have the following circuit:
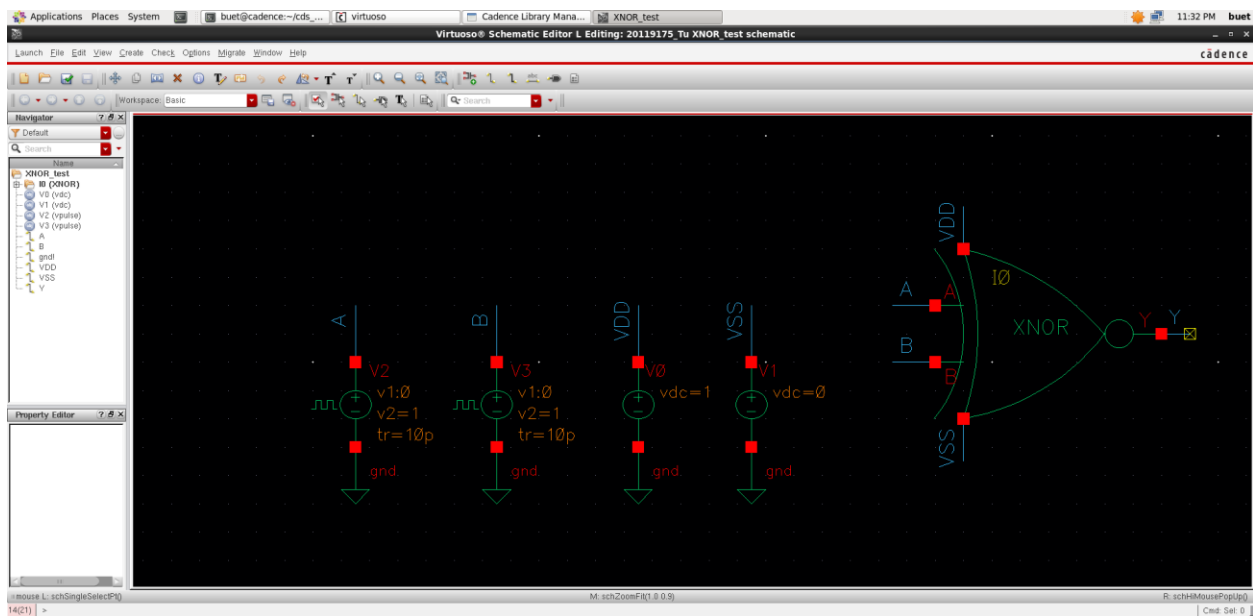

After that, we conduct simulation on cadence virtuoso software. The circuit will look like this:
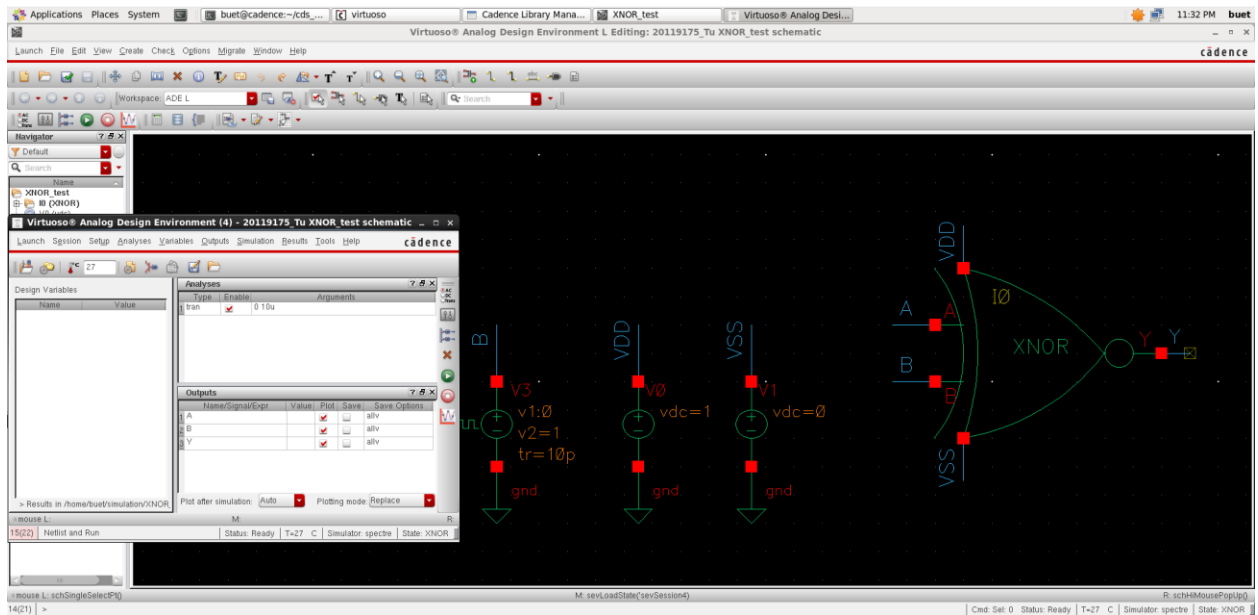
Then, create the XNOR symbol:

Then, conduct circuit simulation:

And here is the simulation result: