

Name: Ngô Tiến Tú

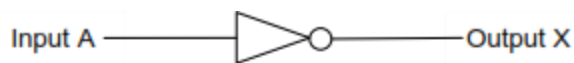
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EXPERIMENT NO.2

Today, I will write about how to create logic gates: Inverter, NOR gate, NAND gate and their symbols. The first is the inverter. Creating an inverter port is very simple, you just need to do the same as the steps I instructed last week, take the components and assemble the circuit as follows.

1. Inverter

The design of the Inverter gate must follow the principle diagram, and the result must follow the following truth table

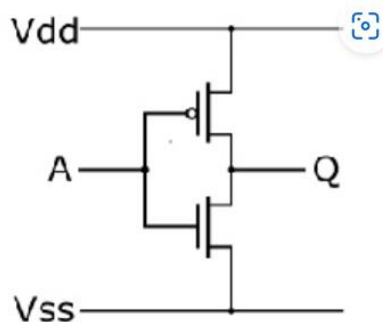


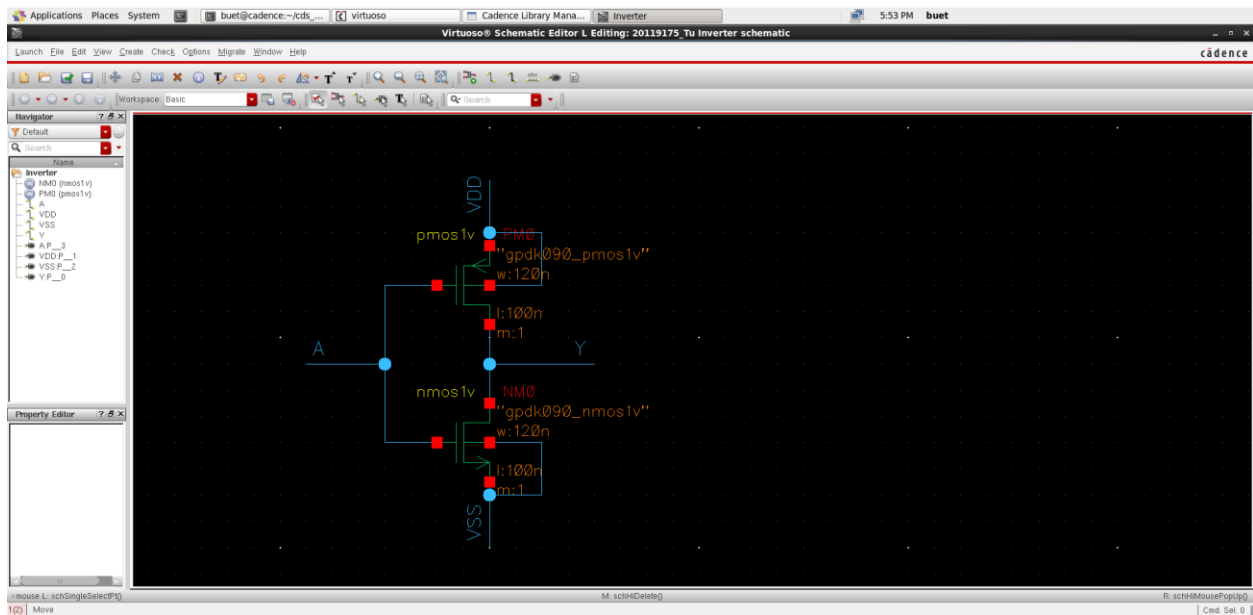
(a) Symbol

| Input A | Output X |
|---------|----------|
| 0 | 1 |
| 1 | 0 |

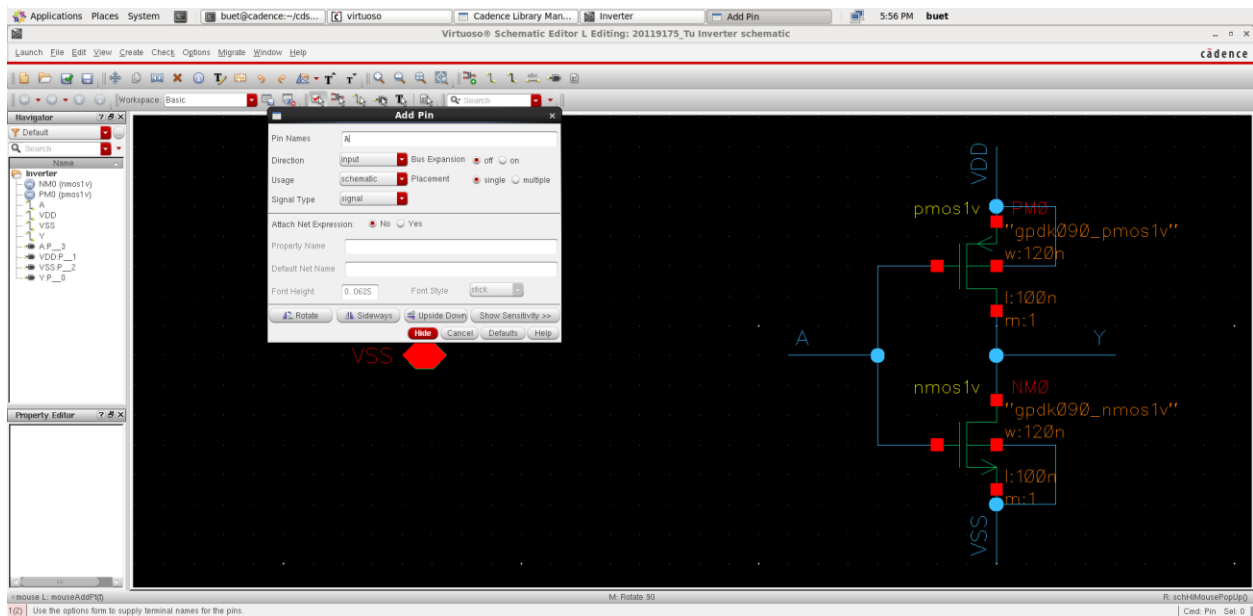
(b) Truth table

The following is the cmos circuit of the inverter gate:

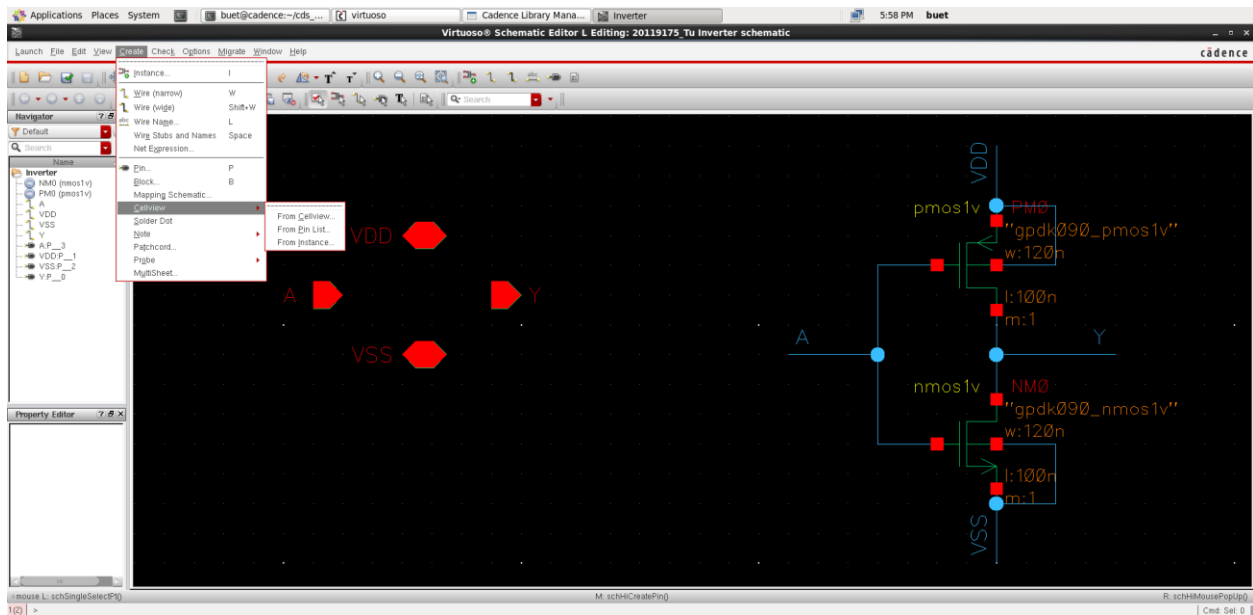




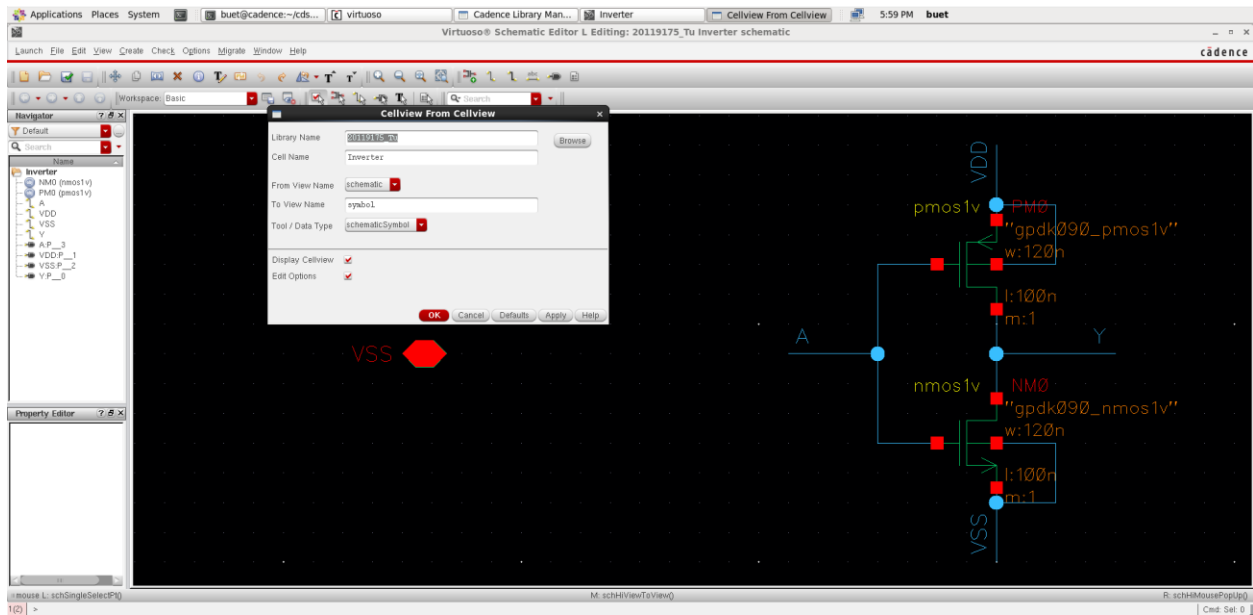
Then to create a connector, press the keyboard shortcut p on the keyboard. The menu appears as shown, you fill in the foot according to the instructions: A- input , Y-output, VDD and VSS are InputOutput.



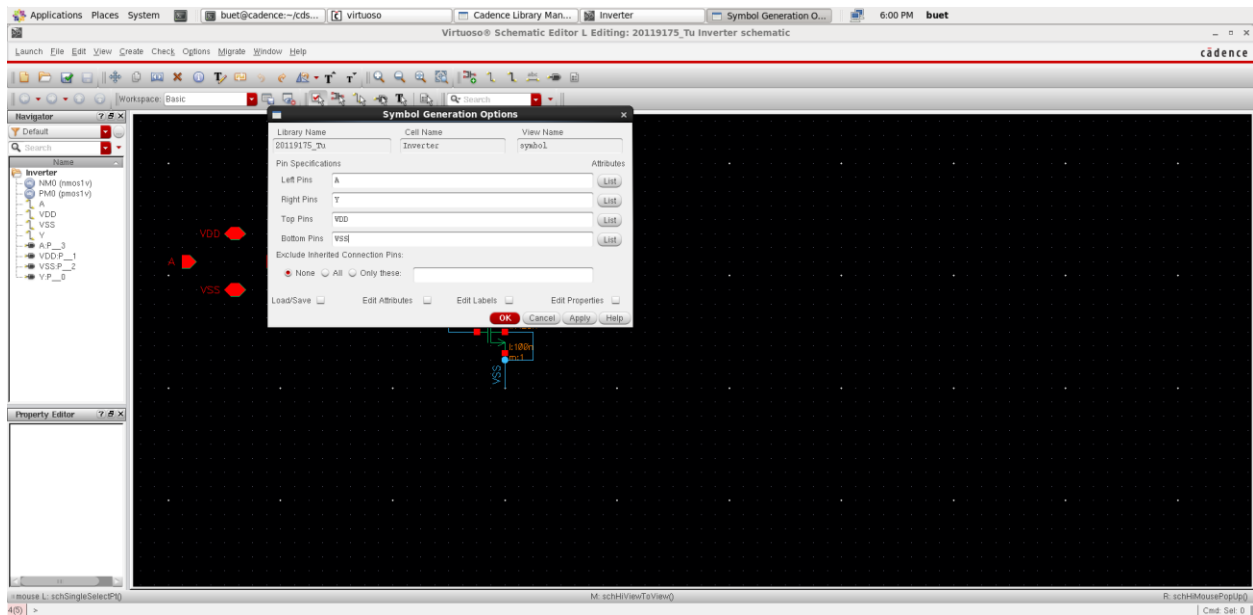
After check and save, choose create -> cellview -> from cellview



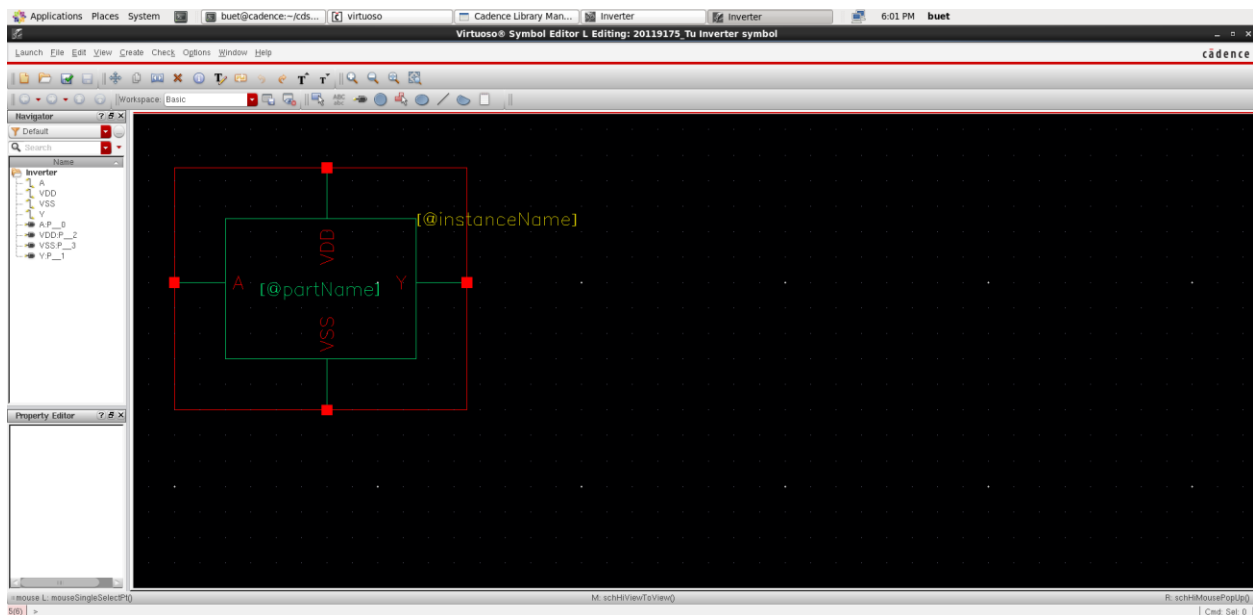
Click OK



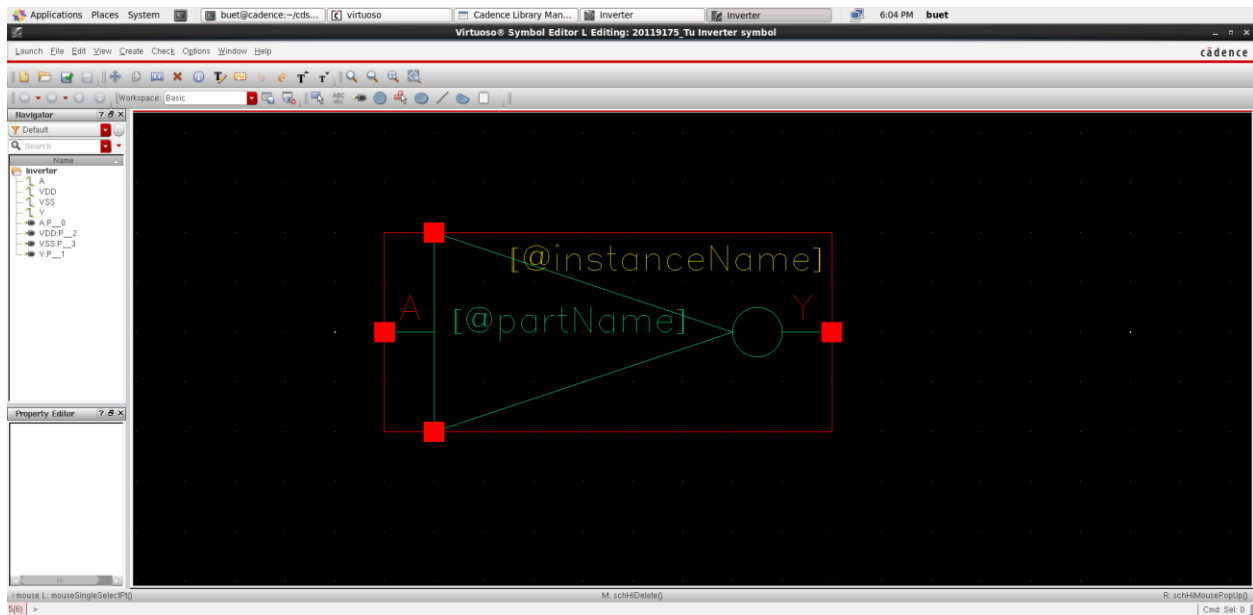
Choose the foot position you want to do



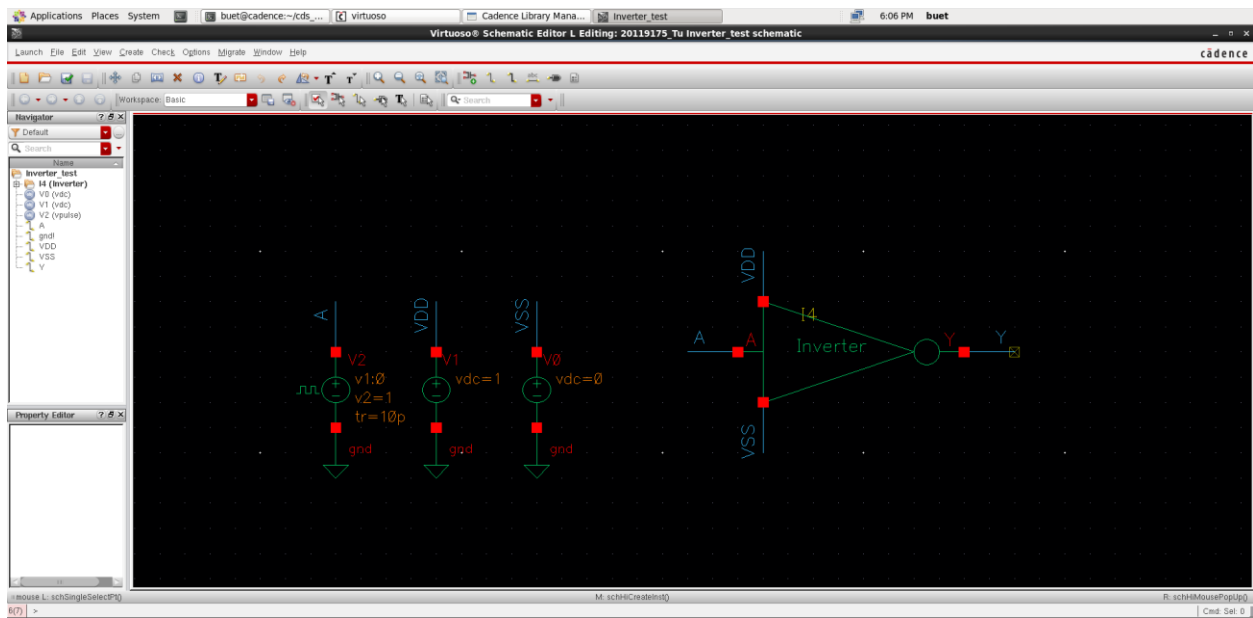
Then the menu appears as shown, your job is to redraw it to look like an inverter port



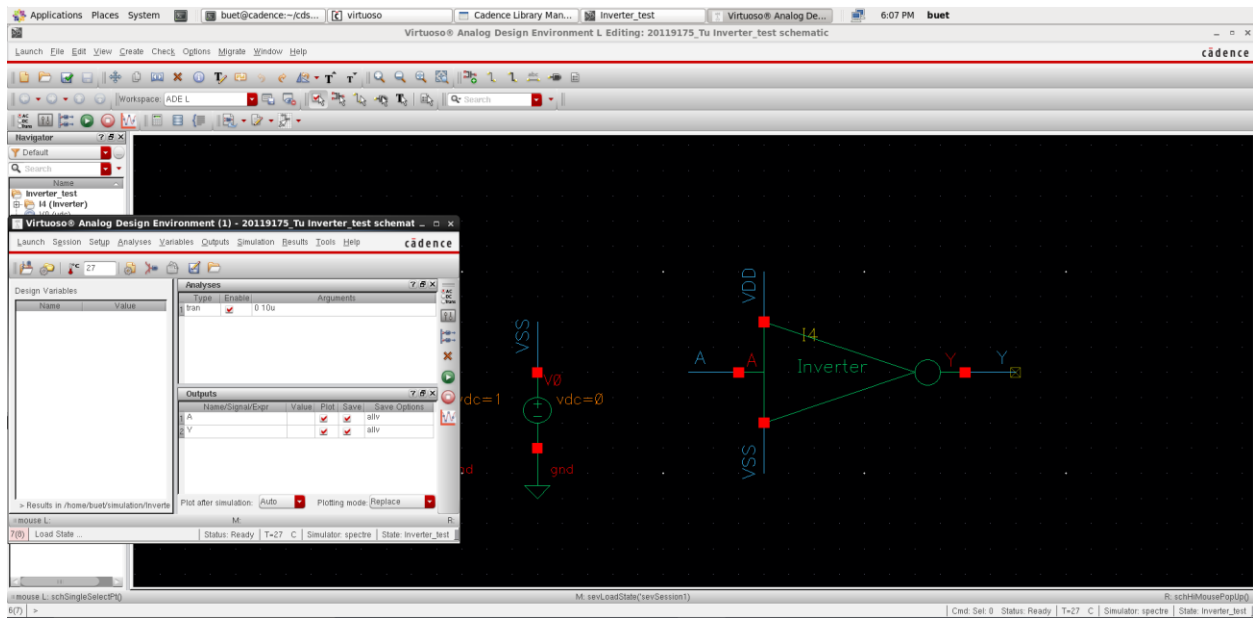
I redraw it like this, then save it to test the circuit.



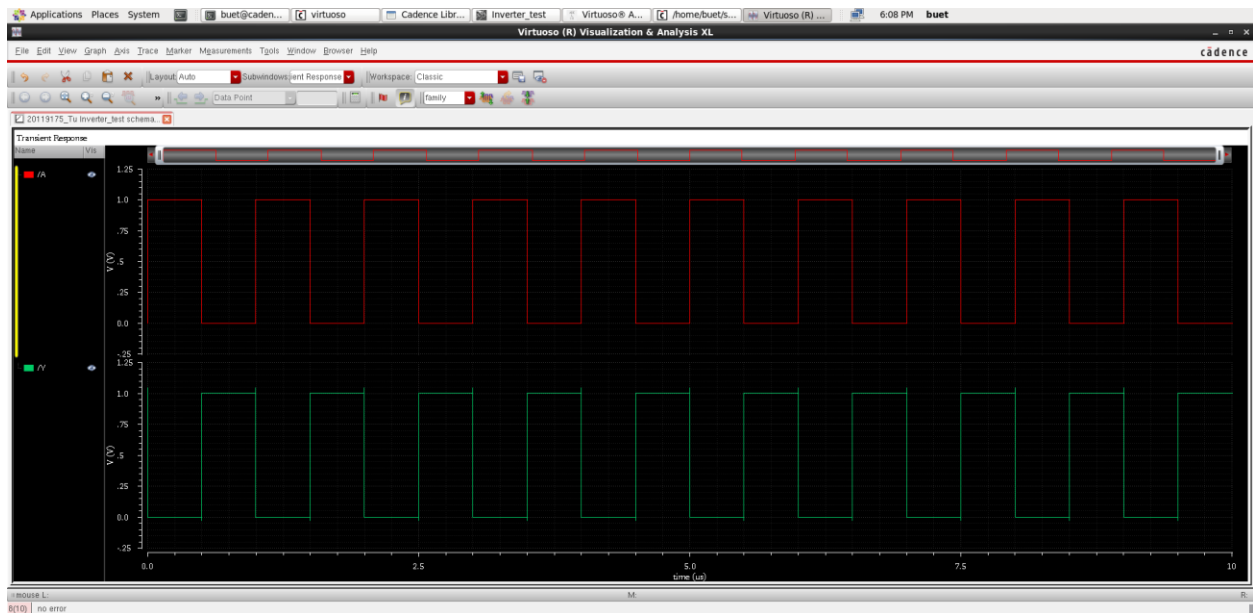
generate 1 pulse to input A to test



I simulate the circuit within 10 microsecond



And this is the result



2. NAND Gate

Similarly, to create an AND gate you do the following: create a cmos circuit including pmos and nmos, create pins, then draw symbols and simulate. Following is the symbol and truth table of the NAND gate

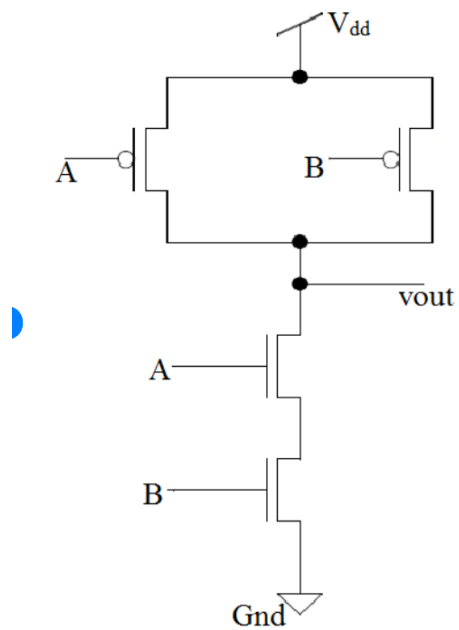


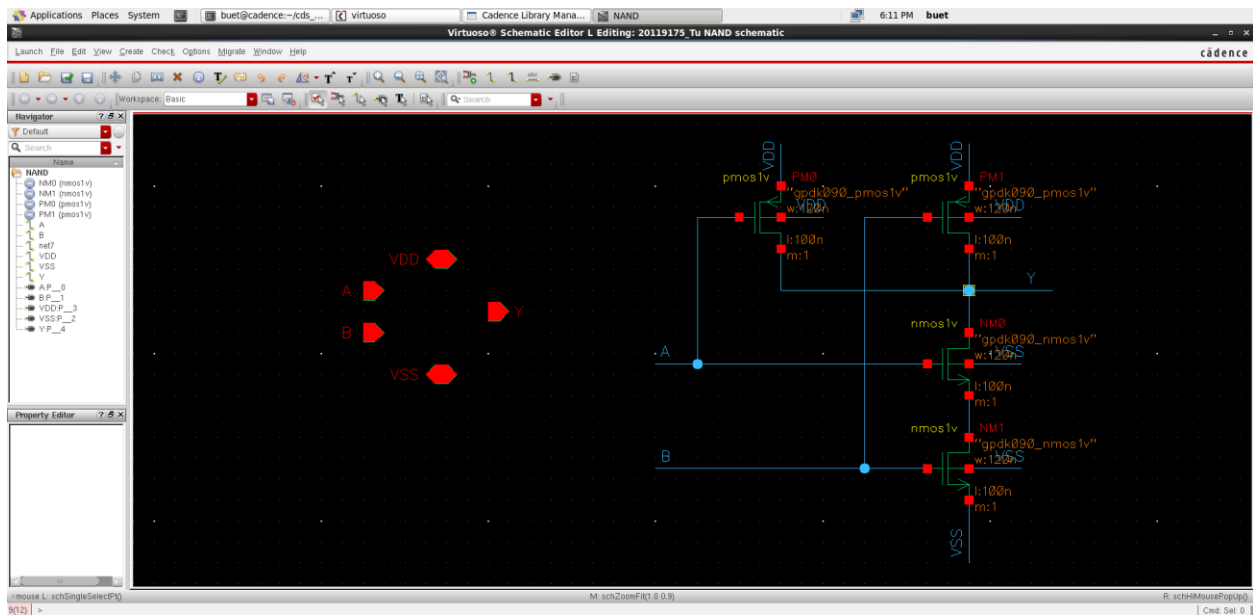
$$Q = A \text{ NAND } B$$

Truth Table

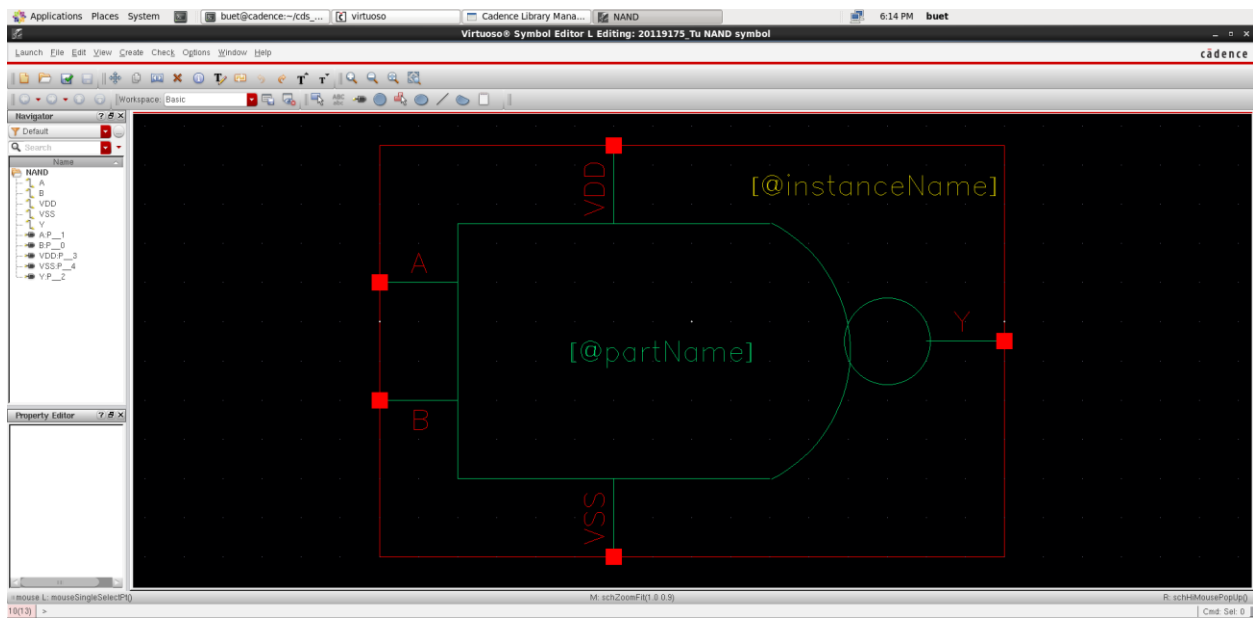
| Input A | Input B | Output Q |
|---------|---------|----------|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

And here is the CMOS circuit of the NAND gate

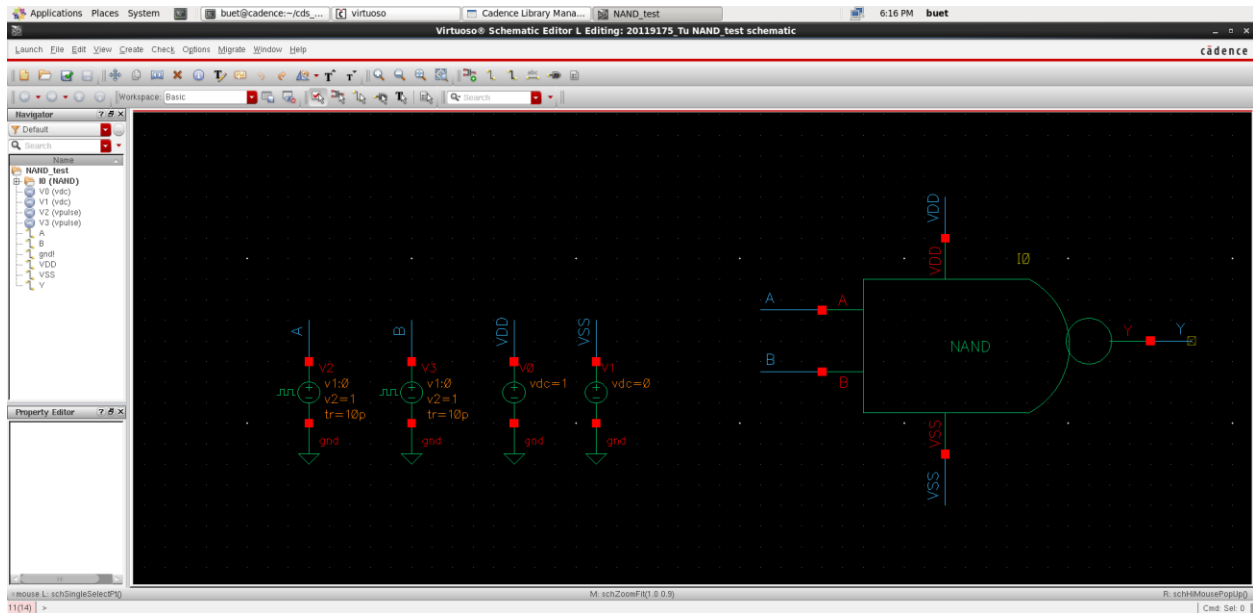




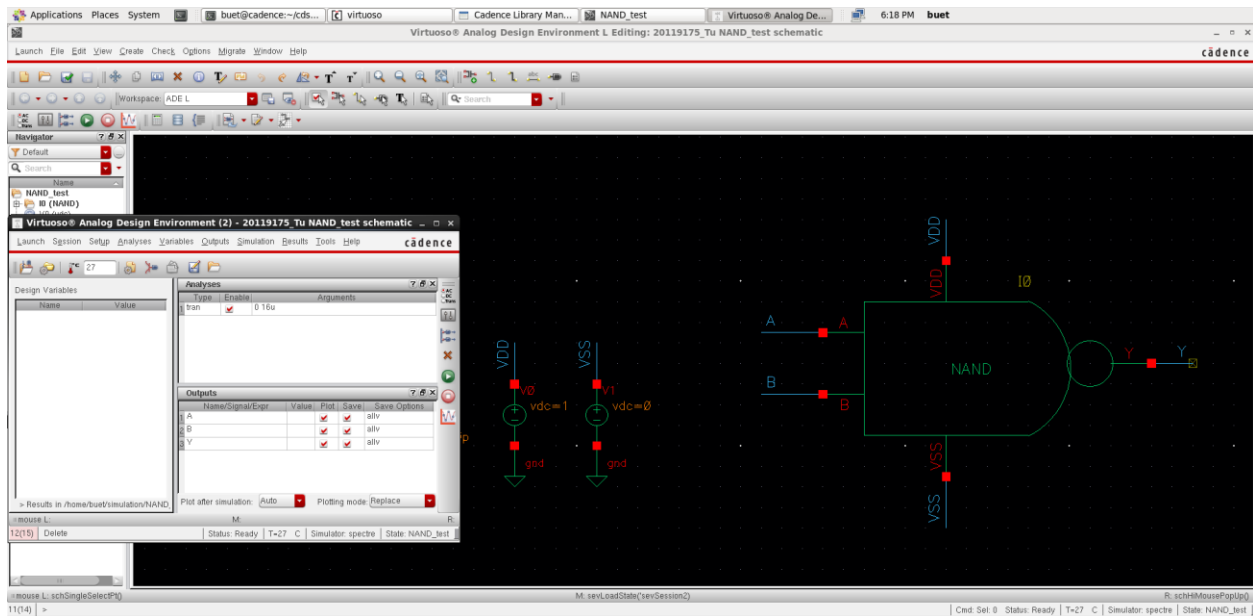
Then draw the symbol as follows



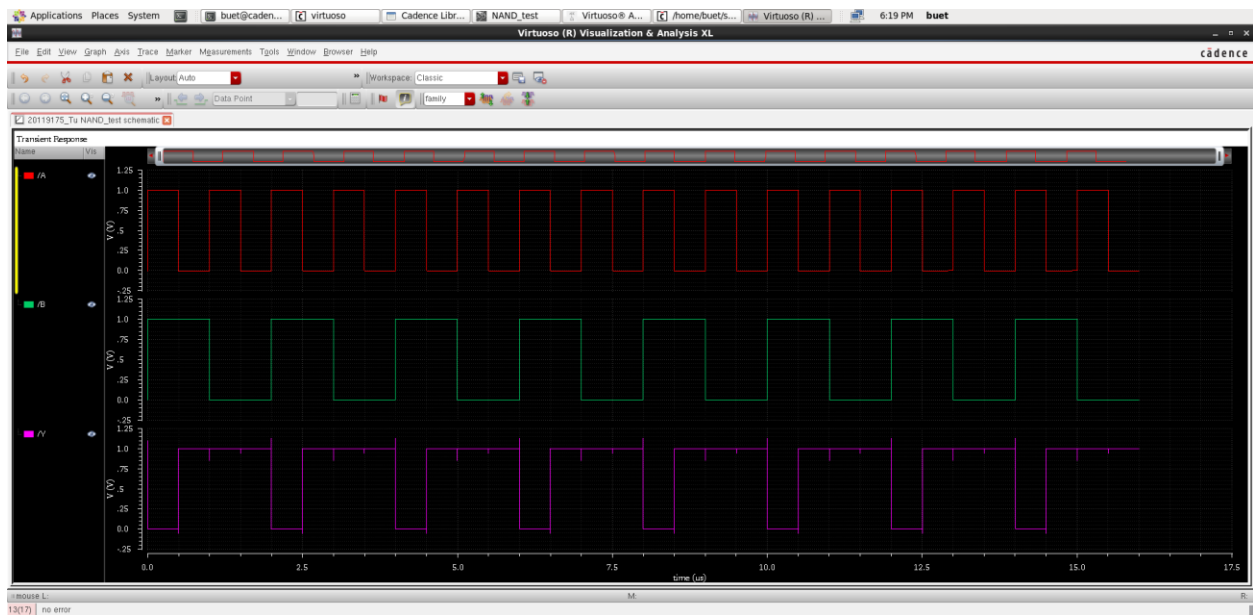
Then conduct simulation by generating 2 different pulses and inputting 2 inputs:



Generating 2 different pulses I showed in last week's report, you can use copy command by pressing c key on keyboard, then drag inputs from old file and drop in new one

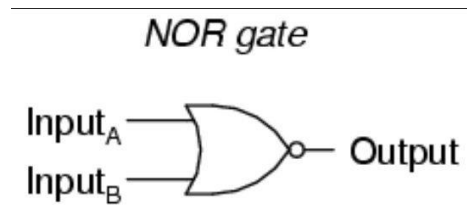


And this is the result



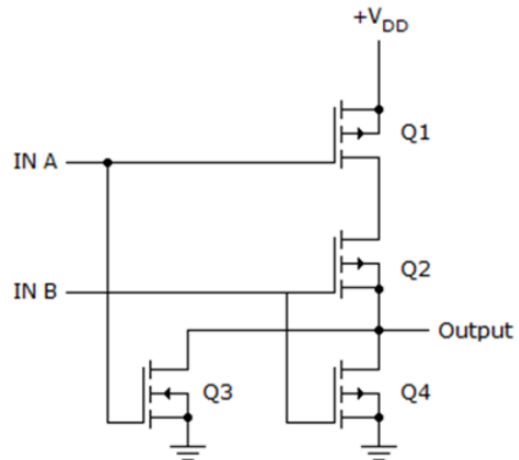
3. NOR Gate

Here is the symbol and truth table of the NOR gate

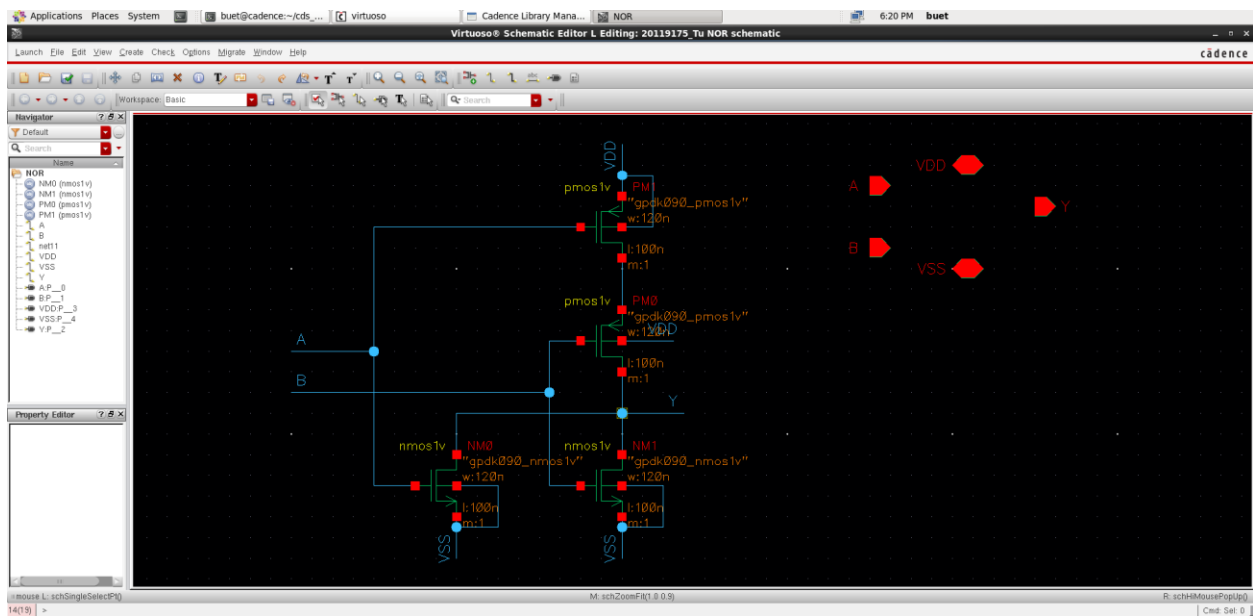


| A | B | Output |
|---|---|--------|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

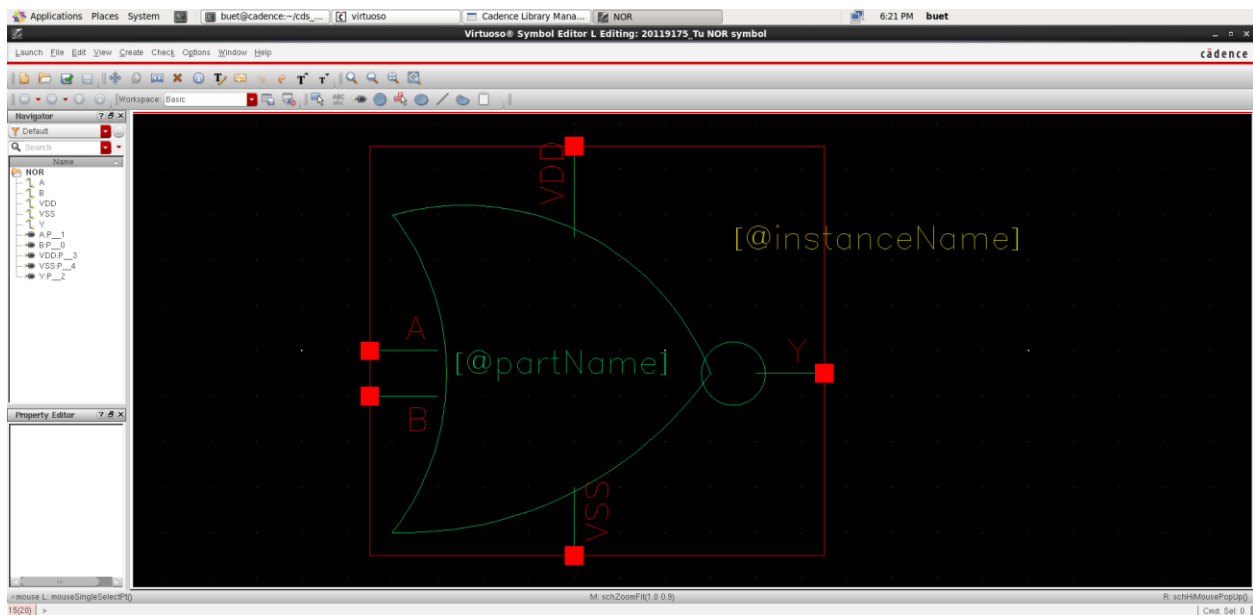
And here is the CMOS circuit of the NAND gate



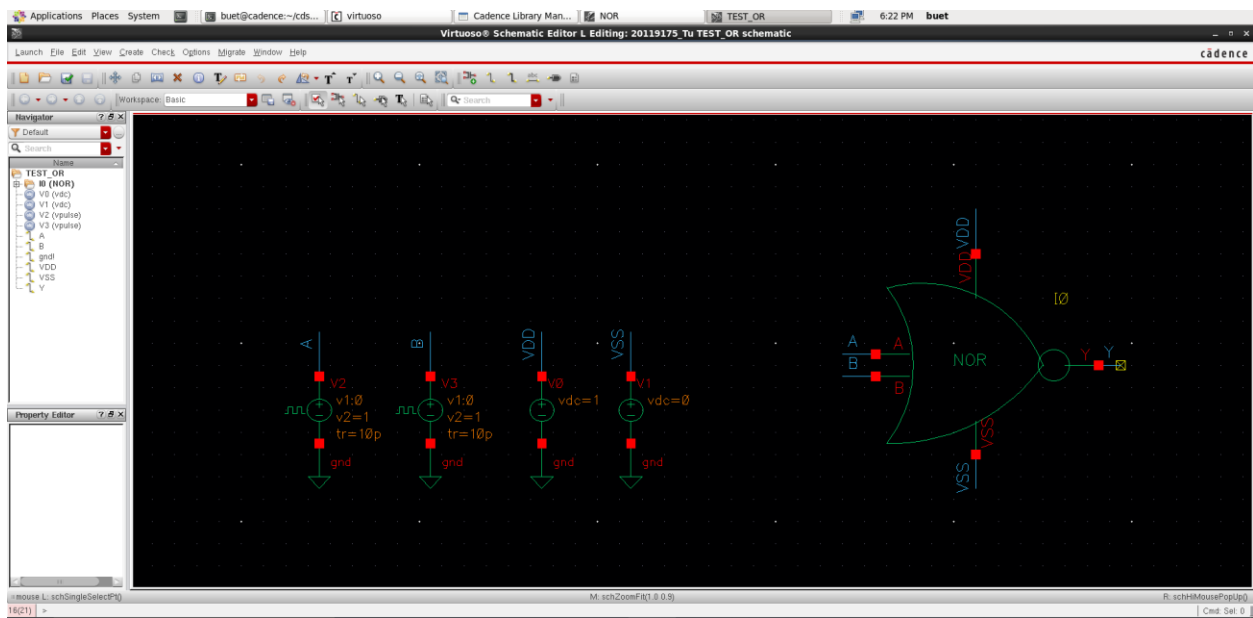
The design of the NOR gate is the same as the design of the previous logic gates, you do the same steps with an overall design as shown below.

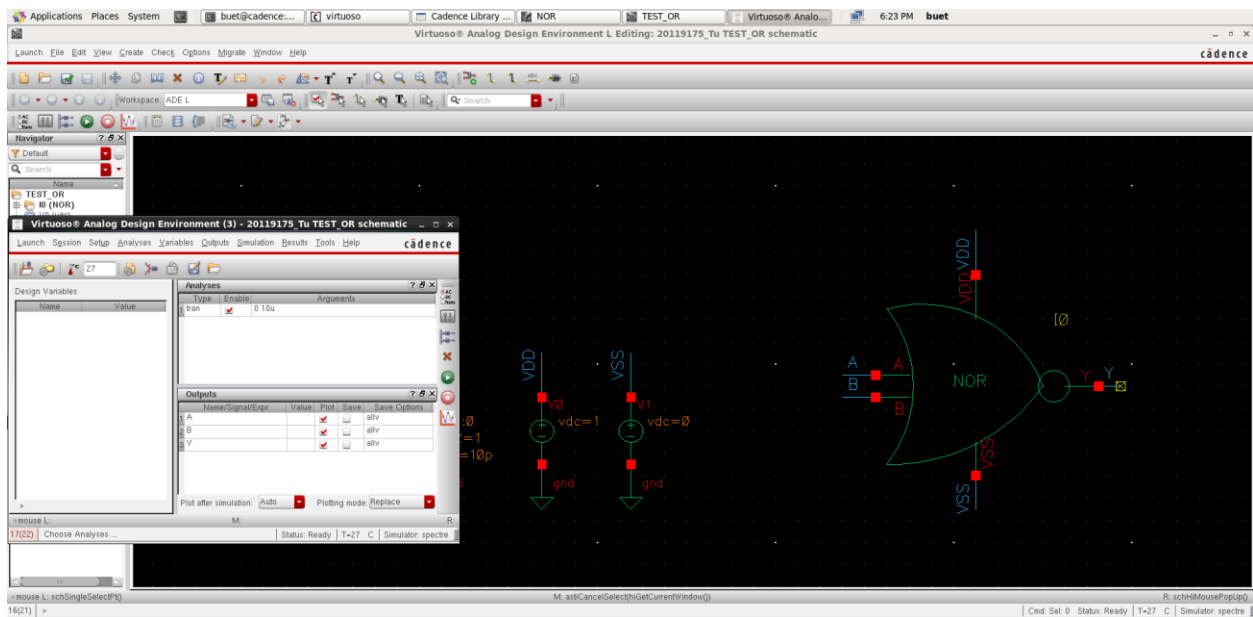


generate the symbol of the NOR gate



After that, conduct simulation





And this is the result

