TRƯỜNG ĐẠI HỌC FPT

KẾ HOẠCH TRIỂN KHAI HỌC PHẦN
PLAN OF COURSE IMPLEMENTATION

DANANG CAMPUS

Tên học phần/*Course name:* **Computer Organization and Architecture / Tổ chức và Kiến trúc máy tính**
Course name

1. **Thời gian triển khai: Học kỳ: SP 2023 từ 02/01/2023 đến 26/03/2023**
Duration: Semester ……from……to……

2. **Số lớp triển khai/***Number of classes : 4*

3. **Đề cương triển khai:** CEA201.
Implement in accordance with Syllabus: CEA201

4. **Danh sách Giảng viên triển khai học phần/** *List of Classes and Lecturers:*

STT *No.*	Tên giảng viên *Lecturer*	STT *No.*	Tên giảng viên *Lecturer*
1	Nguyễn Văn Điền	4	
2		5	
3		6	

5. **Danh sách giảng viên hỗ trợ, trợ giảng, khách mời (nếu có),**
Supporting Lecturers, assistants, guest speakers (if any)

STT No.	Họ và tên Full name	Vai trò Role	Nội dung Content	Thời lượng Duration	Thời gian Time	Số lớp No of Class	Kinh phí Budget

6. **Các hoạt động phát sinh:***Addtional Activities:*

STT No.	Họ và tên Full name	Mục tiêu Target		Thời lượng Duration	Thời gian Time	Số lớp No of Class	Kinh phí Budget

7. **Tài liệu tham khảo bổ sung/***AdditionalReferences:*

8. **Môi trường, công cụ triển khai bổ sung/** *Update Environments and Tools (if any):*

a) Thực hiện giảng dạy hoặc sử dụng trên những website nào:
Websites for Teaching or Using:
http://williamstallings.com/ComputerOrganization/COA9e-Instructor/
http://williamstallings.com/ComputerOrganization/COA9e-student/

b) Yêu cầu về công cụ, kỹ thuật đặc thù gì *(cái gì, ở đâu, như thế nào…)*
Specific Tools and technical required(What? Where? How?, etc.)
http://www.masm32.com/
http://www.windows8downloads.com/win8-masm-64.html

c) Kênh trao đổi thông tin giữa thầy và trò *(kể cả việc nộp bài, cho điểm, nhận xét…)*
Communication channels among lecturers and students (including submitting assignments, marking, and giving comment)

10.Lịch triển khai môn học

Slot	*Week*	*Chapter -Topic -Content*	*Assessment*	*Assignment Homework*	*Note*
1		Introduction to the course Chapter 1: Introduction 1.1 Organization and Architecture 1.2 Structure and Function			
2	*02/01/2023*	Assessing exercises of chapter 1 Chapter 2: Computer Evolution and Performance 2.1 A Brief History of Computers 2.2 Designing for Performance			
3		Chapter 2 contd. 2.3 Multicore, MICs, and GPGPUs 2.6 Performance Assessment			
4		Assessing exercises of chapter 2 Chapter 3 A Top-Level View of Computer Function and Interconnection 3.1 Computer Components 3.2 Computer Function			
5	*09/01/2023*	Chapter 3 contd. 3.3 Interconnection Structures 3.4 Bus Interconnection			
6		Assessing exercises of chapter 3 Chapter 4 Cache Memory 4.1 Computer Memory System Overview 4.2 Cache Memory Principles			
7		Chapter 4 contd. 4.3 Elements of Cache Design			
8	*31/01/2023*	Assessing exercises of chapter 4 Chapter 5 Internal Memory 5.1 Semiconductor Main Memory 5.2 Error Correction			
9		Chapter 5 contd. 5.3 Advanced Dram Organization			
10	*06/02/2023*	Assessing exercises of chapter 5 Chapter 6 External Memory 6.1 Magnetic Disk 6.2 Raid			
11		Chapter 6 External Memory contd.			

		6.2 Raid contd 6.3 Solid State Drives			
12		Assessing exercises of chapter 6 Chapter 7 Input/Output 7.1 External Devices 7.2 I/O Modules 7.3 Programmed I/O			
13		Chapter 7 Input/Output contd. 7.4 Interrupt-Driven I/O 7.5 Direct Memory Access 7.6 I/O Channels and Processors			
14	*13/02/2023*	Assessing exercises of chapter 7 Chapter 8 Operating System Support 8.1 Operating System Overview			
15		Chapter 8 Operating System Support contd. 8.2 Scheduling 8.3 Memory Management			
16		Assessing exercises of chapter 8 Chapter 11 Digital Logic 11.1- Boolean Algebra 11.2-Gates 11.3- Combinational Circuit			
17	*20/02/2023*	Assessing exercises of chapter 9 Chapter 12 Instruction Sets: Characteristics and Functions 12.1 Machine Instruction Characteristics 12.2 Types of Operands			
18		Chapter 12 Instruction Sets: Characteristics and Functions cont. 12.4 Types of Operations			
19	*27/02/2023*	Assessing exercises of chapter 12 Chapter 13 Instruction Sets: Addressing Modes and Formats 13.1 Addressing Modes 13.3 Instruction Formats 13.5 Assembly Language			
20		Practical Assembly Laguage			
21		Practical Assembly Laguage			
22	*06/03/2023*	Practical Assembly Laguage			

23		Practical Assembly Laguage Assignment introduction (2 programs)			
24		Assessing exercises of chapter 13 Chapter 14 Processor Structure and Function 14.1 Processor Organization 14.2 Register Organization			
25	*13/03/2023*	Chapter 14 Processor Structure and Function contd. 14.3 Instruction Cycle 14.4 Instruction Pipelining			
26		Assessing exercises of chapter 14 Chapter 15 Reduced Instruction Set Computers 15.1 Instruction Execution Characteristics 15.2 The Use of a Large Register File 15.3 Compiler-Based Register Optimization 15.4 Reduced Instruction Set Architecture			
27		Assessing exercises of chapter 15 Chapter 16 Instruction-Level Parallelism and Superscalar Processors 16.1 Overview 16.2 Design Issues			
28	*20/03/2023*	Assessing exercises of chapter 16 Chapter 17 Parallel Processing 17.1 Multiple Processor Organizations 17.2 Symmetric Multiprocessors 17.3 Cache Coherence and the MESI Protocol 17.4 Multithreading and Chip Multiprocessors			
29		Assessing exercises of chapter 16 Chapter 18 Multicore Computers 18.1 Hardware Performance Issues 18.2 Software Performance Issues 18.3 Multicore Organization			

30		Assessing assigments Review			

Người phê duyệt/*Approver* *GĐCS/Campus's Director*	Người kiểm tra/*Reviewer* *TBĐT/Head of Academic Affairs Board)*	Người lập/*Creator* *CNBM/Head of department*
Họ tên/*Name:* Ngày/*Date:*	Họ tên/*Name:* Ngày/*Date:*	Họ tên/*Name: Nguyễn Văn Điền* Ngày/*Date: 28/12/2022*