# Syllabus Details

| | |
|---|---|
| Syllabus ID: | 6735 |
| Syllabus Name: | **Computer Organization and Architecture_Tổ chức và Kiến trúc máy tính** |
| Course Name English: | |
| Subject Code: | **CEA201** |
| NoCredit: | 3 |
| Degree Level: | Bachelor |
| Time Allocation: | Study hour (150h) = 45h contact hours + 1h final exam + 104h self-study |
| Pre-Requisite: | |
| Description: | This course in an introduction to computer architecture and organization. It will cover topics in both the physical design of the computer (organization) and the logical design of the computer (architecture). The main contents include the organization of a simple stored-program computer: CPU, busses and memory; Instruction sets, machine code, and assembly language; Conventions for assembly language generated by compilers; Floating-point number representation; Hardware organization of simple processors; Address translation and virtual memory; Very introductory examples of input/output devices, interrupt handling and multi-tasking systems.<br>Chapter covered: Computer Evolution and Performance; A Top-Level View of Computer Function and Interconnection; Cache Memory; Internal Memory; External Memory; Input/Output; Operating System Support; Instruction Sets: Characteristics and Functions; Processor Structure and Function; Reduced Instruction Set Computers; Instruction-Level Parallelism and Superscalar Processors; Parallel Processing; Multicore Computers.<br><br>Assessment scheme:<br><br>1) On-going asessment:<br>- 4 Exercises: 30%<br>- 02 Assignment: (2 Assembly programs) 30%<br>2) Final exam: 40%<br>3) Final result: 100%<br>Completion Criteria:<br>1) Every on-going assessment component >0<br>2) Final Exam Score >=4 & Final Result >=5 |
| StudentTasks: | Upon successful completion of this course, students should:<br>1. Knowledge:<br>- Understand the structure and function of computers generally and a distinction between computer organization and computer architecture.<br>- Understand computer organization: roles of processors, main memory, and interface between the computer and peripherals<br>- Understand computer architecture: instruction set, the number of bits used to represent various data types, I/O mechanism and techniques for addressing memory<br>2. Skills:<br>- Be able to solve binary math operations using the computer.<br>- Be able to write simple assembly language programs<br>- Be able to prepare engineering reports and do presentations scientifically<br>- Be able to apply knowledges to do research projects. |
| Tools: | |
| Scoring Scale: | 10 |
| DecisionNo MM/dd/yyyy: | 1009/QĐ-ĐHFPT |
| IsApproved: | **True** |
| Note: | |
| MinAvgMarkToPass: | 5 |
| IsActive: | True |
| ApprovedDate: | 8/17/2022 |

8 material(s)

| MaterialDescription | Author | Publisher | PublishedDate | Edition | ISBN | IsMainMaterial | IsHardCopy | IsOnline | Note |
|---|---|---|---|---|---|---|---|---|---|
| Computer Organization and Architecture: Design for Performance | William Stallings | Prentice Hall | 2012 | 9th (or 10th) | 978-0132936330 (9th), 978-0134101613 (10th) | ☑ | ☑ | ☐ | |
| Computer architecture : A quantitative approach | John L. Hennessy, David A Patterson | Morgan Kaufmann | | | | ☐ | ☑ | ☐ | |
| http://williamstallings.com/ComputerOrganization/COA9e-Instructor/ | | | | | | ☐ | ☐ | ☑ | |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| http://williamstallings.com/ComputerOrganization/COA9e-student/ | | | | | | ☐ | ☐ | ☑ | |
| PowerPoint Lecture Slides | | | | | | ☐ | ☐ | ☐ | |
| Instructor Solutions Manual | | | | | | ☐ | ☐ | ☐ | |
| Instructor Project Manual | | | | | | ☐ | ☐ | ☐ | |
| Test banks | | | | | | ☐ | ☐ | ☐ | |

9 LO(s)

| CLO Name | CLO Details |
|---|---|
| CLO1 | Explain the general functions and structure of a digital computer |
| CLO2 | Present an overview of the evolution of computer technology from early digital computers to the latest microprocessors. |
| CLO3 | Understand the key performance issues that relate to computer design |
| CLO4 | Describe in detail the essential elements of computer organisation including internal bus, memory, Input/Output ( I/O) organisations and interfacing standards and discuss how these elements function; |
| CLO5 | Summarize, at a top level, the key functions of an operating system (OS). |
| CLO6 | Be able to apply Boolean algebra and digital logic to design and interpret complex digital circuits; |
| CLO7 | Present various types of addressing modes common in instruction sets, an essential characteristics of machine instructions, types of operands supported by typical machine instruction sets |
| CLO8 | Explain processor structure and function in details, the operations of Reduced Instruction Set Computers |
| CLO9 | Investigate, evaluate and communicate general trends in computing technologies such as Instruction-Level Parallelism and Superscalar Processors |

**Mapping of CLOs to PLOs of Curriculum BIT_SE**

| CLO | PLOs | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PLO1 | PLO2 | PLO3 | PLO4 | PLO5 | PLO6 | PLO7 | PLO8 | PLO9 | PLO10 | PLO11 | PLO12 | PLO13 | PLO14 | PLO15 | PLO16 | PLO17 | PLO18 |
| CLO1 | | | | | | | | | ✓ | | | | | | | | | |
| CLO2 | | | | | | | | | ✓ | | | | | | | | | |
| CLO3 | | | | | | | | | ✓ | | | | | | | | | |
| CLO4 | | | | | | | | | ✓ | | | | | | | | | |
| CLO5 | | | | | | | | | ✓ | | | | | | | | | |
| CLO6 | | | | | | | | | ✓ | | | | | | | | | |
| CLO7 | | | | | | | | | ✓ | | | | | | | | | |
| CLO9 | | | | | | | | | ✓ | | | | | | | | | |

**Mapping of CLOs to PLOs of Curriculum BIT_IS**

| CLO | PLOs | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PLO1 | PLO2 | PLO3 | PLO4 | PLO5 | PLO6 | PLO7 | PLO8 | PLO9 | PLO10 | PLO11 | PLO12 | PLO13 | PLO14 | PLO15 | PLO16 | PLO17 | PLO18 |
| CLO1 | | | | | | | | | ✓ | | | | | | | | | |
| CLO2 | | | | | | | | | ✓ | | | | | | | | | |
| CLO3 | | | | | | | | | ✓ | | | | | | | | | |
| CLO4 | | | | | | | | | ✓ | | | | | | | | | |
| CLO5 | | | | | | | | | ✓ | | | | | | | | | |
| CLO6 | | | | | | | | | ✓ | | | | | | | | | |
| CLO7 | | | | | | | | | ✓ | | | | | | | | | |
| CLO8 | | | | | | | | | ✓ | | | | | | | | | |
| CLO9 | | | | | | | | | ✓ | | | | | | | | | |

**Mapping of CLOs to PLOs of Curriculum BIT_IoT**

| CLO | PLOs |
|---|---|

| | Mapping of CLOs to PLOs of Curriculum BIT_IoT | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PLO1 | PLO2 | PLO3 | PLO4 | PLO5 | PLO6 | PLO7 | PLO8 | PLO9 | PLO10 | PLO11 | PLO12 | PLO13 | PLO14 | PLO15 | PLO16 | PLO17 | PLO18 |
| CLO1 | | | | | | | | | ✓ | | | | | | | | | |
| CLO2 | | | | | | | | | ✓ | | | | | | | | | |
| CLO3 | | | | | | | | | ✓ | | | | | | | | | |
| CLO4 | | | | | | | | | ✓ | | | | | | | | | |
| CLO5 | | | | | | | | | ✓ | | | | | | | | | |
| CLO6 | | | | | | | | | ✓ | | | | | | | | | |
| CLO7 | | | | | | | | | ✓ | | | | | | | | | |
| CLO8 | | | | | | | | | ✓ | | | | | | | | | |
| CLO9 | | | | | | | | | ✓ | | | | | | | | | |

| Mapping of CLOs to PLOs of Curriculum BIT_IA | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CLO | PLOs | | | | | | | | | | | | | | | | | |
| | PLO1 | PLO2 | PLO3 | PLO4 | PLO5 | PLO6 | PLO7 | PLO8 | PLO9 | PLO10 | PLO11 | PLO12 | PLO13 | PLO14 | PLO15 | PLO16 | PLO17 | PLO18 |
| CLO1 | | | | | | | | | ✓ | | | | | | | | | |
| CLO2 | | | | | | | | | ✓ | | | | | | | | | |
| CLO3 | | | | | | | | | ✓ | | | | | | | | | |
| CLO4 | | | | | | | | | ✓ | | | | | | | | | |
| CLO5 | | | | | | | | | ✓ | | | | | | | | | |
| CLO6 | | | | | | | | | ✓ | | | | | | | | | |
| CLO7 | | | | | | | | | ✓ | | | | | | | | | |
| CLO8 | | | | | | | | | ✓ | | | | | | | | | |
| CLO9 | | | | | | | | | ✓ | | | | | | | | | |

| Mapping of CLOs to PLOs of Curriculum BIT_AI | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CLO | PLOs | | | | | | | | | | | | | | | | | |
| | PLO1 | PLO2 | PLO3 | PLO4 | PLO5 | PLO6 | PLO7 | PLO8 | PLO9 | PLO10 | PLO11 | PLO12 | PLO13 | PLO14 | PLO15 | PLO16 | PLO17 | PLO18 |
| CLO1 | | | | | | | | | ✓ | | | | | | | | | |
| CLO2 | | | | | | | | | ✓ | | | | | | | | | |
| CLO3 | | | | | | | | | ✓ | | | | | | | | | |
| CLO4 | | | | | | | | | ✓ | | | | | | | | | |
| CLO5 | | | | | | | | | ✓ | | | | | | | | | |
| CLO6 | | | | | | | | | ✓ | | | | | | | | | |
| CLO7 | | | | | | | | | ✓ | | | | | | | | | |
| CLO8 | | | | | | | | | ✓ | | | | | | | | | |
| CLO9 | | | | | | | | | ✓ | | | | | | | | | |

Download All Teacher Material | Download All Student Material

| SessionNo | Topic | LO | ITU | StudentMaterials | S-Download | TeacherMaterials | T-Download | Activity | URLs | LecturerTasks | LTMethod |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Introduction to the course<br>Chapter 1: Introduction<br>1.1 Organization and Architecture | CLO1, CLO2 | | - Slide<br>- Text Book, | CEA201 | - Slide<br>- Text Book, | CEA201 | Do exercises | | | Offline |
| 2 | Introduction to the course<br>Chapter 1: Introduction<br>1.2 Structure and Function | CLO1, CLO2 | | - Slide<br>- Text Book, | CEA201 | - Slide<br>- Text Book, | CEA201 | Do exercises | | | Offline |

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 3 | Assessing exercises of chapter 1<br>Chapter 2: Computer Evolution and Performance<br>2.1 A Brief History of Computers | CLO1, CLO2 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 4 | Assessing exercises of chapter 1<br>Chapter 2: Computer Evolution and Performance<br>2.2 Designing for Performance | CLO3 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 5 | Chapter 2<br>2.3 Multicore, MICs, and GPGPUs | CLO3 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 6 | Chapter 2<br>2.6 Performance Assessment | CLO3 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 7 | Assessing exercises of chapter 2<br>Chapter 3 A Top-Level View of Computer Function and Interconnection<br>3.1 Computer Components | CLO4 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 8 | Assessing exercises of chapter 2<br>Chapter 3 A Top-Level View of Computer Function and Interconnection<br>3.2 Computer Function | CLO4 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 9 | Chapter 3<br>3.3 Interconnection Structures | CLO4 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 10 | Chapter 3<br>3.4 Bus Interconnection | CLO4 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 11 | Assessing exercises of chapter 3<br>Chapter 4 Cache Memory<br>4.1 Computer Memory System Overview | CLO4 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 12 | Assessing exercises of chapter 3<br>Chapter 4 Cache Memory<br>4.2 Cache Memory Principles | CLO4 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 13 | Chapter 4<br>4.3 Elements of Cache Design | CLO4 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 14 | Chapter 4<br>4.3 Elements of Cache Design (cont) | CLO4 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 15 | Assessing exercises of chapter 4<br>Chapter 5 Internal Memory<br>5.1 Semiconductor Main Memory | CLO4 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 16 | Assessing exercises of chapter 4<br>Chapter 5 Internal Memory<br>5.2 Error Correction | CLO4 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 17 | Chapter 5<br>5.3 Advanced Dram Organization | CLO4 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 18 | Chapter 5<br>5.3 Advanced Dram Organization (cont) | CLO4 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 19 | Assessing exercises of chapter 5<br>Chapter 6 External Memory<br>6.1 Magnetic Disk | CLO4 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 20 | Assessing exercises of chapter 5<br>Chapter 6 External Memory<br>6.2 Raid | CLO4 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 21 | Chapter 6 External Memory<br>6.2 Raid (cont) | CLO4 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 22 | Chapter 6 External Memory<br>6.3 Solid State Drives | CLO4 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 23 | Assessing exercises of chapter 6<br>Chapter 7 Input/Output<br>7.1 External Devices<br>7.2 I/O Modules | CLO4 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 24 | Assessing exercises of chapter 6<br>Chapter 7 Input/Output<br>7.3 Programmed I/O | CLO4 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 25 | Chapter 7 Input/Output<br>7.4 Interrupt-Driven I/O | CLO4 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 26 | Chapter 7 Input/Output<br>7.6 I/O Channels and Processors | CLO4 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 27 | Assessing exercises of chapter 7<br>Chapter 8 Operating System Support<br>8.1 Operating System Overview | CLO5 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 28 | Assessing exercises of chapter 7<br>Chapter 8 Operating System Support<br>8.1 Operating System Overview (cont) | CLO5 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 29 | Chapter 8 Operating System Support<br>8.2 Scheduling | CLO5 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 30 | Chapter 8 Operating System Support<br>8.3 Memory Management | CLO5 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 31 | Assessing exercises of chapter 8<br>Chapter 11 Digital Logic<br>11.1- Boolean Algebra<br>11.2-Gates | CLO5 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 32 | Assessing exercises of chapter 8<br>Chapter 11 Digital Logic<br>11.3- Combinational Circuit | CLO6 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 33 | Assessing exercises of chapter 9<br>Chapter 12 Instruction Sets: Characteristics and Functions<br>12.1 Machine Instruction Characteristics | CLO6 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 34 | Assessing exercises of chapter 9<br>Chapter 12 Instruction Sets: Characteristics and Functions<br>12.2 Types of Operands | CLO7 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 35 | Chapter 12 Instruction Sets: Characteristics and Functions cont.<br>12.4 Types of Operations | CLO7 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 36 | Chapter 12 Instruction Sets: Characteristics and Functions cont.<br>12.4 Types of Operations | CLO7 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 37 | Assessing exercises of chapter 12<br>Chapter 13 Instruction Sets: Addressing Modes and Formats<br>13.1 Addressing Modes<br>13.3 Instruction Formats | CLO7 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 38 | Assessing exercises of chapter 12<br>Chapter 13 Instruction Sets: Addressing Modes and Formats<br>13.5 Assembly Language | CLO7 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 39 | Practical Assembly Laguage | CLO7 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 40 | Practical Assembly Laguage | CLO7 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 41 | Practical Assembly Laguage | CLO7 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 42 | Practical Assembly Laguage | CLO7 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 43 | Practical Assembly Laguage | CLO7 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 44 | Practical Assembly Laguage | CLO7 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 45 | Practical Assembly Laguage<br>Assignment introduction (1st program) | CLO7 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 46 | Practical Assembly Laguage<br>Assignment introduction (2nd programs) | CLO7 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 47 | Assessing exercises of chapter 13<br>Chapter 14 Processor Structure and Function<br>14.1 Processor Organization | CLO8 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 48 | Assessing exercises of chapter 13<br>Chapter 14 Processor Structure and Function<br>14.2 Register Organization | CLO8 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 49 | Chapter 14 Processor Structure and Function<br>14.3 Instruction Cycle | CLO9 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 50 | Chapter 14 Processor Structure and Function<br>14.4 Instruction Pipelining | CLO9 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 51 | Assessing exercises of chapter 14<br>Chapter 15 Reduced Instruction Set Computers<br>15.1 Instruction Execution Characteristics<br>15.2 The Use of a Large Register File | CLO9 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 52 | Assessing exercises of chapter 14<br>Chapter 15 Reduced Instruction Set Computers<br>15.3 Compiler-Based Register Optimization<br>15.4 Reduced Instruction Set Architecture | CLO9 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 53 | Assessing exercises of chapter 15<br>Chapter 16 Instruction-Level Parallelism and Superscalar Processors<br>16.1 Overview | CLO9 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 54 | Assessing exercises of chapter 15<br>Chapter 16 Instruction-Level Parallelism and Superscalar Processors<br>16.2 Design Issues | CLO9 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 55 | Assessing exercises of chapter 16<br>Chapter 17 Parallel Processing<br>17.1 Multiple Processor Organizations<br>17.2 Symmetric Multiprocessors | CLO9 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 56 | Assessing exercises of chapter 16<br>Chapter 17 Parallel Processing<br>17.3 Cache Coherence and the MESI Protocol<br>17.4 Multithreading and Chip Multiprocessors | CLO9 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 57 | Assessing exercises of chapter 16<br>Chapter 18 Multicore Computers<br>18.1 Hardware Performance Issues<br>18.2 Software Performance Issues | CLO9 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 58 | Assessing exercises of chapter 16<br>Chapter 18 Multicore Computers<br>18.3 Multicore Organization | CLO9 | | - Slide<br>- Text Book, | | - Slide<br>- Text Book, | | Do exercises | | | Offline |
| 59 | Assessing assigments<br>Review 1 | | | | | | | | | | Offline |
| 60 | Assessing assigments<br>Review 2 | | | | | | | | | | Offline |

27 Constructive question(s)

| | Session No | Name | Details |
|---|---|---|---|
| 1 | 1 | CQ1 | In Figure 1.4 "Computer: Top-Level Structure", in a circle the basic structure of a computer, can the "main memory" component be eliminated? |
| 2 | 2 | CQ1 | Why are computers using Vacuum Tubes heavier than computers using transistors? |
| 3 | 2 | CQ2 | In Figure 2.11 Processor Trends, do you have any comments from 2005 to 2010? |
| 4 | 3 | CQ1 | Table 2.7 Embedded Systems Examples and Their Market, read it carefully, and find a market (or a device) that uses embedded systems other than the examples in table 2.7. Why did you choose that device? |
| 5 | 4 | CQ1 | What general categories of functions are specified by computer instructions. List and briefly define the possible states that define an instruction execution. List and briefly define two approaches to dealing with multiple interrupts? |
| 6 | 4 | CQ2 | Interrupt is a basic and important function of microprocessor, can you give a real life example describing how it works like interrupt? |

| | | | |
|---|---|---|---|
| 7 | 5 | CQ1 | What types of transfers must a computer's interconnection structure (e.g., bus) support. What is the benefit of using a multiple-bus architecture compared to a single-bus architecture? |
| 8 | 5 | CQ2 | In Figure 3.2 Computer components: Top level view, in Main Memory, can we store "data" above "instruction"? |
| 9 | 6 | CQ1 | What are the differences among sequential access, direct access, and random access. What is the general relationship among access time, memory cost, and capacity. How does the principle of locality relate to the use of multiple memory levels? |
| 10 | 7 | CQ1 | What are the differences among direct mapping and associative mapping. For a direct-mapped cache, a main memory address is viewed as consisting of three fields. List and define the three fields. For an associative cache, a main memory address is viewed as consisting of two fields. List and define the two fields? |
| 11 | 8 | CQ1 | What are two interpretations of the term random-access memory. What is the difference between DRAM and SRAM in terms of application. What is the difference between DRAM and SRAM in terms of characteristics such as speed, size, and cost. Explain why one type of RAM is considered to be analog and the other digital? |
| 12 | 9 | CQ1 | What are some applications for ROM. What are the differences among EPROM, EEPROM, and flash memory. How is the syndrome for the Hamming code interpreted. How does SDRAM differ from ordinary DRAM? |
| 13 | 10 | CQ1 | What are the advantages of using a glass substrate for a magnetic disk. How are data written onto a magnetic disk. How are data read from a magnetic disk. Define the terms seek time, rotational delay, access time, and transfer time? |
| 14 | 11 | CQ1 | What common characteristics are shared by all RAID levels. Briefly define the seven RAID levels. How is redundancy achieved in a RAID system. In the context of RAID, what is the distinction between parallel access and independent access? |
| 15 | 12 | CQ1 | List three broad classifications of external, or peripheral, devices. What is the International Reference Alphabet? Give an example. What are the major functions of an I/O module. List and briefly define three techniques for performing I/O? |
| 16 | 13 | CQ1 | What is the difference between memory-mapped I/O and isolated I/O. When a device interrupt occurs, how does the processor determine which device issued the interrupt. When a DMA module takes control of a bus, and while it retains control of the bus, what does the processor do? |
| 17 | 14 | CQ1 | List and briefly define the key services provided by an OS. List and briefly define the major types of OS scheduling. What is the difference between a process and a program. What is the purpose of swapping? |
| 18 | 15 | CQ1 | If a process may be dynamically assigned to different locations in main memory, what is the implication for the addressing mechanism. Is it necessary for all of the pages of a process to be in main memory while the process is executing. Is it necessary for the pages of a process in main memory to be in sequential order. What is the purpose of a translation lookaside buffer? |
| 19 | 17 | CQ1 | List and briefly explain five important instruction set design issues. What types of operands are typical in machine instruction sets. What is the relationship between the IRA character code and the packed decimal representation. What is the difference between an arithmetic shift and a logical shift? |
| 20 | 18 | CQ1 | Why are transfer of control instructions needed. List and briefly explain two common ways of generating the condition to be tested in a conditional branch instruction. What is meant by the term nesting of procedures. List three possible places for storing the return address for a procedure return? |
| 21 | 19 | CQ1 | What is the advantage of autoindexing. What is the difference between postindexing and preindexing. What facts go into determining the use of the addressing bits of an instruction. What are the advantages and disadvantages of using a variable-length instruction format? |
| 22 | 24 | CQ1 | What general roles are performed by processor registers. What categories of data are commonly supported by user-visible registers. What is the function of condition codes. What is a program status word? |
| 23 | 25 | CQ1 | Why is a two-stage instruction pipeline unlikely to cut the instruction cycle time in half, compared with the use of no pipeline. List and briefly explain various ways in which an instruction pipeline can deal with conditional branch instructions. How are history bits used for branch prediction? |
| 24 | 26 | CQ1 | What are some typical distinguishing characteristics of RISC organization. Briefly explain the two basic approaches used to minimize register-memory operations on RISC machines. If a circular register buffer is used to handle local variables for nested procedures, describe two approaches for handling global variables. What are some typical characteristics of a RISC instruction set architecture? |
| 25 | 27 | CQ1 | What is the essential characteristic of the superscalar approach to processor design. What is the difference between the superscalar and super pipelined approaches. What is instruction-level parallelism. What is the distinction between instruction-level parallelism and machine parallelism? |
| 26 | 28 | CQ1 | List and briefly define three types of computer system organization. What are the chief characteristics of an SMP (symmetric multiprocessor). What are some of the potential advantages of an SMP compared with a uniprocessor. What is the difference between software and hardware cache coherent schemes? |
| 27 | 29 | CQ1 | Summarize the differences among simple instruction pipelining, superscalar, and simultaneous multithreading. Give several reasons for the choice by designers to move to a multicore organization rather than increase parallelism within a single processor. Why is there a trend toward giving an increasing fraction of chip area to cache memory. List some advantages of a shared L2 cache among cores compared to separate dedicated L2 caches for each core? |

3 assessment(s)

| Category | Type | Part | Weight | Completion Criteria | Duration | CLO | Question Type | No Question | Knowledge and Skill | Grading Guide | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Assignment | on-going | 2 | 30.0% | >0 | Option 1: At home Option2: (For Constructivism Approach only): Follow lecturer's proposal | | Option 1: Developing Assemly program Option 2 (For Constructivism Approach only): Follow lecturer's proposal | Option 1: 2 Option 2 (For Constructivism Approach only): Follow lecturer's proposal1: 2 Option 2: Follow lecturer's proposal | Basic programs | Teachers assess their works on their computers | 30% of total progress mark |
| Exercises | on-going | 4 | 30.0% | >0 | Option 1: N/A Option2: (For Constructivism Approach only): Follow lecturer's proposal | | Option 1: Writing Option 2 (For Constructivism Approach only): Follow lecturer's proposal | Option 1: Depends on chapters Option 2 (For Constructivism Approach only): Follow lecturer's proposal1: Depends on chapters; Option 2: Follow lecturer's proposalon chapters | Studied chapters; knowledge and skills | Students write answers to their notebook | 30% of total progress mark |
| Final exam | final exam | 1 | 40.0% | 4 | 60' | | Multiple choice | 50 | All chapters; knowledge and skills of digital system; | by Exam board | 40% of total progress mark |