# Survey of new trends in Industry for Programmable hardware: FPGAs, MPPAs, MPSoCs, Structured ASICs, eFPGAs and new wave of innovation in FPGAs

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## Abstract

***We will present a survey of trends in the semiconductor industry for programmable hardware. The main objective of this paper is educational and the focus is FPGAs and its related or vs technologies which have emerged mostly in the second half of the last decade. We will try to analyze what were the prominent reasons for emerging of these technologies. What are the advantages and drawbacks of them, what makes FPGAs still most dominant in this area and will it be same or change in future. FPGAs themselves during this time have dramatically changed and the classical term FPGA does not fully characterize in name what FPGAs have actually become now. These changes and the continuing rising strength of multicore and ultimate power consumption challenge in industry will have what impact. Will these technologies collide or co-exist in future (nobody in industry or academics knows that and it is hard to predict). We will try to present the distinguishing technical and commercial potentials of different technologies which give an edge of one over the other.***

## 1. Introduction

Field Programmable Gate Arrays (FPGAs) have been known as the de facto symbol of prototyping and the reconfigurable computing. The idea of reconfigurable computing goes back to 1960s. Gerald Estrin made a land mark paper of the early concepts of reconfigurable computing with processor and reconfigurable hardware array. Several researches followed the concept mostly in academics and also in industry [1][2][3][4]. However it actually became a reality by the dawn of strength of FPGAs in industry that realizations and experimentation of the theories of reconfigurable computing became possible in reality.

The semiconductor industry in all its history has not seen anything that can match a microprocessor or FPGA in terms of versatility and heterogeneity of potentials. Not long ago in the beginning of the last decade the reconfigurable computing research community fell in a serious crush on coarse-grain reconfigurable hardware and FPGAs. Computation in time vs computation in space [3] was a major focus. Research and Industrial community were taught how bad and slow were Von Neumann approach and how parallel and fast these new architectures are. It was a nice time and horrors of power consumption was not a major concern and clock frequencies were rising higher and higher. As Moore's law passed the 90nm node all what people were planning and thinking for future changed. It was the time of industrial birth of Multicore (Intel's move to multicore was paradigm shift signal to industry and exemplified the upcoming challenges of power consumption). Von Neumann once again came back as a "hero" to the community telling us that he as a team in form of multi/many cores can compete with FPGAs and exploit features of non Von Neumann coarse-grained reconfigurable architectures. That opened a new portal of research and products for academics and industry including progress of Network on Chips (NoCs).

By the end of last decade several enhancements were done in both the FPGAs and this new area of multicore-like solutions including product launches and the technologies are continuously improving making them competitive solutions in many areas. If we look at the versatility of processors and FPGAs, historically several marriage attempts of them have been done by academics and industry, either directly or in form of new architectures exploiting the fundamental principles. This has a painful history and so many have failed [3][4][6][7]. The prominent successful example of industrial success in this regard is the inclusion of processors inside the FPGAs (in soft or hard form). We will try to address this issue in context of roadmaps of FPGA giants to understand what might be the major reasons of success of such approach compared to many theoretically similar concepts which failed (Processor inside FPGA vs FPGA inside Processor).

This paper is an educational survey in this area for students and researchers. We will present the fundamental benefits and features of FPGAs. We have made this research jointly with academics and industry so one of our major contributions is that we will try to present both the technical and commercial aspects. We will try to analyze the reasons why some technologies apparently more innovative often fail to an old conservative one. We will explore what are the prominent reasons behind them and what is their significance.

As it is not possible to cover the breadth of semiconductor industry we have kept strong focus only on FPGAs and the emerging technologies which are similar to FPGAs in terms of architecture and target market segment. Furthermore we have only considered industrial solutions in this work. A good example and overview of academics work can be found in [3][4], and a detailed survey in the historical advancement of programmable logic devices can be found in [5]. The industrial references are carefully chosen based on quality, up

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to date and their cumulative references. They provide basic insights to industry news and information flow structure.

The theme and organization of the rest of the paper is as follows. Section 2 will present the strongest potentials of FPGAs along with their weaknesses which created opportunities for other solutions. In section 3 for completion of scenario we will discuss structured ASICs which are similar to FPGAs in architecture and offer an interesting tradeoff between FPGAs and ASICs for low to average volumes. Section 4 will discuss theme of the emerging technologies which have tried to take the niche from FPGA market share. We will show how these technologies have been inspired by FPGAs and have used the Multicore concept to compete with FPGAs. Section 5 will provide a brief overview of the new FPGA startup companies that have emerged in the past few years. Section 6 will give a glimpse of the high-end heterogeneous MPSoC Platforms. Section 7 will present what FPGA vendors have learned in all these years form their challenges and emerging competitions and how they are adapting to it for their future devices. We will briefly discuss technological and commercial edge of Processors inside FPGAs vs FPGAs inside processors in context of roadmaps of FPGA vendors. Finally in section 8 we will conclude.

## 2. FPGAs: Fundamental pros and cons

**Standard RTL Programming flow**

Since their invention in mid 1980s the fundamental target and objective of FPGAs has remained the field programmable capability of prototyping the ASICs. Based on that the model of programming FPGAs is inherently HDL. It is the foundation source of designing the ASICs, is highly mature and industry standard with state of the art tools support.

**FPGAs have become Programmable Platforms**

Moore's law is the major driving source for all the industry and is particularly important for giant semiconductor companies, FPGAs success has also been highly attributed to it. Like intel for microprocessors, the FPGA vendors are also always among the first adopter on new technology node and remain ahead in this regard to most of the remaining segments of industry, the regular nature of FPGA architecture provides them added scaling edge. Both de facto FPGA giants (Xilinx and Altera) are hitting 28nm at end of 2010. By continuously following Moore's law and architectural upgrades based on changing market needs FPGAs have now become capable of implementing entire SoCs. In fact they have turned now in a complex heterogeneous mix of coarse-grain elements and classical fine grained LUTs. The term FPGA (Field Programmable Gate Arrays) no longer correctly justify the capabilities of modern FPGAs. As an example Xilinx has already started the term Programmable Platforms for its devices. Figure 1 shows abstract diagram of 40nm Stratix IV device of Altera. The complexity and heterogeneity of blocks used in the device can be seen in it and can be noticed that the classical fine grain FPGA fabric is highly accompanied by heterogeneous blocks of dedicated functionalities.

**Universal nature due to prototype capability**

The strongest strength of FPGAs is that they have universal capabilities due to their prototype ability and HDL programming model. This is not true for a microprocessor. This power helps FPGAs absorb complex functionalities in form of Hard Macro blocks. It can be a processor, an IP or anything else. Since the programming model is HDL it gives instant usability of the component without any burden of new standards or languages. Highly mature in-house or 3rd party synthesis tools are available due to standard RTL flow.

**IP eco-system is RTL dominated**

The RTL flow of FPGAs provides an added benefit to IP eco-system of the industry. It is easier to port IPs both for ASICs and FPGAs as both uses RTL. This also holds true for FPGAs of different vendors because they all use RTL flow so porting the design to another FPGA is not extremely complicated like it is in microprocessors where legacy code plays a high role in its success and market dominance.

Furthermore as RTL is inherently parallel, mapped application is automatically optimally parallelized by CAD (Computer Aided Design) tools utilizing the best of the target hardware resources (this still is one of major difficulty for multicore/multicore-like solutions). Finally as FPGAs are the closest mediums of having the ASICs on a programmable platform it is relatively easy for FPGA vendors to turn any functionality into a dedicated hard macro block. Figure 1 shows how much this has evolved with time.

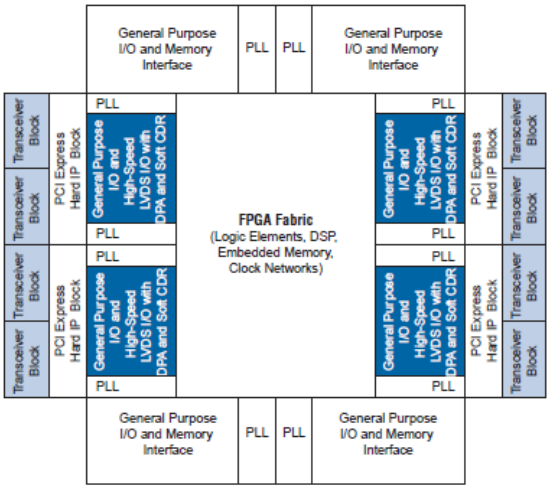


Fig. 1: Stratix IV 40nm FPGAs of Altera (Source: Altera web)

**FPGAs vs ASICs gap, power is major issue**

On the down side, the immense programmable and prototype capabilities come with a very high price in terms of Area, Power and Speed which makes FPGAs in many cases too hard to be used as a product. It has been shown by research that FPGAs have a gap of around 30-40X in terms of Area, 12-14X in terms of Power and 4-5X in Speed when compared to an ASIC [8]. It can be seen that the gaps are very high and very different for the three categories. First the biggest one is in area, this somehow gets slightly compensated by the fact that FPGAs are always a few generations ahead in

Moore's law and since they are programmable devices for large segment of clients they have mass production which further helps to reduce the cost. For timing sometimes using the parallel nature of FPGAs some exploitation can be tried with tradeoff in Area and Power. However the critical aspect certainly lies in power consumption that is now considered a major challenge in ASICs and therefore surely becomes further prominent in FPGAs. This is the hardest challenge for FPGAs [8]. As the architecture of FPGAs is inherently made with huge flexibility of prototyping, it is relatively difficult for FPGAs to take full leverage of the advanced power management schemes used in latest SoCs like DVFS (Dynamic Voltage and Frequency Scaling), clock gating, GALS (Globally Asynchronous Locally Synchronous) etc. It is there where the emerging technologies can have an edge above FPGAs due to coarser grain nature and programming style which have some superior potentials to exploit the latest advancements in the above mentioned power management techniques. Because no matter how many Hard Macros FPGAs absorb in them they have to maintain their original dominating potential of prototyping and target a wide segment of market which makes them low cost.

## 3. Structured ASICs

Structured ASICs are the class of devices based mostly on FPGA-like architecture and have special configuration mechanism to program the device at mask level. This greatly reduces the cost and provides enhanced performance, however once created it is not re-programmable. eASIC is a prominent example in this regard. Both Xilinx and Altera also propose similar solutions for mass production, Easy Path and Hard Copy respectively. The details can be easily analyzed on the websites of the mentioned companies.

## 4. Multicore and Massively Parallel Processor Arrays (MPPAs)

### From fine grain to coarse-grain

In previous sections we saw that FPGAs have a high silicon penalty due to very high flexibility. The fundamentals of FPGA architecture are well known. The central processing element of an FPGA is a Look Up Table (LUT) which allows implementation of any kind of Boolean function (whereas ASIC use hardwired logic gates). To ensure high flexibility of interconnecting these LUTs requires huge amount of routing composed of programmable switches and configuration for them which take significant area of the device. This gave rise to new architectural concepts where the focus was to decrease the degree of fine grained flexibility of FPGAs to a coarser grained one and furthermore application specific which was inherent as when we change the level of flexibility the application domains narrow. However the resulting solutions are orders of magnitude better in performance, power and cost when compared to general purpose FPGAs.

### Competition with well established market leaders

Several innovative solutions have been proposed in this area and are still coming up. It is however well known that majority of them failed to compete FPGAs due to several technical and commercial reasons. It is not possible to discuss all these solutions here, a detailed industrial survey can be found in [6][7]. In [4] authors have also covered similar issues including several academic approaches and have finally concluded in favor of FPGAs. The failure reasons are more commercial than technical. The market dominance of well established players [7] has kept the competition stakes quite high for new entrants, companies with low differentiations badly failed; in comparison innovative startups with strong differentiations succeeded to either find a niche from market or got acquired by a bigger company which bought them to strengthen its products portfolio or existing technology.

### Importance of Standards in Industry

Most of these new technologies were/are novel and require some special constraint of programming to optimally utilize their hardware. This makes it very hard for the industry to adapt it as there is no standard behind it. Due to that these solutions can neither give/take benefit to/from the IP eco-system nor the standard ANSI C/C++. With FPGAs or successful multicore-like solutions it is obvious that programming is always HDL or ANSI C/C++ and now ESL (Electronic System Level) at industrial level is bridging HDL and ANSI C/C++. Companies coming up with solutions with some constrained flavor of a subset or new language find it is quite hard to convince industry and customers to adapt to that new language flavor. The companies see that as a risky investment of their resources to use it. In section 5 we will discuss several FPGA startups and will see that all of them despite if some of them propose something very new are strictly following the standards.

### Example Solutions

We present two examples of solutions in this area to briefly highlight the points we discussed above, a detailed overview of several companies, their solutions and business status can be seen in [6]. Detailed analysis about MPPAs and MPSoCs can be found in the article from Ambric [10].

Figure 2 shows an example of coarse-grain architecture from MathStar (www.mathstar.com). The device is a fine example of coarse-grain reconfigurable architectures. The functional unit in this device instead of LUT is a small ALU. They call their device FPOA (Field Programmable Object Array). From the figure it can be seen that the design style is similar like the regular Island style of FPGAs like in Xilinx e.g. Other than ALUs the device also contains memory and MAC blocks for signal processing. Due to coarse-grain nature and their patented interconnect architecture these FPOAs can run in frequency of 1GHz. When we come on the programming side the device is programmed in an abstract block levels using tools from Mentor Graphics called Visual Elite. Programming this device in an optimal manner is done in a non standard way which makes it relatively difficult to use compared to FPGAs. However the technology is very innovative and for specific applications they demonstrate their solution compared to an FPGA is better.

Figure 3 shows the Tile64 device of Tilera Corporation (www.tilera.com). It is a nice example of massively parallel processor arrays. The architecture style is again regular like FPGAs. In case of Tilera each tile is a processor core which can run a full operating system, or multiple tiles together can run a multi-processing operating system like SMP Linux. The processor cores are connected by their iMesh on-chip network. Their programming tools suite MDE (Multicore Development Environment) provides ease of programming with ANSI C/C++. They have developed several tools to take the leverage of multicore hardware and ease of debugging and profiling. Among some other notable companies doing successful innovations [6] are picoChip (specific for wireless networks), Silicon Hive etc.

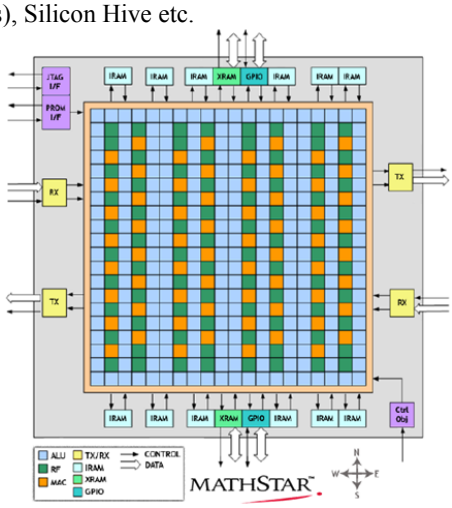


Fig. 2: MathStar FPOA (Source: MathStar web)

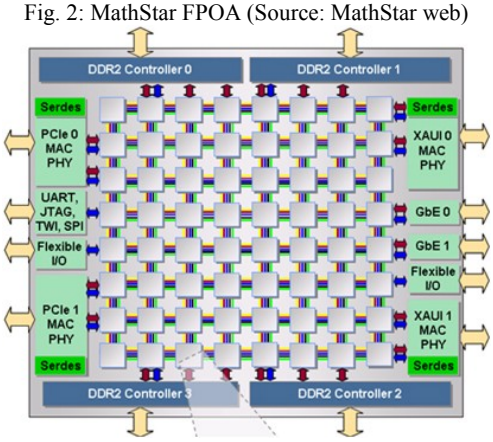


Fig. 3: Tile64 of Tilera (Source: Tilera web)

## 5. FPGAs Startups, their differentiations

In the last few years several new FPGA startup companies have emerged [7] despite the well known failure history of startups in this area. This trend also indicates that there is still room for new innovations in this area. In this section we show key features of these startups. We present what are their prominent differentiation claim points for finding a niche in FPGAs market share. For the design tools all these companies have a standard RTL flow design like classical FPGAs. Another interesting point to note is that majority of the FPGA companies (established and emerging) are using or moving to the same Fab that is TSMC. This makes world's largest standalone Fab almost the de facto Fab for all FPGAs in the world. Altera is well known for its long partnership with TSMC since early 90s [11]. Xilinx historically has preferred multi foundry approach. The most recent chips were with partnerships with UMC, Samsung for its high end and low end devices. Xilinx has announced to use TSMC for its 28nm Extensible Processing Platform devices with hard processor blocks of ARM [15], we will discuss it further in section 7.

**Abound Logic (former M2000)**

Abound Logic is focused on creating low cost ultra high density FPGAs for Prototyping, high performance computing and telecom applications. Their current proposed Raptor FPGAs are built on TSMC 65nm and have logic densities in range of 750K LUTs, with numerous hard macro blocks of memories, DSPs, SerDes, Ethernet, PCI etc. The company is also known for providing the embedded FPGA FlexEOS macros a few years back when it was M2000. Their eFPGA is found in the Morpheus project [12]. According to their website it seems that they no longer support eFPGAs. Now their focus is fully on developing configurable logic SoCs.

**SiliconBlue**

SiliconBlue is founded and managed by several ex-employees of Xilinx and Altera. The company has a major focus on low-power FPGAs which can be used for battery-based portable devices. Their iCE65 FPGA devices family is built on low-power TSMC 65nm process. They have done several innovations in packaging and configuration mechanism to make their devices very compact, low-power and single chip solution for the target. Their FPGAs have very low static power. Their FPGAs compared to other providers are relatively small, Logic cells (LUT4+FF) range from 1200 to 16000. They have embedded memory blocks and phase-lock loops (PLL) as hard macros. They also propose their FPGAs in the form of a Die for SIP (System in Package) solutions. One of their most appreciated innovations is a single chip solution. As the FPGA is SRAM based like almost all FPGAs that exist (except ACTEL), making a single chip solution having embedded FLASH is expensive due to complex process needed for Flash. They have used well known non-volatile XPM memories from Kilopass. They are only one-time programmable but have ultra compact size and can be easily fabricated with standard CMOS process. This allows SiliconBlue to provide a low cost single chip FPGA solution. By far among all the new FPGA startups SiliconBlue is most successful and their devices are in mass production.

**Achronix**

Achronix is the first FPGA to be commercially launched which is different from conventional architectures. They have developed Asynchronous FPGAs. This allows very high speed operations. According to the company they claim to deliver world's fastest FPGAs with frequencies up to 1.5GHz. Their Speedster family of FPGAs is fabricated on TSMC 65nm process. Their logic densities go up to 164K LUTs. In addition they have hard blocks of memory, multipliers,

SerDes, PLLs and memory controllers. Their CAD tools suite ACE (Achronix CAD Environment) provides a seamless classical RTL tools flow for the programmer by hiding all the effects of Asynchronous FPGA hardware. Their target market segments are Networking, Telecommunication, DSP, High performance computing, military and aerospace etc.

**Tabula & Tier Logic with 3D FPGAs**

In March 2010 two FPGA startup companies launched their products. Currently detailed information about the technology and architectures are not openly available. Both companies have made devices beyond classics like Achronix.

Starting from Tabula their technology can be considered as a masterpiece of dynamic reconfiguration. The device is not physically 3D in manufacturing; they call the time as 3rd axes. By this advantage their ABAX 3PLD devices fabricated on 40nm TSMC process when compared to an equivalent classical 2D FPGA have gains of around 2.5X in logic density, 2.0X in Memory and 3.7X in DSP performance. More importantly as stated before despite of the architecture which is completely un-natural physically, the programming model according to the company is purely standard RTL based. Their 3D Spacetime Compiler makes this possible.

Tier Logic has actually fabricated a 3D device. Their groundbreaking innovation is that they have completely removed the configuration SRAM cells from the silicon and implemented them on top of the Metal layers using Thin Film Transistor (TFT) technology from TOSHIBA. This allows to almost double the logic density of the FPGA fabric as the millions of SRAM configuration cells are no longer there. This also helps in increased performance and power saving. The major benefit they propose lies in the fact that the configuration is on the top of device, it is therefore very easy to transform the device to an ASIC (Structured ASIC concept) by just removing the SRAM layer and replacing it with programming the metal layer while keeping same timing.

**Menta**

Menta is the newest FPGA startup in these new companies and is in its early research state. Founded in 2007 in Montpellier, France the company is specifically focused on embedded FPGAs (eFPGAs). The objective of the company is to create highly customized domain specific eFPGAs for market segment of ASICs and ASSPs so the target market segment is different than of FPGAs. The technology is highly scalable and target independent, so customers can immediately take benefit of having eFPGA in their system and based on the need of target market constraints can go for a custom solution for a specific node. For many market segments for ASIC/ASSP it is difficult for the companies to fully migrate to an FPGA solution to get flexibility. eFPGAs provide a fine medium in bridging the full FPGA and full ASIC solutions. The architecture of eFPGA like all other FPGA companies is classical and standard RTL programming flow is used bringing the inherent benefits of it.

The eFPGA Creator tools suite of the company allows creation of customized eFPGA Core in a user friendly GUI environment which with its built in analysis tools and close coupling with backend silicon tools helps to build, analyze and validate the architecture to fine tune it to target needs. In addition to that the company with close collaboration with LIRMM (University of Montpellier) is working on use of MRAM (Magnetoresistive Random Access Memory) for non volatile configuration and superior architectural benefits for partial/dynamic reconfiguration, multi-context compared to SRAM and FLASH with ease of fabrication with standard CMOS process compared to FLASH.

## 6. Heterogeneous MPSoC platforms

So far we have seen several programmable architectures found in industry which are FPGAs or FPGAs-like. In this section we will briefly discuss the high-end SoCs in industry whose market share is much higher than FPGAs and other similar technologies. Such products are usually from IDMs (Integrated Device Manufacturers) or giant fabless companies. Figure 4 shows the well-known OMAP4 platform from TI, similar competitive products are made by Samsung, Qualcomm, Broadcom etc. These products have to ship in ultra high volume and have to face strong challenges of consumer electronics products, their design is complex, heterogeneous and application oriented. However even at that level it is highly desirable to have some post manufacturing flexibility to amortize the high development cost of these SoCs to several end products. Currently the processor (single or multicore) is the main source of flexibility by software.

Some interesting observations can be made based on fig. 1, fig. 4. FPGAs through time have continued to go more heterogeneous to decrease the gap with the SoCs, their superset prototyping nature has greatly helped them in this regard. They started with full fine grain devices and with time other than getting general purpose heterogeneous (with hard blocks of memories and multipliers) they started getting platform oriented by providing more than one kind of FPGAs based on the target market. Xilinx is a pioneering example of it with its targeted Platforms. Even with these innovations there is still a long road to go when FPGAs become a real competitive threat to these SoCs. Will FPGAs ever reach that place in future or should FPGAs ever reach that point is a complicated issue both technologically and commercially. However it's quite true that it helps FPGAs acquire more and more market share of ASICs and ASSPs hence leaving behind only the very high-end SoCs to really justify the enormous cost which is spent making them.

At this point we can also see the most challenging battle between FPGAs vs MPSoC like platforms at present. It is RTL vs Software programming. Right now industry is highly hardware dominated and there is a vast IP eco-system fundamentally based on RTL and FPGA vendors take leverage of it. However MPSoC like platforms have some superior properties compared to hardware FPGAs, like ease of programming which currently is struggling as there is still no standard to meet well developed RTL flows, significant efforts are on their way in Industry and academics to address this issue. In [13] a good overview of the challenges involved

with programming of multicore and the efforts on the way to address them with open solutions like OpenMP (www.openmp.org) and several tools from Intel to help programmers exploit its multicore processors is discussed. ESL will further play a major role and in itself represents that people want/like to write software compared to hardware. There is a lot of effort underway by EDA vendors and academics how to make programming for multicore easier and efficient. It might be possible that in few years a standard becomes for it which can benefit emerging technologies like MPPAs which use a smaller RISC machines compared to high end processors to exploit more parallelism (Thin vs Thick or Fat vs Slim processor cores). Currently the major focus of industry is to get tools for the high-end Multicore market processors like Intel/AMD, ARM etc. These companies are slowly and carefully increasing their cores keeping consideration of their legacy software and tools maturity.

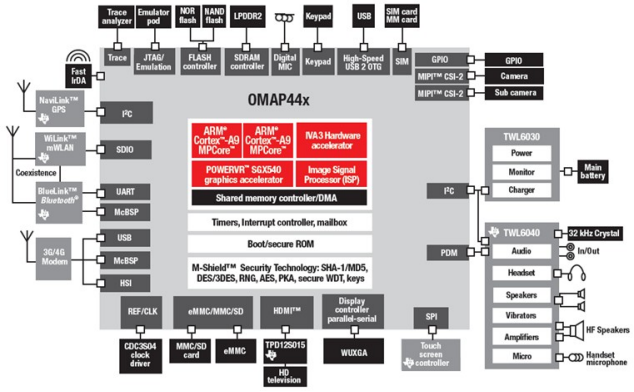


Fig. 4: Texas Instruments OMAP4 (Source: TI web)

## 7. New roadmaps of FPGA giants

In previous sections we covered the fundamental strengths and weaknesses of FPGAs. We saw how new technologies evolved and tried to address specific market segments where they can provide a better solution compared to FPGAs by using the weakness of FPGAs as their strength. However FPGAs also have dramatically changed with time and the FPGA vendors are well aware of the pros and cons of their technology. The most recent announcements of FPGA giants of putting Hard processor blocks is a milestone step by FPGAs and response to the competitive technologies. We will only discuss Xilinx here, similar announcements are made from Altera with MIPS and Actel has already launched its latest SmartFusion FPGAs [14] with complete ARM processor and AMBA bus systems as hard silicon.

The announcement of 28nm Extensible Processing Platform [15][16] devices from Xilinx using hard blocks of ARM is based on same paradigm than PowerPC hard processor block in previous devices. But the concept is totally changed for these new devices, they are software centric compared to hardware centric. Figure 5 shows a block diagram showing the principle. It can be seen that there is a complete dual core ARM processor system built in hard logic inside the device which can act stand alone and can boot software at power up and FPGA fabric is configured after that which is opposite to previous devices. The processor has the control over the FPGA fabric part connected by AMBA. This makes the device more like heterogeneous SoCs as discussed in last section (fig. 4). This allows the devices to have significant benefits for high-performance applications like Automotive Driver Assistance, Intelligent Video Surveillance, Wireless Communications, and Industrial etc. [15]. Having the ARM processors brings all the benefit of the software dominance of ARM in embedded systems including OS (Operating Systems) and use of AMBA will help exploit the rich IP eco-system that exists in industry around AMBA. As the processors are hard blocks and the device are fabricated on TSMC it helps leverage the physical processor IP of ARM with benefits of power consumption, and high speed. The dual core ARM processors in the device can run at 800MHz [15]. Other than industry these devices will greatly help academics for new experiments for reconfigurable computing.

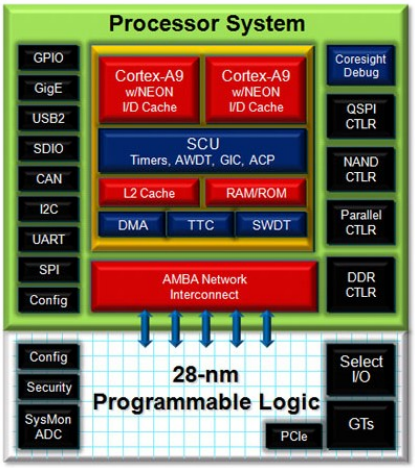


Fig. 5: Xilinx upcoming 28nm EPP devices (Source: EEtimes)

**Processor inside FPGA vs FPGA inside Processor**

At this point one very important factor can also be briefly analyzed; this historically has remained a big failure reason of one approach over the other although theoretically being quite same. When we try to put an FPGA inside a processor (functional unit) some crucial problems arise which have been overlooked or ignored in many previous works. Despite it is the best and most optimal way to get the reconfigurable accelerator, it suffers at least three major flaws which makes it un-acceptable especially for industry in most cases. Firstly it changes the processor Integrity both hardware and software (processor vendors including end customers don't like that). Secondly easy said than done, it is complex to find an effective way of connecting it to the processor and estimating the best size and granularity of the reconfigurable portion. Third in principle it makes the processor guy the solution provider, who has to adapt his processor for every change needed due to reconfigurable portion. The end result in most cases is chaos, it is this and several other reasons that all leading processor companies and SoC vendors never like to

hear or create such solutions. Going the other way around makes the story totally different and is the reason why processors inside FPGA devices (soft/hard) have enjoyed huge success and are now going to next level (figure 5). It makes things lot easier and sound both technically and commercially in comparison for the other way around approach. The processor IP provider fully concentrates on his product differentiation and does not have to make a modified IP for every end customer and due to that all end customers also take the benefit of software dominance of that processor. The FPGA companies based on their target market create products which combine the benefits of software and their reconfigurable hardware [14][15]. The complex functions can be moved to the reconfigurable part and acts like an IP to the processor; furthermore ESL is helping to auto transform the software to hardware conversion and will get further improved in future helping software developers especially.

The concept further extends for SoC providers also; they can take leverage of same concept to differentiate their products by using in house or 3rd party eFPGA providers who are fully focused on differentiation of their IP like processor companies. An example of this concept was shown by [12].

## 8. Conclusions & Future

In this paper we tried to address different emerging trends in industry for programmable hardware. We discussed the historical importance and relationship between processors and FPGAs, the prominent points which make FPGAs a dominant choice when it comes to programmable logic. FPGAs have immense configurability power but this power comes at a heavy silicon price which makes FPGAs difficult to be adopted in some products despite the need of flexibility. We saw competitive technologies which have emerged to address the down sides of FPGAs. We tried to analyze why many of new technologies fail, what usually are the primary reasons for that. They also serve as guidelines for new-comers and researchers to address the point that, the complexity level of challenges and requirements in industry have become so high that innovation in just one segment which has conflict with several other segments makes it very hard to actually succeed. So it is very important to follow standards. We discussed several new startup companies in the area of FPGAs and saw what are their differentiating potentials compared to well established market leaders. We saw that they are following the standards even if some have unconventional device.

We discussed one of the high-end Programmable platform SoCs in the industry to have a feeling how these complex heterogeneous systems look like and what analogy they have with FPGAs and emerging MPSoC like platforms. We discussed the latest trends and roadmaps of the FPGAs giants in industry and saw how they are taking full advantage of the potentials of FPGAs and making the competition stakes higher for new technologies. We tried to briefly address the historical Processor inside FPGA vs other way around issues in technical and commercial scenario and importance of eFPGAs for SoCs to take leverage of the concept like FPGAs.

Looking towards the future, it is hard to predict anything, even industry experts are foreseeing that there will be a platform collision in the industry and it is uncertain who will win/loose, or will they coexist [17]. There are also discussions on Nano Technologies for beyond CMOS scaling [18]. The Semiconductor Industry Empire [19] is split into several segments. FPGAs at present represents roughly about less than 2% of it [7][19]. With new roadmaps of FPGAs and changing trends in industry one thing seems probable that market share of FPGAs will increase in near future. In long term there is one element which will decide/change the shape of the industry "Power Consumption". For portable devices it needs no explanation but it is becoming crucial even for non portable devices (Data Centers, Telecom, Home appliances etc.) due to energy costs and green requirements. It will force industry for innovations in several segments for finding differentiation from each other. Who ever will make a breakthrough in that will rule the future. In that regard FPGAs, MPSoCs and MPSoCs like solutions all will have a tough competition road ahead and Heterogeneity seems imminent in future.

In any case for research community there is a lot to enjoy and explore and this decade will be very prominent for advancement in reconfigurable computing.

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