EE4415 Lab 2: Signal Processing and Fourier Transform

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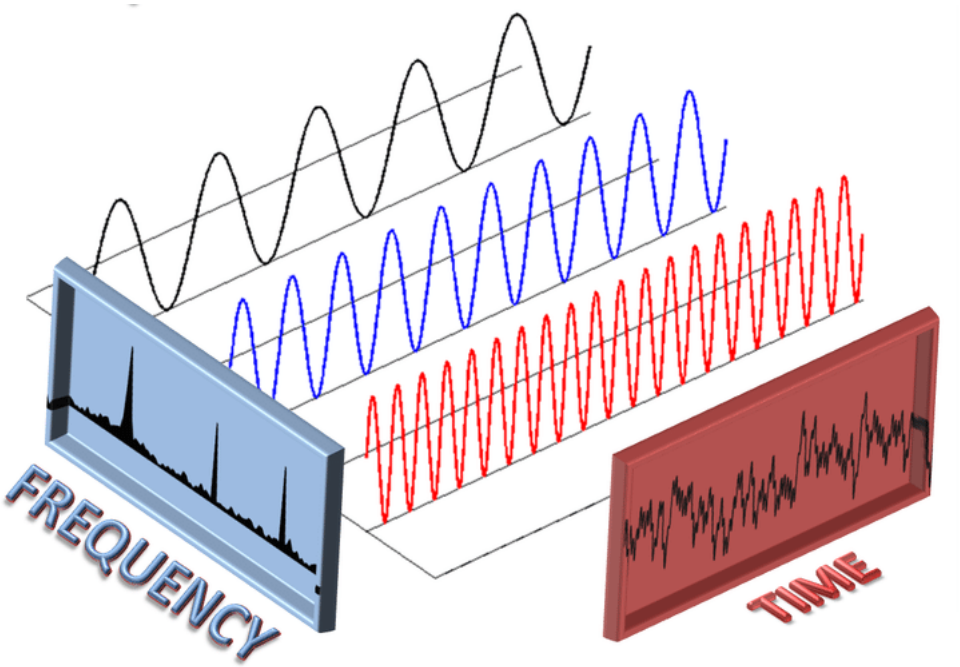
- Introduction
- Working principle of (I)FFT and real application
- Implementation (RTL)
- Lab report
- Quick start

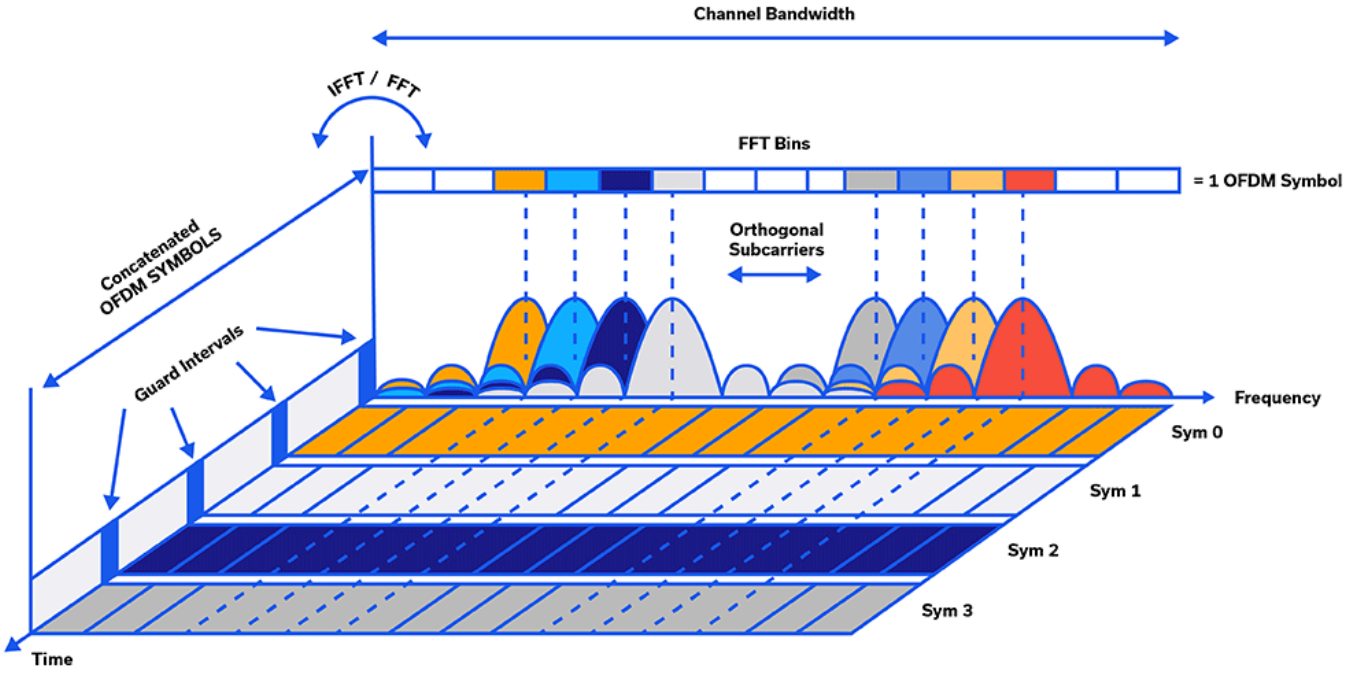
Introduction: (Inverse) Fourier Transform

- The Fourier Transform is a mathematical technique that transforms a function of time, x(t), to a function of frequency, X(ω). Inverse Fourier Transform is the reverse operation of Fourier Transform
  - one of the most important tools in signal processing
  - a tool to analyze signals in another dimension



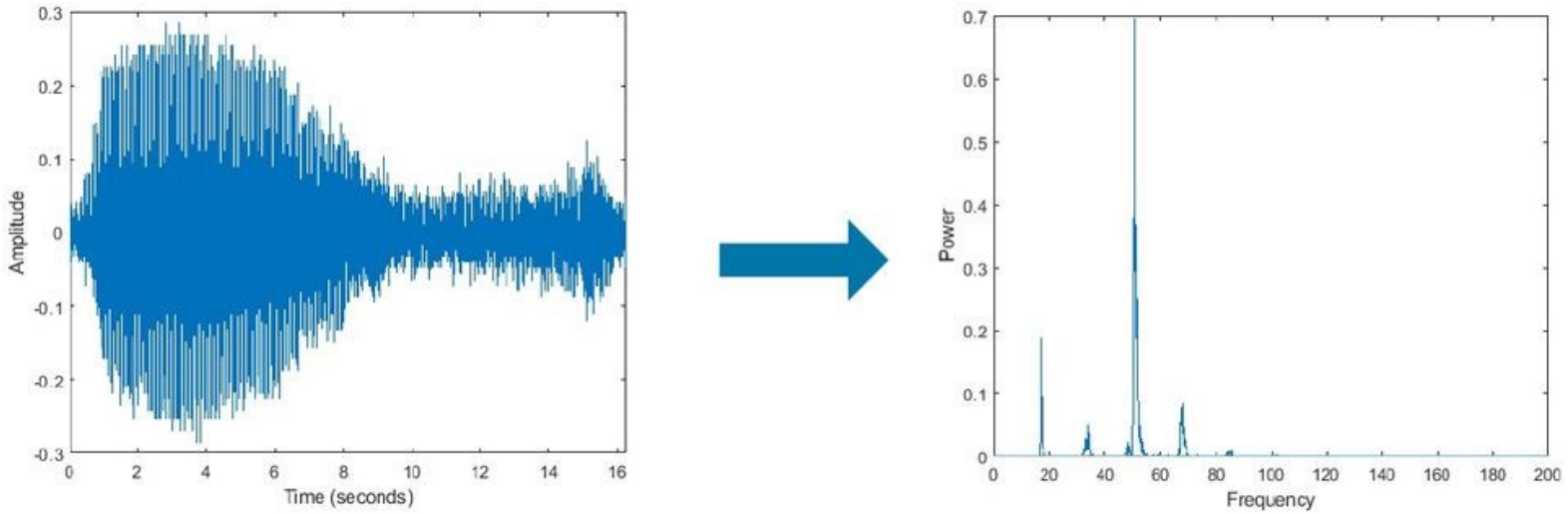
Introduction: (Inverse) Fourier Transform

- Applications:
  - Wireless communication (e.g., OFDM)



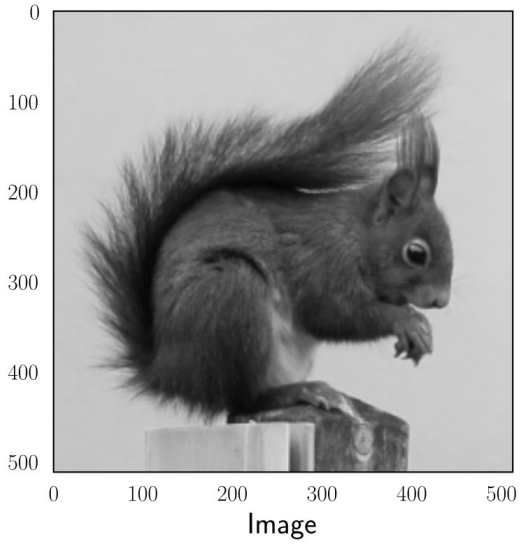
Introduction: (Inverse) Fourier Transform

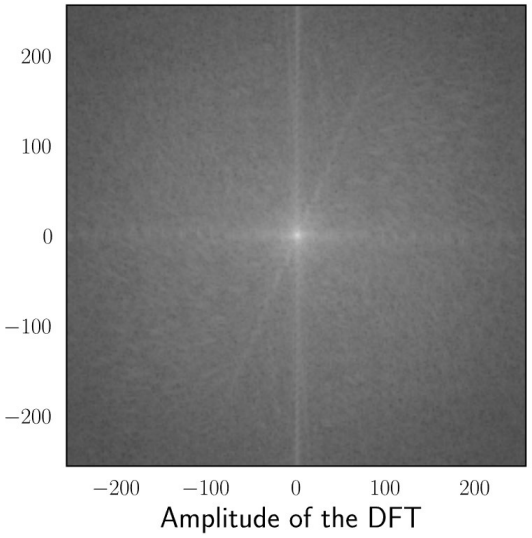
- Applications:
  - Audio processing

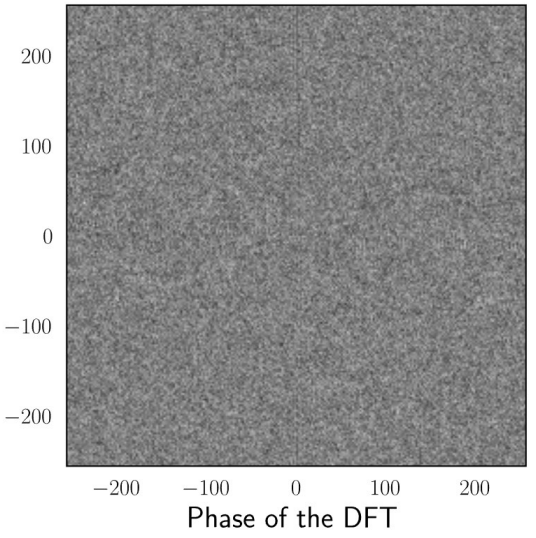


Introduction: (Inverse) Fourier Transform

- Applications:
  - image analysis

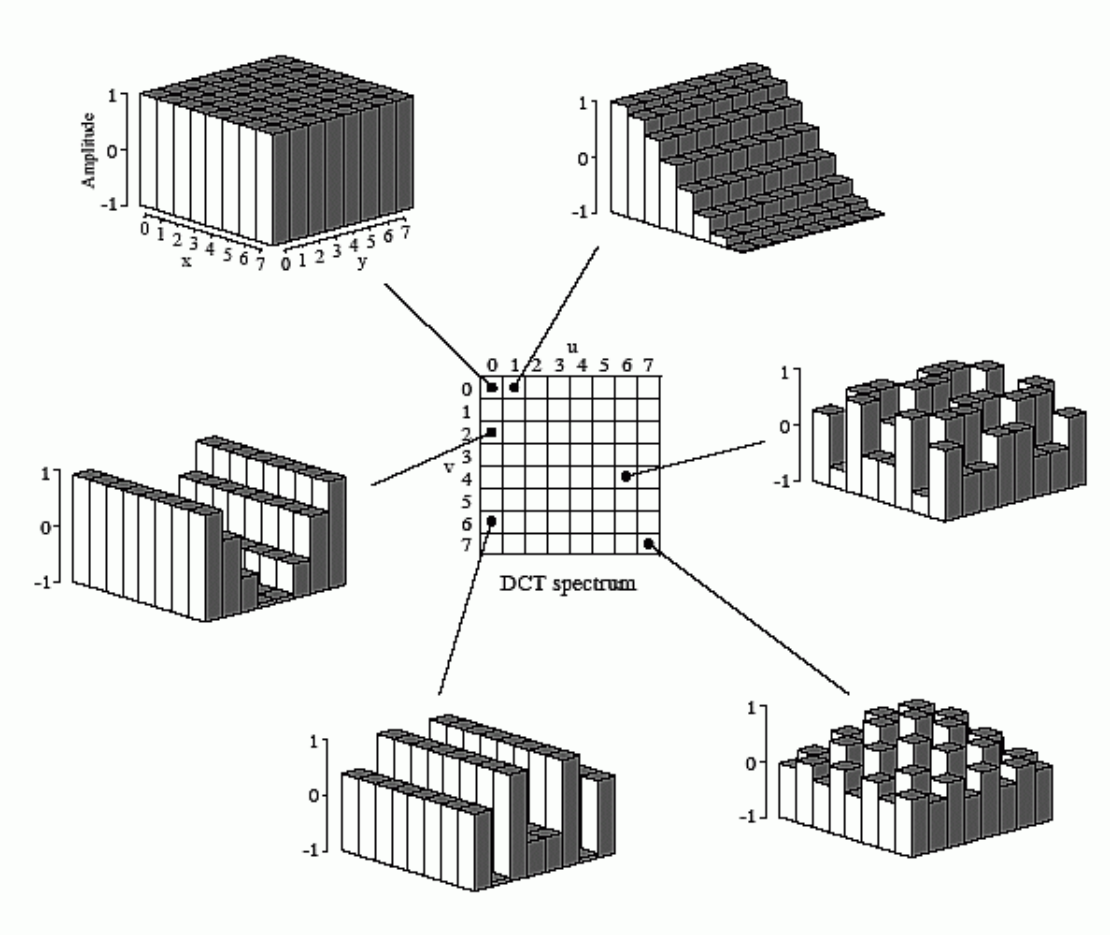






Introduction: (Inverse) Fourier Transform

- Applications:
  - data compression (e.g., JPEG)



(Inverse) Discrete Fourier Transform

- Discrete Fourier Transform (DFT) X_k of an N-point discrete-time signal x_n
  - $N_k = \sum_{n=0}^{N-1} x_n W_N^{nk}, \qquad 0 \le k \le N-1$
    - where W_N^{nk} is a factor equals to $e^{-j2\pi\, nk/N}$
- Inverse Discrete Fourier Transform (IDFT) x_n of an N discrete-frequency points X_k
  - $x_n = \frac{1}{N}\sum_{n=0}^{N-1} X_k W_N^{-nk}, \qquad 0 \le n \le N-1$

(Inverse) Discrete Fourier Transform

- Discrete Fourier Transform (DFT) X_k of an N-point discrete-time signal x_n
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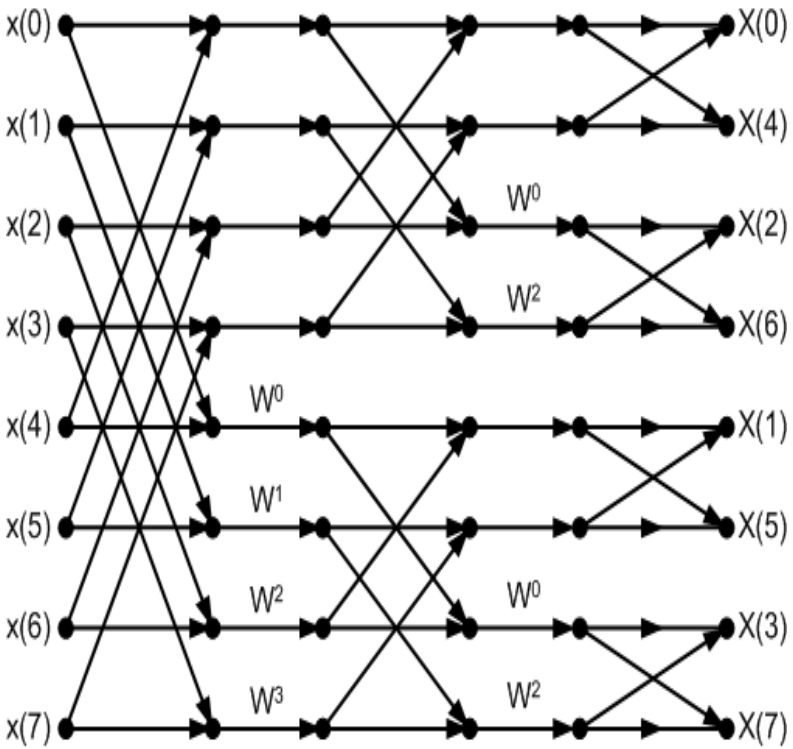
  - $x_n = \frac{1}{N} \sum_{n=0}^{N-1} X_k W_N^{-nk}, \qquad 0 \le n \le N-1$

=> IDFT can be easily implemented by reusing the hardware core/architecture (e.g. complex MAC) of DFT

- w/ a time complexity of $O(N^2)$

(Inverse) Fast Fourier Transform

- (I)FFT decreases the time complex of the algorithm to $O(N\log_2(N))$ through data flow represented by a butterfly diagram
  - sharing and reusing MAC results among outputs

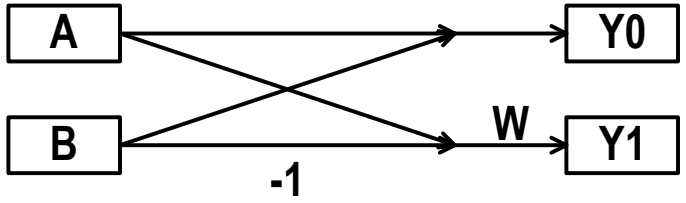


- Example: FFT (N=8)
  - radix = 2
    - #interleaved DFTs a DFT is divided into every stage
  - #stage = 3
    - #stages of DFT interleaves
  - $\text{radix}^{\#\text{stage}} = N$
  - #complex MAC operations
    - 8*3(#stage) = 24
- $O(N\log_2(N)) < O(N^2)$

Basic element of a butterfly diagram: Butterfly unit

- Radix-2 butterfly unit: 2I/2O
  - Y0 = A + B
  - Y1 = (A - B) × W

  => 2 complex adder, 1 complex multiplier

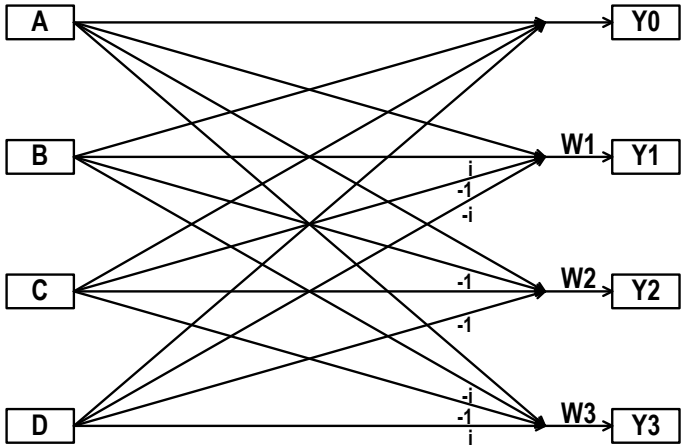


- Radix-4 butterfly unit: 4I/4O
  - Y0 = A + B + C + D
  - Y1 = (A + i×B - C - i×D) × W1
  - Y2 = (A - B + C - D) × W2
  - Y3 = (A - i×B - C + i×D) × W3

  => 3 complex adder, 8 complex multiplier

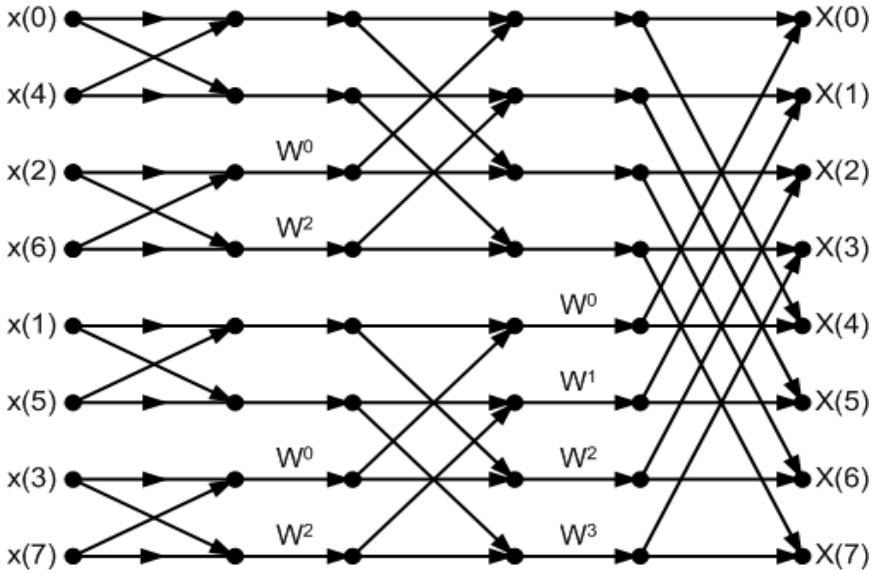
  => 25% less multiplier than Radix-2

  (W are called twiddle factors)

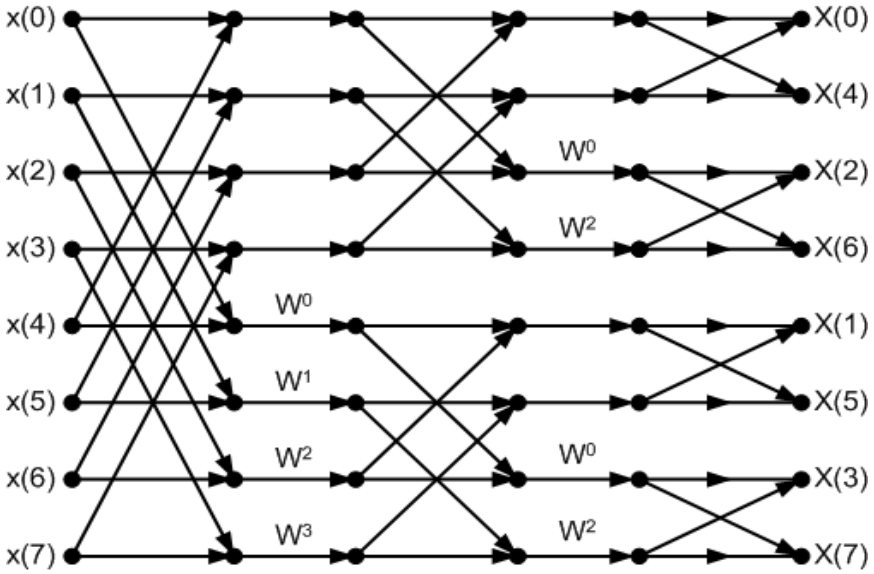


Two types of Butterfly diagram for (I)FFT

- Decimation In Time (DIT)
  - start 2-point DFT from the time-domain side
  - time indices are in bit-reversed order
- Decimation In Frequency (DIF)
  - start 2-point DFT from the frequency-domain side
  - frequency indices are in bit-reversed order



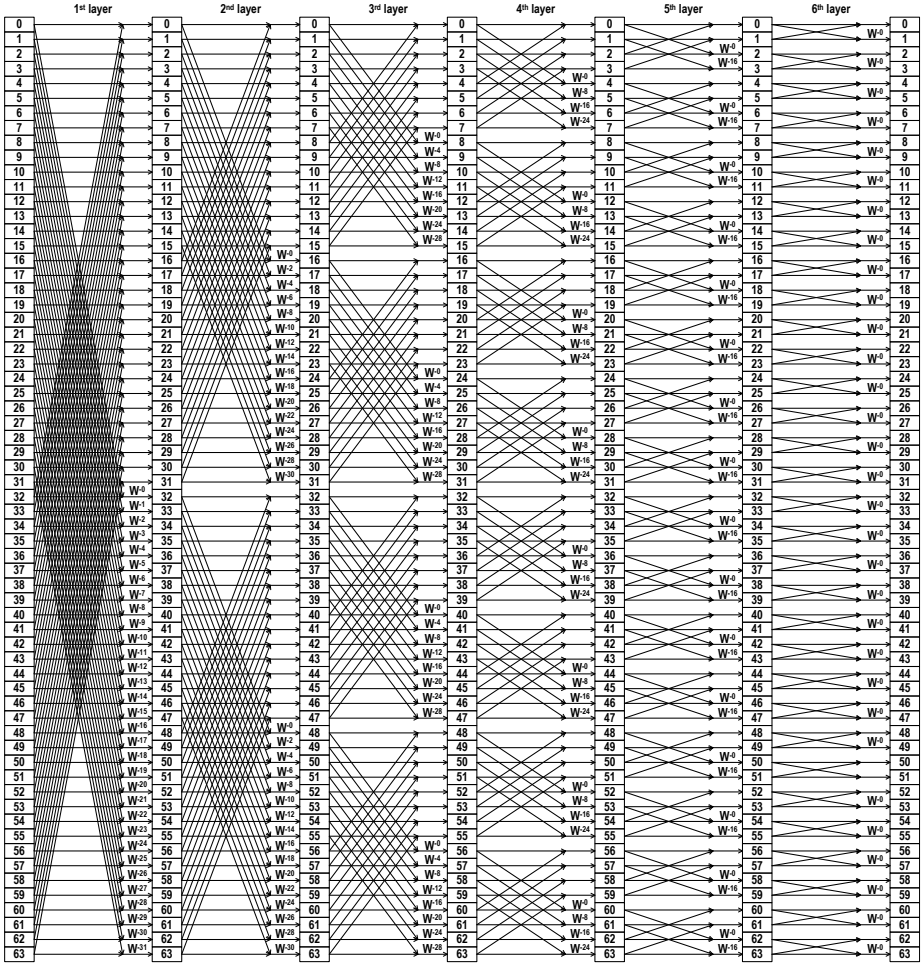
DIT FFT (N=8)



DIF FFT (N=8)

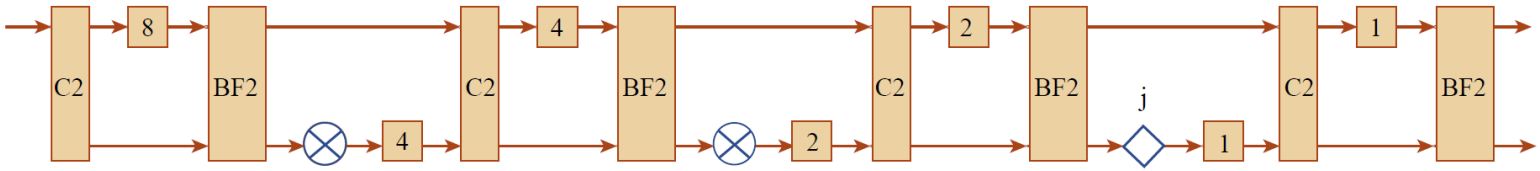
DIT radix-2 BF diagram for 64-IFFT

- In this lab, you need to design a circuit for 64-IFFT calculation based on DIT radix-2 butterfly (BF) diagram (see DIT_radix2_BF_64IFFT.pdf).

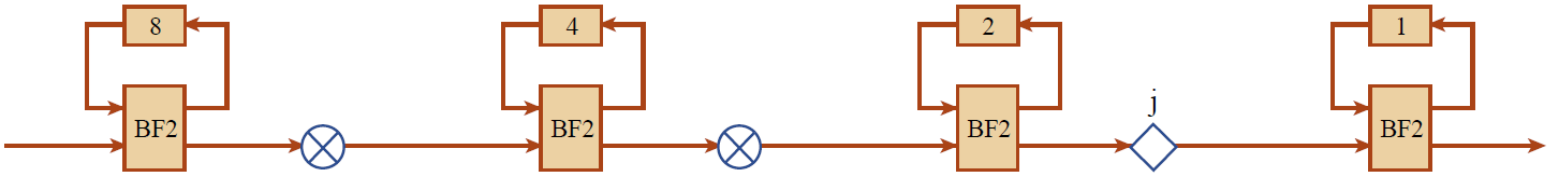


Pipelined (I)FFT architectures

- Taking Radix-2 32-(I)FFT as an example
  - multi-path delay commutator (R2MDC)
    - the most classical approach for pipeline implementation of radix-2 (I)FFT
    - Input sequence broken into two parallel data streams flowing forward with correct "distance" between data elements entering the butterfly scheduled by proper delays

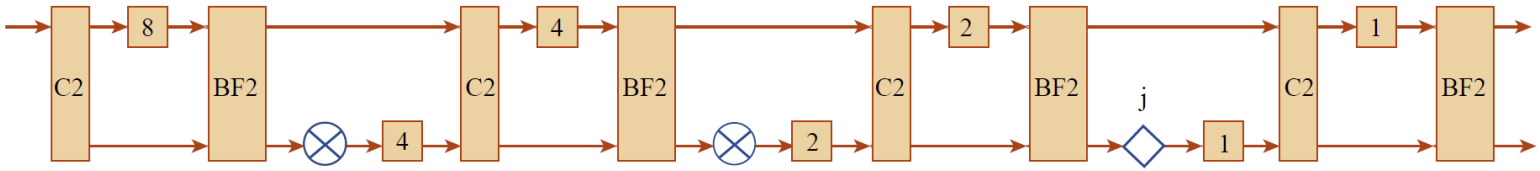


  - single-path delay feedback (R2SDF)

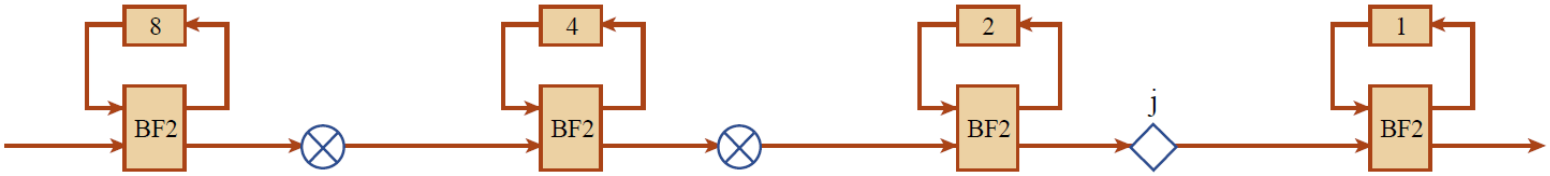


Pipelined (I)FFT architectures

- Taking Radix-2 32-(I)FFT as an example
  - **multi-path delay commutator (R2MDC) – for this lab**
    - the most classical approach for pipeline implementation of radix-2 (I)FFT
    - Input sequence broken into two parallel data streams flowing forward with correct "distance" between data elements entering the butterfly scheduled by proper delays

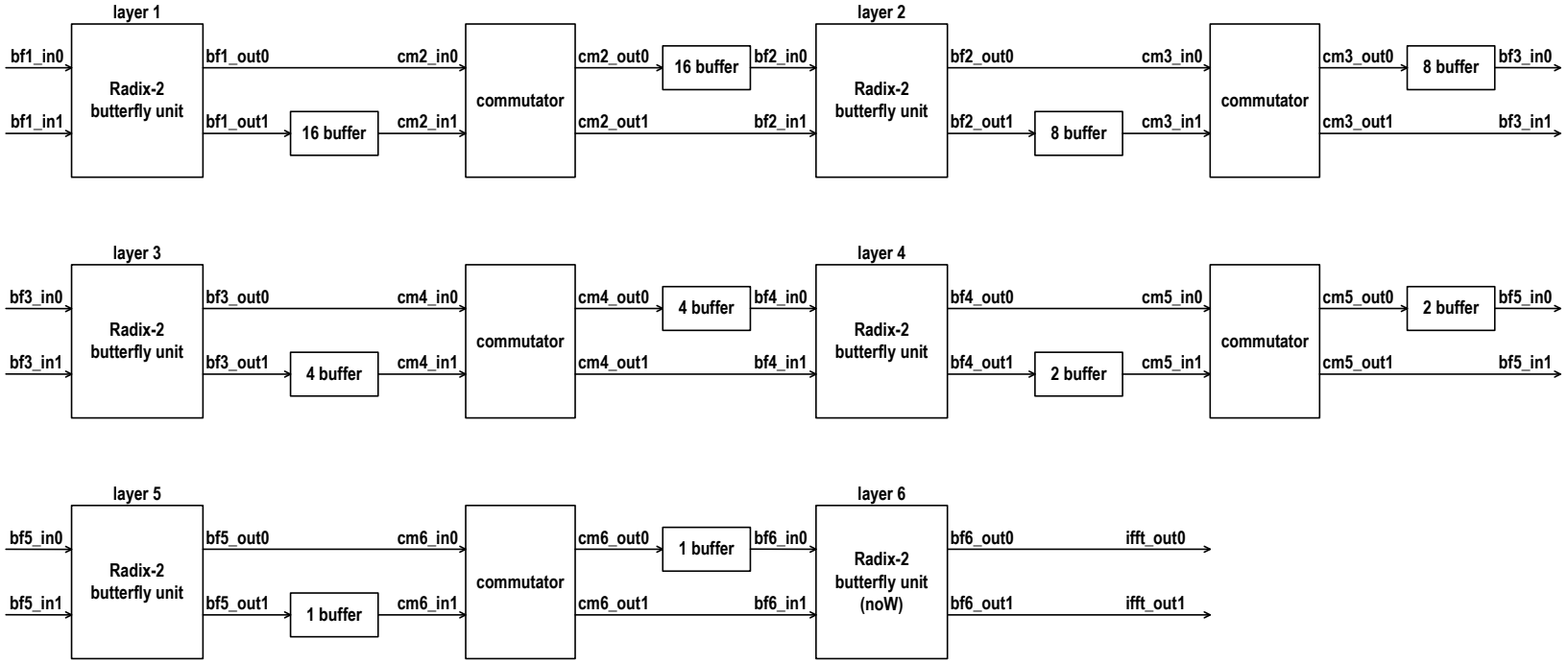


  - single-path delay feedback (R2SDF)



R2MDC pipeline architecture in 64-IFFT

- R2MDC pipeline architecture in 64-IFFT: 6 layers
  - buffers: to delay the data flow with certain cycles
  - radix-2 butterfly unit: to perform complex multiplication and accumulation
  - commutator: to re-order data between two paths



Dataflow in R2MDC pipeline for DIT 64-IFFT

- input of the 1st BF unit:

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32

pipeline

- output of the 1st BF unit:

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32

- delay the 2nd path by 16 cycles (input of the 1st commutator)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32

- output of the 1st commutator

47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

- delay the 1st path by 16 cycles (input of the 2nd BF unit)

47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

Dataflow in R2MDC pipeline for DIT 64-IFFT

- output of the 2nd BF unit:

47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

- delay the 2nd path by 8 cycles (input of the 2nd commutator)

								47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16								

- output of the 2nd commutator

								55	54	53	52	51	50	49	48	39	38	37	36	35	34	33	32	23	22	21	20	19	18	17	16	7	6	5	4	3	2	1	0
63	62	61	60	59	58	57	56	47	46	45	44	43	42	41	40	31	30	29	28	27	26	25	24	15	14	13	12	11	10	9	8								

- delay the 1st path by 8 cycles (input of the 3rd BF unit)

55	54	53	52	51	50	49	48	39	38	37	36	35	34	33	32	23	22	21	20	19	18	17	16	7	6	5	4	3	2	1	0
63	62	61	60	59	58	57	56	47	46	45	44	43	42	41	40	31	30	29	28	27	26	25	24	15	14	13	12	11	10	9	8

Dataflow in R2MDC pipeline for DIT 64-IFFT

- output of the 3rd BF unit:

55	54	53	52	51	50	49	48	39	38	37	36	35	34	33	32	23	22	21	20	19	18	17	16	7	6	5	4	3	2	1	0
63	62	61	60	59	58	57	56	47	46	45	44	43	42	41	40	31	30	29	28	27	26	25	24	15	14	13	12	11	10	9	8

- delay the 2nd path by 4 cycles (input of the 3rd commutator)

				55	54	53	52	51	50	49	48	39	38	37	36	35	34	33	32	23	22	21	20	19	18	17	16	7	6	5	4	3	2	1	0
63	62	61	60	59	58	57	56	47	46	45	44	43	42	41	40	31	30	29	28	27	26	25	24	15	14	13	12	11	10	9	8				

- output of the 3rd commutator

				59	58	57	56	51	50	49	48	43	42	41	40	35	34	33	32	27	26	25	24	19	18	17	16	11	10	9	8	3	2	1	0
63	62	61	60	55	54	53	52	47	46	45	44	39	38	37	36	31	30	29	28	23	22	21	20	15	14	13	12	7	6	5	4				

- delay the 1st path by 4 cycles (input of the 4th BF unit)

59	58	57	56	51	50	49	48	43	42	41	40	35	34	33	32	27	26	25	24	19	18	17	16	11	10	9	8	3	2	1	0
63	62	61	60	55	54	53	52	47	46	45	44	39	38	37	36	31	30	29	28	23	22	21	20	15	14	13	12	7	6	5	4

Dataflow in R2MDC pipeline for DIT 64-IFFT

- output of the 4th BF unit:

59	58	57	56	51	50	49	48	43	42	41	40	35	34	33	32	27	26	25	24	19	18	17	16	11	10	9	8	3	2	1	0
63	62	61	60	55	54	53	52	47	46	45	44	39	38	37	36	31	30	29	28	23	22	21	20	15	14	13	12	7	6	5	4

- delay the 2nd path by 2 cycles (input of the 4th commutator)

		59	58	57	56	51	50	49	48	43	42	41	40	35	34	33	32	27	26	25	24	19	18	17	16	11	10	9	8	3	2	1	0
63	62	61	60	55	54	53	52	47	46	45	44	39	38	37	36	31	30	29	28	23	22	21	20	15	14	13	12	7	6	5	4		

- output of the 4th commutator

		61	60	57	56	53	52	49	48	45	44	41	40	37	36	33	32	29	28	25	24	21	20	17	16	13	12	9	8	5	4	1	0
63	62	59	58	55	54	51	50	47	46	43	42	39	38	35	34	31	30	27	26	23	22	19	18	15	14	11	10	7	6	3	2		

- delay the 1st path by 2 cycles (input of the 5th BF unit)

61	60	57	56	53	52	49	48	45	44	41	40	37	36	33	32	29	28	25	24	21	20	17	16	13	12	9	8	5	4	1	0
63	62	59	58	55	54	51	50	47	46	43	42	39	38	35	34	31	30	27	26	23	22	19	18	15	14	11	10	7	6	3	2		

Dataflow in R2MDC pipeline for DIT 64-IFFT

- output of the 5th BF unit:

61	60	57	56	53	52	49	48	45	44	41	40	37	36	33	32	29	28	25	24	21	20	17	16	13	12	9	8	5	4	1	0
63	62	59	58	55	54	51	50	47	46	43	42	39	38	35	34	31	30	27	26	23	22	19	18	15	14	11	10	7	6	3	2

- delay the 2nd path by 1 cycles (input of the 5th commutator)

	61	60	57	56	53	52	49	48	45	44	41	40	37	36	33	32	29	28	25	24	21	20	17	16	13	12	9	8	5	4	1	0
63	62	59	58	55	54	51	50	47	46	43	42	39	38	35	34	31	30	27	26	23	22	19	18	15	14	11	10	7	6	3	2		

- output of the 5th commutator

	62	60	58	56	54	52	50	48	46	44	42	40	38	36	34	32	30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
63	61	59	57	55	53	51	49	47	45	43	41	39	37	35	33	31	29	27	25	23	21	19	17	15	13	11	9	7	5	3	1		

- delay the 1st path by 1 cycles (input of the 6th BF unit)

62	60	58	56	54	52	50	48	46	44	42	40	38	36	34	32	30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
63	61	59	57	55	53	51	49	47	45	43	41	39	37	35	33	31	29	27	25	23	21	19	17	15	13	11	9	7	5	3	1

- output of the 6th BF unit:

62	60	58	56	54	52	50	48	46	44	42	40	38	36	34	32	30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
63	61	59	57	55	53	51	49	47	45	43	41	39	37	35	33	31	29	27	25	23	21	19	17	15	13	11	9	7	5	3	1

Dataflow in R2MDC pipeline for DIT 64-IFFT

- Recall: time indices are in bit-reversed order at DIT BF diagram output
  - in this lab assignment, we can ignore the step of re-ordering outputs
  - reference outputs given in /ref are not re-ordered
- files in /ref: including 1000 test cases
  - test_twiddle_lut_re: real part of twiddle factors from W_{64}^{-0} to W_{64}^{-31}
  - test_twiddle_lut_im: imaginary part of twiddle factors from W_{64}^{-0} to W_{64}^{-31}
  - test_ifft_in0_re: real part of the inputs to the 1st path of the pipeline
  - test_ifft_in0_im: imaginary part of the inputs to the 1st path of the pipeline
  - test_ifft_in1_re: real part of the inputs to the 2nd path of the pipeline
  - test_ifft_in1_im: imaginary part of the inputs to the 2nd path of the pipeline
  - test_ifft_out0_reference_re: expected real part of the outputs from the 1st path
  - test_ifft_out0_reference_im: expected imaginary part of the outputs from the 1st path
  - test_ifft_out1_reference_re: expected real part of the outputs from the 2nd path
  - test_ifft_out1_reference_im: expected imaginary part of the outputs from the 2nd path

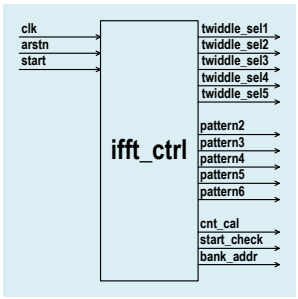
(files with _bin as suffix are read by testbench, files with _dec_nofrac as suffix are readable for debugging)

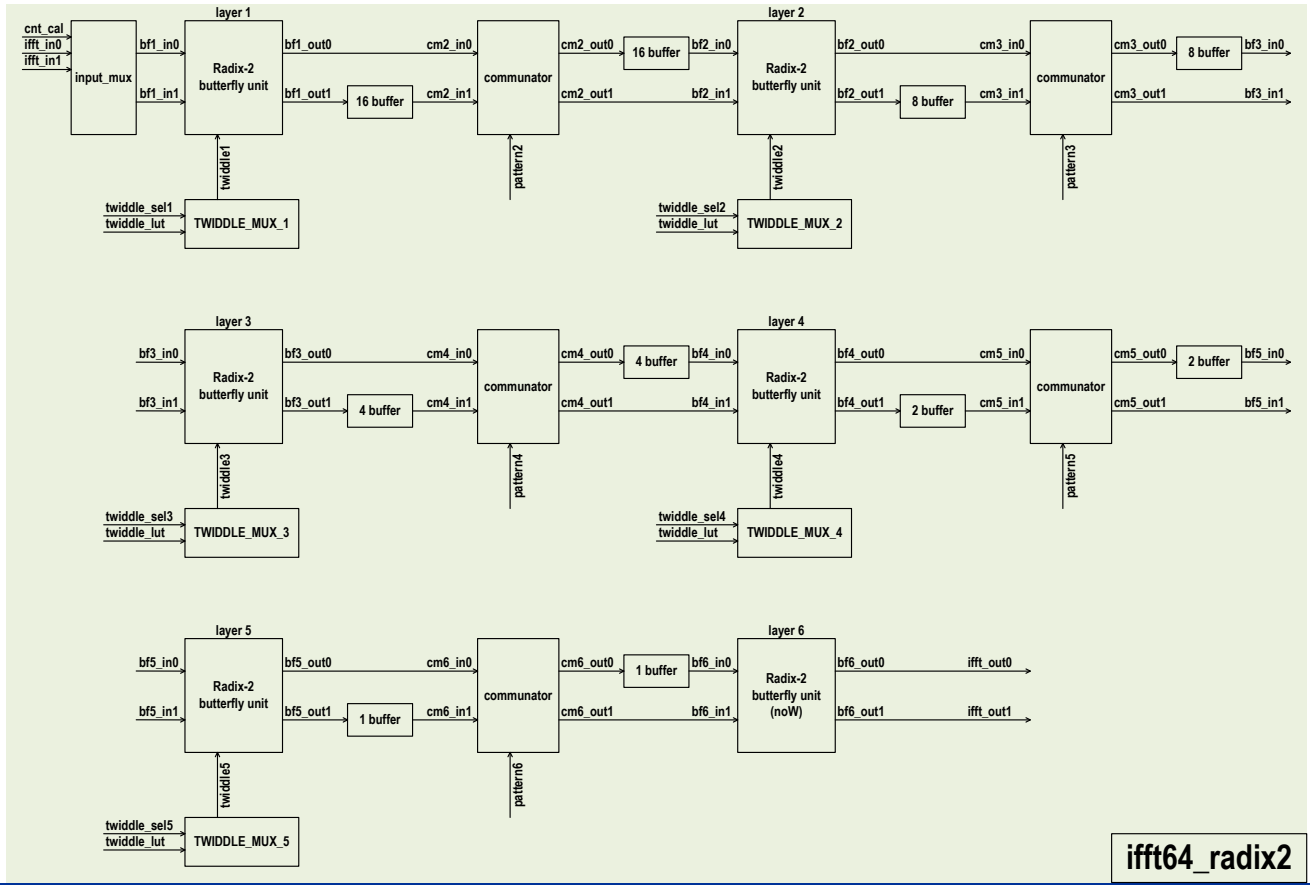
Complex adder and multiplier

- Numerical format in this lab assignment: signed fixed-point numbers
  - 16 bits for both real part and imaginary part
  - 1 bit (MSB) for sign: using 2's complement
  - 7 bits for integer part
  - 8 bits for fractional part
- Hints:
  - There is no need to differentiate integer part and fractional part when writing RTL codes, simply assuming all numbers are multiplied by 2^8
    - all data in files with _dec_nofract as suffix are decimal multiplied by 2^8 for easier reading and debugging.
    - however, you need to differentiate and be careful about integer and fractional bits when designing the multiplier for signed fixed-point numbers
  - Try to build a BF unit hierarchically (e.g., building a signed adder and a signed multiplier first, and then, build complex adder multiplier)

Architecture of the whole system

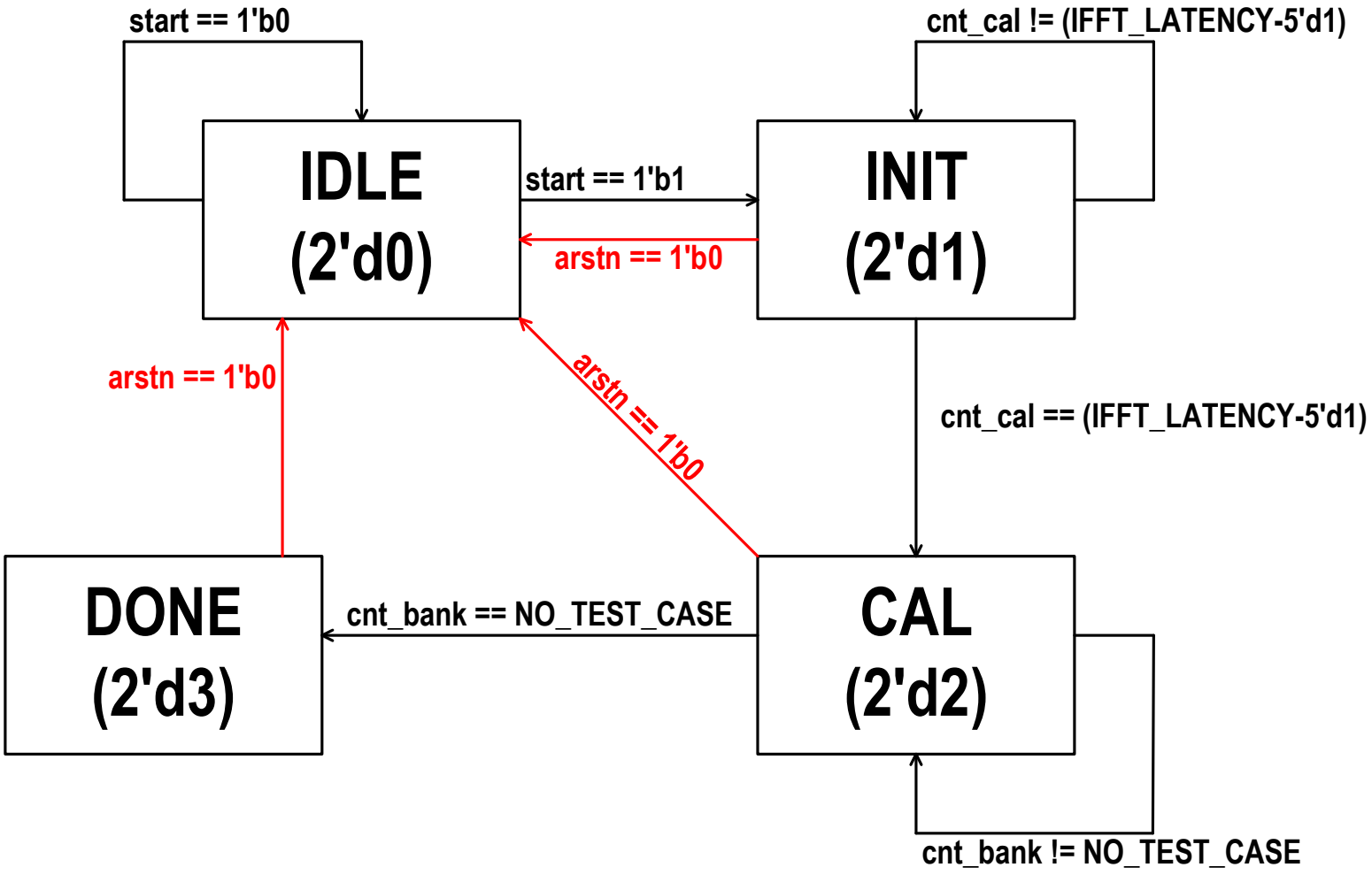
- ifft64_radix2_top
  - ifft64_ctrl: FSM + cnt_cal + cnt_bank
  - ifft64_ifft: 6 layers + input MUX + twiddle MUX





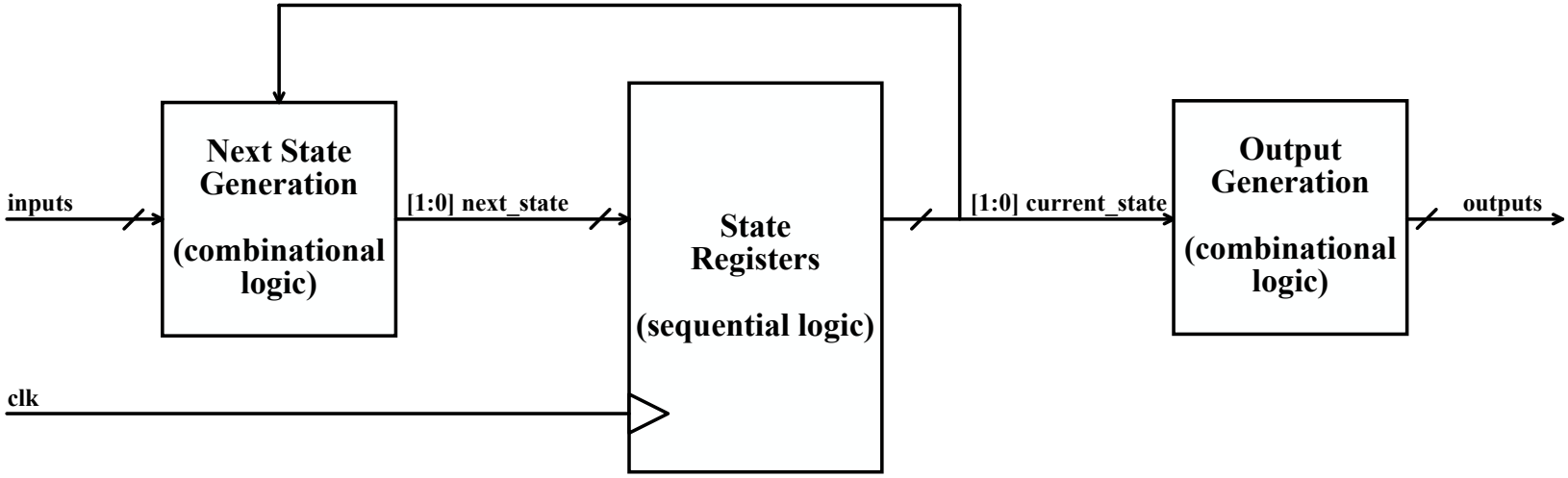
Controller design

- Finite State Machine (FSM):

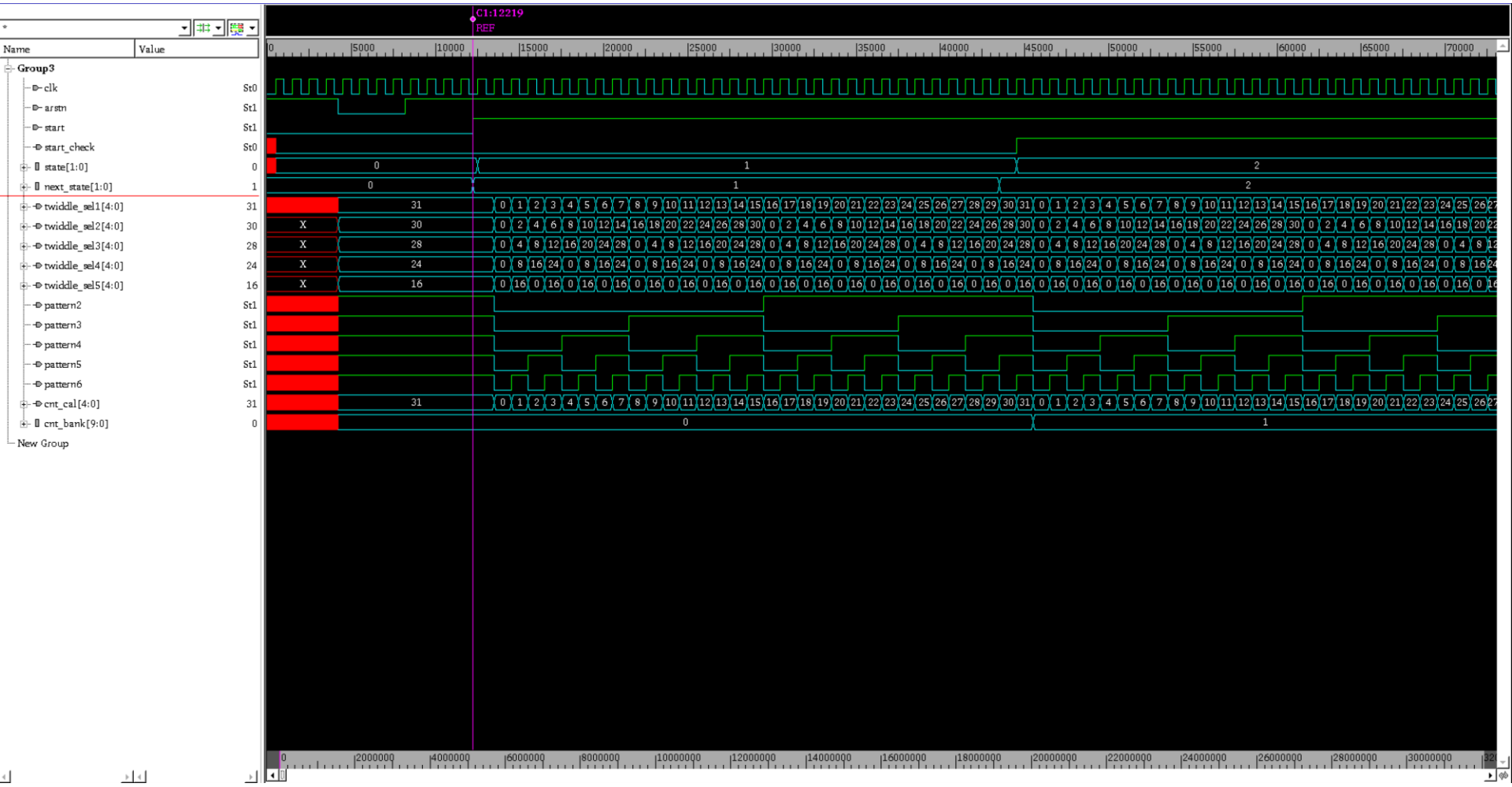


Controller design

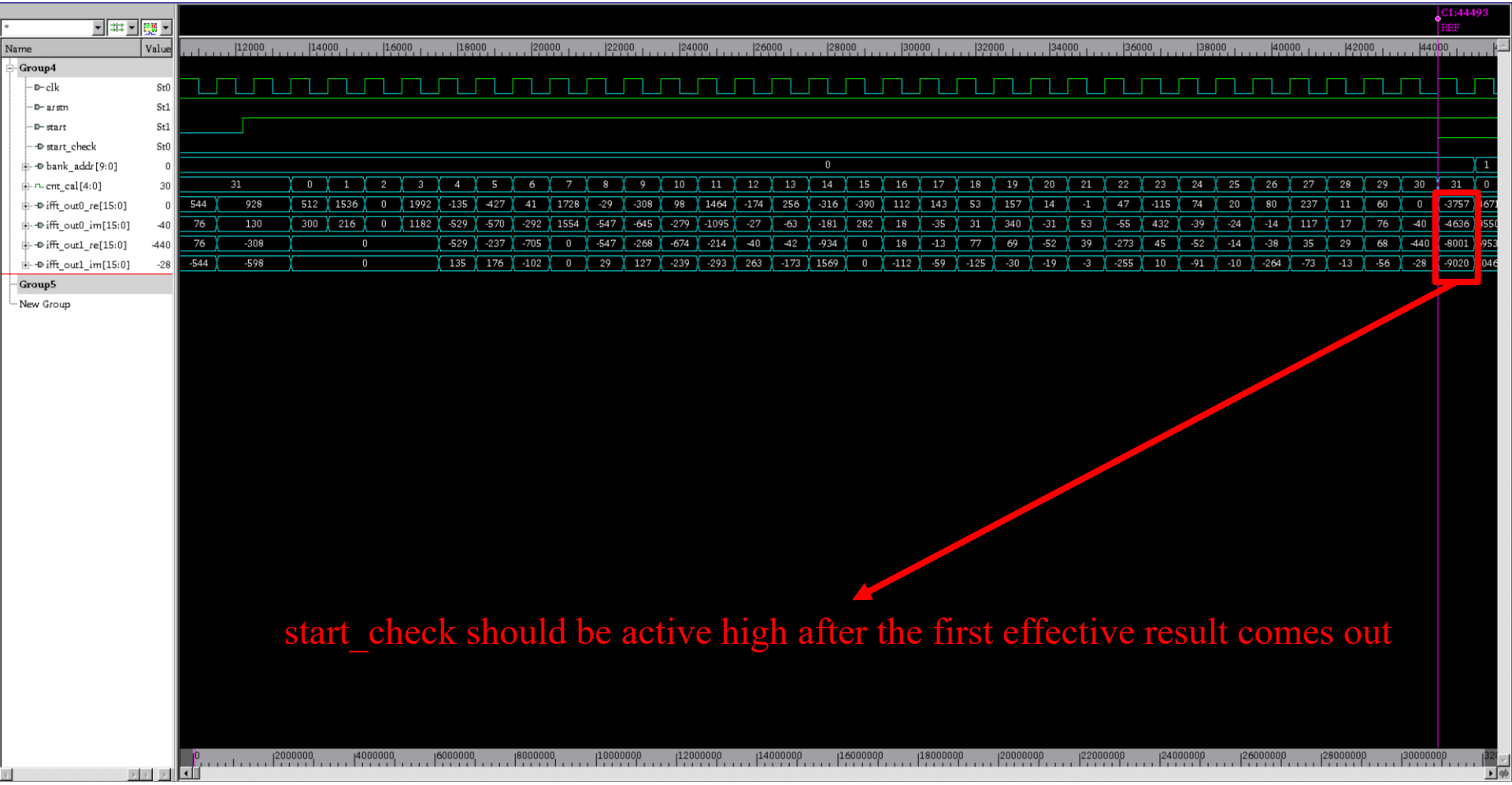
- Finite State Machine (FSM):



Example: waveform (control signals)



Example: waveform (IFFT64 output)



Example: timing&area report for ifft64_radix2_top.v

```
ifft64_radix2/BF_5/COM_MUL0/U16/Y (INVX1_RVT)           0.03       7.85 f
ifft64_radix2/BF_5/COM_MUL0/U34/Y (XOR2X1_RVT)          0.09       7.94 r
ifft64_radix2/BF_5/COM_MUL0/ADD0/B[7] (signed_fixed_point_add_6)
                                                        0.00       7.94 r
ifft64_radix2/BF_5/COM_MUL0/ADD0/add_10/B[7] (signed_fixed_point_add_6_DW01_add_0)
                                                        0.00       7.94 r
ifft64_radix2/BF_5/COM_MUL0/ADD0/add_10/U1_7/CO (FADDX1_RVT)
                                                        0.09       8.03 r
ifft64_radix2/BF_5/COM_MUL0/ADD0/add_10/U1_8/CO (FADDX1_RVT)
                                                        0.09       8.12 r
ifft64_radix2/BF_5/COM_MUL0/ADD0/add_10/U1_9/CO (FADDX1_RVT)
                                                        0.09       8.20 r
ifft64_radix2/BF_5/COM_MUL0/ADD0/add_10/U1_10/CO (FADDX1_RVT)
                                                        0.09       8.29 r
ifft64_radix2/BF_5/COM_MUL0/ADD0/add_10/U1_11/CO (FADDX1_RVT)
                                                        0.09       8.38 r
ifft64_radix2/BF_5/COM_MUL0/ADD0/add_10/U1_12/CO (FADDX1_RVT)
                                                        0.09       8.46 r
ifft64_radix2/BF_5/COM_MUL0/ADD0/add_10/U1_13/CO (FADDX1_RVT)
                                                        0.09       8.55 r
ifft64_radix2/BF_5/COM_MUL0/ADD0/add_10/U1_14/CO (FADDX1_RVT)
                                                        0.09       8.64 r
ifft64_radix2/BF_5/COM_MUL0/ADD0/add_10/U1_15/S (FADDX1_RVT)
                                                        0.11       8.75 f
ifft64_radix2/BF_5/COM_MUL0/ADD0/add_10/SUM[15] (signed_fixed_point_add_6_DW01_add_0)
                                                        0.00       8.75 f
ifft64_radix2/BF_5/COM_MUL0/ADD0/Y[15] (signed_fixed_point_add_6)
                                                        0.00       8.75 f
ifft64_radix2/BF_5/COM_MUL0/Y_re[15] (complex_mul_1)
                                                        0.00       8.75 f
ifft64_radix2/BF_5/Y1_re[15] (bf_radix2_1)              0.00       8.75 f
ifft64_radix2/BUFF_6_be_re/buf_in[15] (Nbuffer_buffer_depth1_buffer_width1_0)
                                                        0.00       8.75 f
ifft64_radix2/BUFF_6_be_re/generate_block_2_0__STAGE0/stage_in[15] (one_reg_stage_4)
                                                        0.00       8.75 f
ifft64_radix2/BUFF_6_be_re/generate_block_2_0__STAGE0/generate_block_1_15__REG_0/reg_in (one_reg_49)
                                                        0.00       8.75 f
ifft64_radix2/BUFF_6_be_re/generate_block_2_0__STAGE0/generate_block_1_15__REG_0/reg_out_reg/D (DFFARX1_RVT)
                                                        0.11       8.85 f
data arrival time                                                  8.85

clock clk (rise edge)                                  10.00      10.00
clock network delay (ideal)                             0.00      10.00
clock uncertainty                                      -0.10       9.90
ifft64_radix2/BUFF_6_be_re/generate_block_2_0__STAGE0/generate_block_1_15__REG_0/reg_out_reg/CLK (DFFARX1_RVT)
                                                        0.00       9.90 r
library setup time                                     -0.02       9.88
data required time                                                 9.88
---------------------------------------------------------------------------
data required time                                                 9.88
data arrival time                                                 -8.85
---------------------------------------------------------------------------
slack (MET)                                                        1.02
```

```
****************************************
Report : area
Design : ifft64_radix2_top
Version: J-2014.09-SP2
Date   : Mon Mar  4 22:42:04 2024
****************************************

Library(s) Used:

    saed32rvt_tt1p05v125c (File: /app11/saed_32

Number of ports:                         3150
Number of nets:                          3185
Number of cells:                            2
Number of combinational cells:              0
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                       2

Combinational area:              61436.770226
Buf/Inv area:                     3755.994263
Noncombinational area:           14239.180279
Macro/Black Box area:                0.000000
Net Interconnect area:           17952.303348

Total cell area:                 75675.950505
Total area:                      93628.253853
```

Example: timing&area report for ifft64_radix2_top.v

- Timing/Area trade-off curve with the same design

```
clock clk (rise edge)                                   10.00      10.00
clock network delay (ideal)                              0.00      10.00
clock uncertainty                                       -0.10       9.90
ifft64_radix2/BUFF_6_be_re/generate_block_2_0__STAGE0/generate_block_1_15_
                                                         0.00       9.90 r
library setup time                                      -0.02       9.88
data required time                                                  9.88
--------------------------------------------------------------------------
data required time                                                  9.88
data arrival time                                                  -8.85
--------------------------------------------------------------------------
slack (MET)                                                         1.02
```

```
clock clk (rise edge)                                    9.00       9.00
clock network delay (ideal)                              0.00       9.00
clock uncertainty                                       -0.10       8.90
ifft64_radix2/BUFF_6_be_im/generate_block_2_0__STAGE0/generate_block_1_15_
                                                         0.00       8.90 r
library setup time                                      -0.02       8.88
data required time                                                  8.88
--------------------------------------------------------------------------
data required time                                                  8.88
data arrival time                                                  -8.72
--------------------------------------------------------------------------
slack (MET)                                                         0.16
```

```
****************************************
Report : area
Design : ifft64_radix2_top
Version: J-2014.09-SP2
Date   : Mon Mar  4 22:42:04 2024
****************************************

Library(s) Used:

    saed32rvt_tt1p05v125c (File: /app11/saed_32

Number of ports:                         3150
Number of nets:                          3185
Number of cells:                            2
Number of combinational cells:              0
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                       2

Combinational area:              61436.770226
Buf/Inv area:                     3755.994263
Noncombinational area:           14239.180279
Macro/Black Box area:                0.000000
Net Interconnect area:           17952.303348

Total cell area:                 75675.950505
Total area:                      93628.253853
```

```
****************************************
Report : area
Design : ifft64_radix2_top
Version: J-2014.09-SP2
Date   : Mon Mar  4 22:55:42 2024
****************************************

Library(s) Used:

    saed32rvt_tt1p05v125c (File: /app11/saed_32

Number of ports:                         3150
Number of nets:                          3185
Number of cells:                            2
Number of combinational cells:              0
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                       2

Combinational area:              61437.532652
Buf/Inv area:                     3761.585426
Noncombinational area:           14239.180279
Macro/Black Box area:                0.000000
Net Interconnect area:           18032.734120

Total cell area:                 75676.712931
Total area:                      93709.447051
```

Example: timing&area report for ifft64_radix2_top.v

- before and after timing optimization (retiming, pipeline, etc.)

```
clock clk (rise edge)                                    10.00      10.00
clock network delay (ideal)                               0.00      10.00
clock uncertainty                                        -0.10       9.90
ifft64_radix2/BUFF_6_be_re/generate_block_2_0__STAGE0/generate_block_1_15_
                                                          0.00       9.90 r
library setup time                                       -0.02       9.88
data required time                                                   9.88
-----------------------------------------------------------------------
data required time                                                   9.88
data arrival time                                                   -8.85
-----------------------------------------------------------------------
slack (MET)                                                         1.02
```

```
clock clk (rise edge)                                    10.00      10.00
clock network delay (ideal)                               0.00      10.00
clock uncertainty                                        -0.10       9.90
ifft64_radix2/COMMUTATOR_6/clk_r_REG25_S17/CLK (DFFARX1_RVT)
                                                          0.00       9.90 r
library setup time                                       -0.03       9.87
data required time                                                   9.87
-----------------------------------------------------------------------
data required time                                                   9.87
data arrival time                                                   -7.20
-----------------------------------------------------------------------
slack (MET)                                                         2.66
```

```
****************************************
Report : area
Design : ifft64_radix2_top
Version: J-2014.09-SP2
Date   : Mon Mar  4 22:42:04 2024
****************************************

Library(s) Used:

    saed32rvt_tt1p05v125c (File: /app11/saed_32

Number of ports:                         3150
Number of nets:                          3185
Number of cells:                            2
Number of combinational cells:              0
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                       2

Combinational area:              61436.770226
Buf/Inv area:                     3755.994263
Noncombinational area:           14239.180279
Macro/Black Box area:                0.000000
Net Interconnect area:           17952.303348

Total cell area:                 75675.950505
Total area:                      93628.253853
```

```
****************************************
Report : area
Design : ifft64_radix2_top
Version: J-2014.09-SP2
Date   : Mon Mar  4 23:08:59 2024
****************************************

Library(s) Used:

    saed32rvt_tt1p05v125c (File: /app11/saed_32

Number of ports:                         3150
Number of nets:                          3186
Number of cells:                           13
Number of combinational cells:              0
Number of sequential cells:                11
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                       3

Combinational area:              56243.845911
Buf/Inv area:                     2875.385276
Noncombinational area:           19499.961172
Macro/Black Box area:                0.000000
Net Interconnect area:           23163.489646

Total cell area:                 75743.807082
Total area:                      98907.296728
```

Synthesis Constraints

To be saved as constraint.tcl in your /syn folder

- Clock period of 10 ns.
- Clock uncertainty of 0.1 ns
- Input transition of (exclude clock) of 0.1 ns
- Input delay (exclude clock and reset) of 0.2 ns
- Output delay (all outputs) of 0.2 ns
- Load capacitance (all outputs) of 5 fF
- Driving gates: inverter gates with 4X strength
- Max area (no constraints): 0

To be completed in report

Step 1: RTL implementation (10%)

- Submit your RTL code for all the blocks (start with the given .v files).
- Describe this script (/vcs/makefile).
  - What are going to be performed by typing “make compile” and “make clean”?
- Pass all the 1000 test cases through VCS simulation.
- Show the waveforms in DVE.

Step 2: Synthesis (5%)

- Please complete the constraint.tcl file
- Describe these scripts (/syn/makefile, /syn/dc-syn.tcl)
  - What are going to be performed by typing “make synthesis”, “make plot”, and “make clean”?
- Synthesize your ifft64_radix2_top module
  - Show the timing and area reports. Check is there any violation? Point out which part of circuits cause the critical path.
- In real design cases, you are going to use the synthesized files for next step (the .ddc, .sdc, sdf, .v files in the /syn/output folder). Compare the synthesized netlist (.v file) with your Verilog code and show your comments.

To be completed in report

Part 3: Timing and area optimization (8%)

- Make changes to your constraint files and plot the timing/area trade-off curve.
- Apply any design optimization method that you learnt from the lecture (retiming, pipeline, etc.)
  - For retiming, you may either do it manually or insert below command into your .tcl script in /**syn/dc-syn.tcl**. Design compiler will re-allocate the registers automatically with this command "optimize_registers -print_critical_loop -minimum_period_only".
  - Will the whole system still work properly after register insertion, retiming, etc… and why?
  - Show your comments on the comparison between original design and your optimized design (in circuit, area, timing, etc.).

Part 4: Improvement (open ended) (2%)

- Can you further improve the whole design?
  - Explain your ideas and the corresponding design trade-offs
  - Please also show your timing and area reports after making any change.
  - e.g. remove the unnecessary registers, reduce the I/O bitwidth, …

Quick start

Part 0: startup

- Make a new directory for your project
- Go to the new directory
- Copy the lab materials (/app11/lab_session/ee4415_part2_2324) into your new directory
- Make sure you have below folders: ref, syn, tb, src, vcs

Part 1: RTL implementation

- Implement your design in the /src folder or testbench in the /tb folder
- Check the contents in /vcs/makefile
- Run VCS simulation: type “make compile” in /vcs folder, you may have to modify the makefile script if you wish to run your own testbench.
- Check waveform: type “make plot” in /vcs folder
- Clean the simulation results: type “make clean” in /vcs folder

Part 2: Synthesis

- Complete your constraint.tcl
- Check the contents in /syn/dc-syn.tcl, /syn/makefile
- Synthesize your design: type “make synthesis” in /syn folder
- Clean the synthesis results: type “make clean” in /syn folder

Part 3: Timing and area optimization

- Backup your scripts
- Similar to part 2, but you may need to modify /syn/constraint.tcl and /syn/dc-syn.tcl

Part 4: Improvement (open ended)

- Similar to part 2 and part 3.

Helpsheet

Useful Linux commands

Create new folder	mkdir folder_name
Go to a directory	cd target_path
Go to the upper directory	cd ..
Remove something (be careful)	rm target_path –r
Move something	mv source_path target_path
Copy something	cp source_path target_path –a
Open a .v file with vim	vim filename
Open a .v file with GUI	gedit filename
Open a .pdf file	evince filename
Show current path	pwd
Show all the files in current path	ls –a

Simulation with VCS

Compile design	vcs -full64 +lint=all -debug_all -timescale=1ns/10ps filenames
Run simulation	./simv
Exit	quit

Show waveform in DVE

Save .vpd	Insert below lines into your testbench's initial block: $vcdplusfile("waveform.vpd"); $vcdpluson(); // your code $vcdplusoff();
Show waveform	dve -vpd waveform.vpd &