

RM68042 Data Sheet

Single Chip Driver with 262K color

for 320RGBx480 a-Si TFT LCD

Revision : 0.6
Date : Apr. 16, 2010

Revision History

Version No.	Date	Page	Description
V06.0	2010/04/16		Draft

CONFIDENTIAL

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1. General Description

RM68041 is a 262,144-color single-chip SoC driver for a-TFT liquid crystal display with resolution of 320RGBx480 dots, comprising a 960-channel source driver, a 480-channel gate driver, 345,600 bytes GRAM for graphic data of 320RGBx480 dots, and power supply circuit.

The RM68041 supports 18-/16-/9-/8-bit data bus interface (DBI) and serial peripheral interfaces (SPI). It also supplies 18-bit or 16-bit RGB interface (DPI) for driving video signal directly from application controller. The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

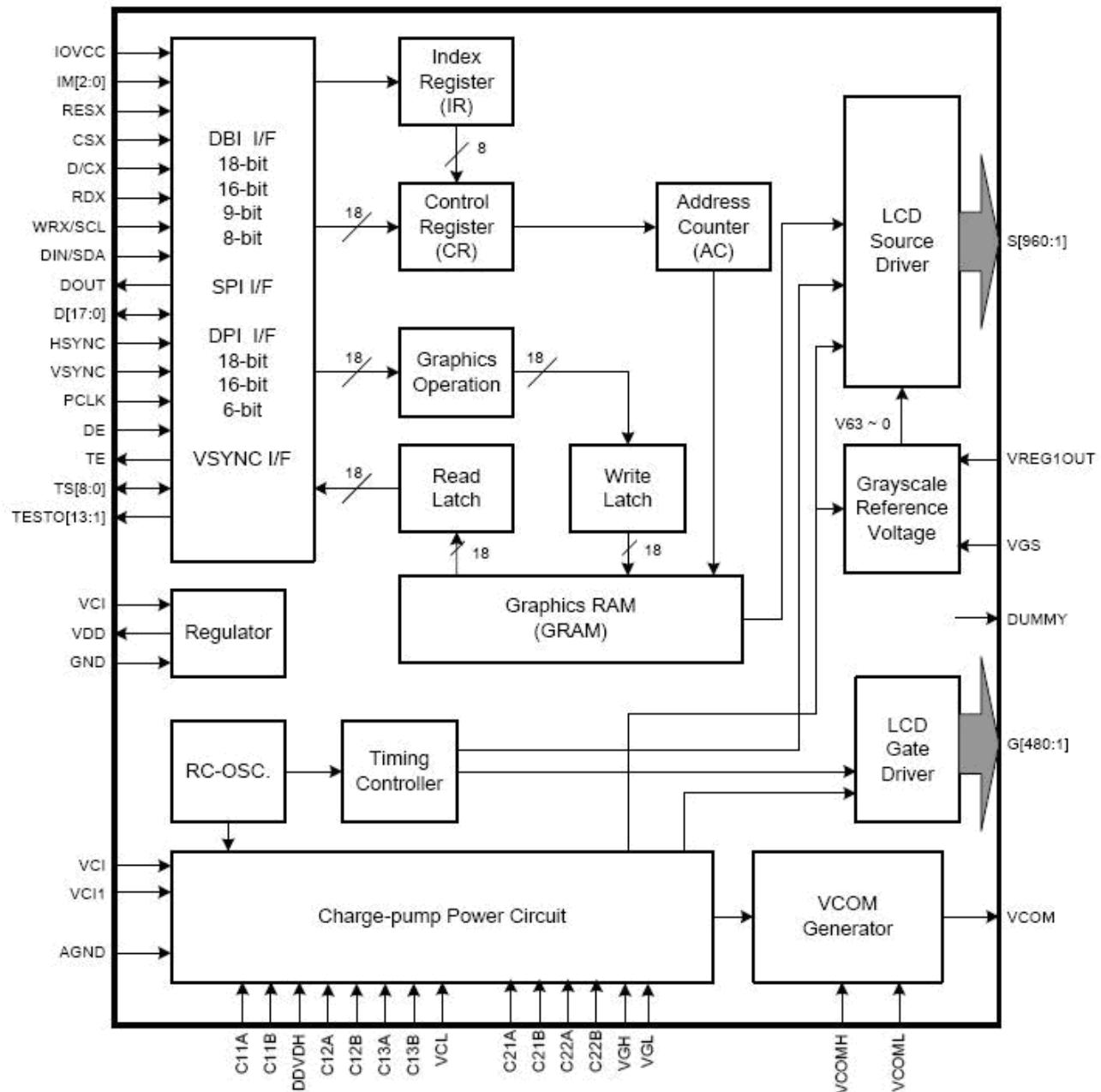
RM68041 can operate with 1.65V I/O interface voltage, and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The RM68041 also supports a function to display in 8 colors and a sleep mode, allowing for precise power control by software and these features make the RM68041 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- Display resolution: [320xRGB](H) x 480(V)
- Output:
 - 960 source outputs
 - 480 gate outputs
 - Common electrode output
- a-TFT LCD driver with on-chip full display RAM: 345,600 bytes
- MCU Interface
 - MIPI-DBI(Comply with MIPI DBI Version 2.00)
 - Type B 16-/18- bit, 8-/9-bit
 - Type C 4-line 9bit (Option 1), 8bit (Option 3)
 - 16-bits, 18-bits RGB (DPI) interface
 - MIPI DCS command sets
 - 3-pin/4-pin serial interface
- Display mode:
 - Full color mode: 262K-colors
 - Reduced color mode: 8-colors (3-bits MSB bits mode)
- On chip functions:
 - VCOM generator and adjustment

- Timing generator
- Oscillator
- DC/DC converter
- Line/frame inversion
- MTP:
 - 16-bit ID1 and ID2
 - 7-bits for VCOM adjustment
- Low -power consumption architecture
 - Low operating power supplies:
 - $\text{IOVcc} = 1.65\text{V} \sim 3.3\text{V}$ (interface I/O)
 - $\text{Vci} = 2.5\text{V} \sim 3.3\text{V}$ (analog)
- LCD Voltage drive:
 - Source/VCOM power supply voltage
 - $\text{DDVDH} - \text{GND} = 4.5\text{V} \sim 6.0\text{V}$
 - $\text{VCL} - \text{GND} = -1.0\text{V} \sim -3.0\text{V}$
 - $\text{VCI} - \text{VCL} \leq 6.0\text{V}$
 - Gate driver output voltage
 - $\text{VGH} - \text{GND} = 10\text{V} \sim 18\text{V}$
 - $\text{VGL} - \text{GND} = -5\text{V} \sim -12.5\text{V}$
 - $\text{VGH} - \text{VGL} \leq 32\text{V}$
 - VCOM driver output voltage
 - $\text{VCOMH} = 3.0\text{V} \sim (\text{DDVDH}-0.5)\text{V}$
 - $\text{VCOML} = (\text{VCL}+0.5)\text{V} \sim 0\text{V}$
 - $\text{VCOMH-VCOML} \leq 6.0\text{V}$
- Operate temperature range: -40°C to 85°C

3. Block Diagram



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4. Pin Description

Pin Name	I/O	Descriptions																																																						
IM[2:0]	I	Select the MPU system interface mode <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>IM2</th><th>IM1</th><th>IM0</th><th>MPU-Interface Mode</th><th>DB Pin in use</th><th>Colors</th></tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>DBI Type B 18-bit</td><td>DB[17:0]</td><td>262K</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>DBI Type B 9-bit</td><td>DB[8:0]</td><td>262K</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>DBI Type B 16-bit</td><td>DB[15:0]</td><td>65K/262K</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>DBI Type B 8-bit</td><td>DB[7:0]</td><td>65K/262K</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>Setting prohibited</td><td>-</td><td>-</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>DBI Type C 9-bit</td><td>DIN, DOUT</td><td>8/262K</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>Setting prohibited</td><td>-</td><td>-</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>DBI Type C 8-bit</td><td>DIN, DOUT</td><td>8/262K</td></tr> </tbody> </table>	IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use	Colors	0	0	0	DBI Type B 18-bit	DB[17:0]	262K	0	0	1	DBI Type B 9-bit	DB[8:0]	262K	0	1	0	DBI Type B 16-bit	DB[15:0]	65K/262K	0	1	1	DBI Type B 8-bit	DB[7:0]	65K/262K	1	0	0	Setting prohibited	-	-	1	0	1	DBI Type C 9-bit	DIN, DOUT	8/262K	1	1	0	Setting prohibited	-	-	1	1	1	DBI Type C 8-bit	DIN, DOUT	8/262K
IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use	Colors																																																			
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0	1	1	DBI Type B 8-bit	DB[7:0]	65K/262K																																																			
1	0	0	Setting prohibited	-	-																																																			
1	0	1	DBI Type C 9-bit	DIN, DOUT	8/262K																																																			
1	1	0	Setting prohibited	-	-																																																			
1	1	1	DBI Type C 8-bit	DIN, DOUT	8/262K																																																			
RESX	I	This signal low will reset the device and must be applied to properly initialize the chip. Signal is low active.																																																						
CSX	I	Chip select input pin ("Low" enable).																																																						
D/CX	I	Display data / Command selection pin D/CX='1': Display data. D/CX='0': Command data. If not used, please fix this pin at GND level.																																																						
RDX	I	Read control pin for the DBI interface. If not used, please connect this pin to IOVCC.																																																						
WRX/SCL	I	Write control pin for the DBI interface. When the DBI type C is selected, this pin is used as serial clock pin. If not used, please connect this pin to IOVCC.																																																						
DB[17:0]	I/O	These pins are data bus. If not used, please connect these pins to GND.																																																						
DIN/SDA	I/O	Serial data input pin and used for the DBI type C mode. If not used, please connect this pin to ground.																																																						
DOUT	O	Serial data output pin and used for the DBI type C mode.																																																						
TE	O	Tearing effect output pin to synchronizes MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, please open this pin.																																																						
PCLK	I	Pixel clock signal in DPI interface mode. If not used, please fix this pin at GND level.																																																						

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VSYNC	I	Vertical sync. signal in DPI interface mode. If not used, please fix this pin at GND level.						
Hsync	I	Horizontal sync. signal in DPI interface mode. If not used, please fix this pin at GND level.						
DE	I	Data enable signal in DPI interface mode. If not used, please fix this pin at GND level.						
SD	I	Control pin to shut down display, only used in the DPI interface mode. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr><th>SD</th><th>Shut Down Control</th></tr> <tr><td>0</td><td>Normal Display</td></tr> <tr><td>1</td><td>Display shut down</td></tr> </table>	SD	Shut Down Control	0	Normal Display	1	Display shut down
SD	Shut Down Control							
0	Normal Display							
1	Display shut down							
CM	I	Control pin for switching between normal color and reduced color mode, only used in the DPI interface mode. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr><th>CM</th><th>Color Mode</th></tr> <tr><td>0</td><td>Normal Display Color</td></tr> <tr><td>1</td><td>Reduced Color Mode (8-color)</td></tr> </table>	CM	Color Mode	0	Normal Display Color	1	Reduced Color Mode (8-color)
CM	Color Mode							
0	Normal Display Color							
1	Reduced Color Mode (8-color)							

Power Input Pins

IOVCC	P	Power supply to interface pins Connect to external power supply (IOVCC= 1.65~3.3V).
VCI	P	Power supply to liquid crystal power supply analog circuit. Connect to external power supply (VCI=2.5~3.3V).
DGND AGND	P	Power ground pin. Make sure GND=0V.
VPG	P	Power supply pin for the NV memory programming. Please provide 6 volt to this pin for NV memory programming.

LCD signals Pins

S1 ~ S960	O	Source driver output pins.
G1 ~ G480	O	Gate driver output pins.
VDD	O	Internal logic regulator output. Used as internal logic power supply. Connect to stabilizing capacitor.
VCI1	P	Reference voltage for the step-up circuit 1. Set VCI1 level so that DDVDH, VGH and VGL are within the ratings.

DDVDH	P	Power supply for the source driver and VCOM.
VGH	P	Power supply to drive liquid crystal.
VGL	P	Power supply for LCD drive.
VCL	P	Power supply to drive VCOML.
C11A, C11B, C12A, C12B	P	Make sure to connect to capacitor that is used in internal step-up circuit 1.
C13A, C13B, C21A, C21B, C22A, C22B,	P	Make sure to connect to capacitor that is used in internal step-up circuit 2. Connect to capacitors according to the step-up factors in use.
VREG1OUT	P	Outputs voltage level generated from VRH VCILVL. The step-up factor applied to VRH VCILVL is set by VRH bits. $VREG1OUT=4.0 \sim (DDVDH-0.500)[V]$
VCOM	P	TFT display common electrode power supply. Alternates between voltage levels between VCOMH-VCOML. Registers set the alternating cycle.
VCOMH	P	VCOM high level. Adjust the voltage by internal electronic volume (VCM)
VCOML	P	VCOM low level. Adjust the voltage by VDV bits. $VCOML=(VCL+0.5) \sim 0[V]$
VGS	I	Reference level for grayscale generating circuit.
TEST pins		
TS[8:0]	I	Test pins These pins are internal pulled low. Please leave these pins as open.
TESTO[16:1]	O	Test pins Please leave these pins as open.
TESTA1-A3	I/O	Test pins Please leave these pins as open.
DUMMY	-	Dummy Pins These pins are floating.

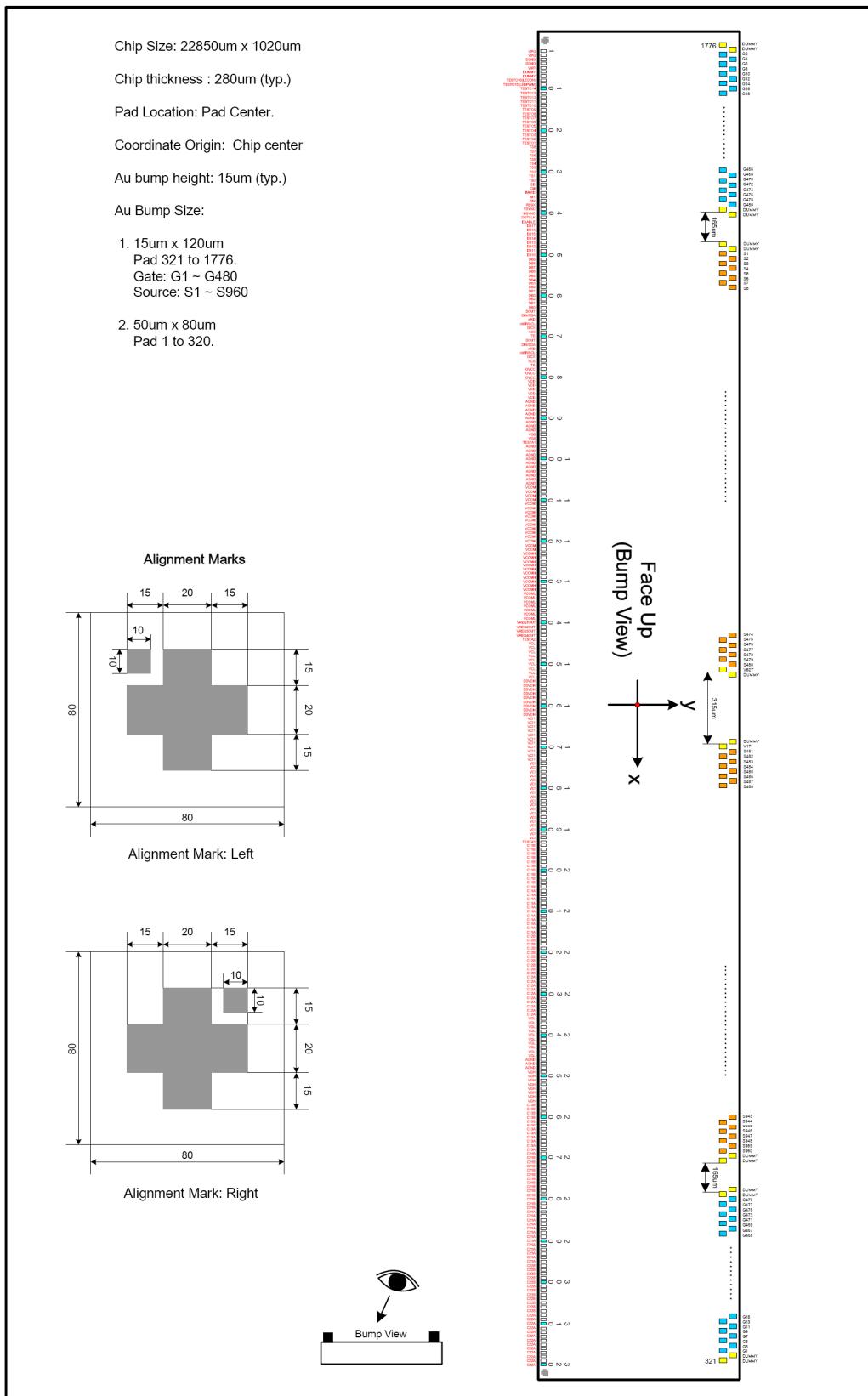
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V1T V62T VWT	I	Test pins Please leave these pins as open.
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Liquid crystal power supply specifications Table

No.	Item	Description
1	TFT Source Driver	960 pins (320 x RGB)
2	TFT Gate Driver	480 pins
3	TFT Display's Capacitor Structure	Cst structure only (Common VCOM)
4	Liquid Crystal Drive Output	S1 ~ S960 V0 ~ V63 grayscales
		G1 ~ G480 VGH - VGL
		VCOM VCOMH - VCOML: Amplitude = electronic volumes
5	Input Voltage	IOVcc 1.65 ~ 3.30V
		Vci 2.50 ~ 3.30V
6	Liquid Crystal Drive Voltages	DDVDH 4.5V ~ 6.0V
		VGH 10V ~ 18V
		VGL -5V ~ -12.5V
		VCL -1.0V ~ -3.0V
		VGH - VGL Max. 32V
		Vci - VCL Max. 6.0V
7	Internal Step-up Circuits	DDVDH Vci1 x2
		VGH Vci1 x4, x5, x6
		VGL Vci1 x-3, x-4, x-5
		VCL Vci1 x-1

5. Pad Arrangement and Coordination



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No	Name	X	Y
1	VPG	-11165	-409
2	VPG	-11095	-409
3	DGND	-11025	-409
4	DGND	-10955	-409
5	VWT	-10885	-409
6	DUMMY	-10815	-409
7	DUMMY	-10745	-409
8	TESTO16	-10675	-409
9	TESTO15	-10605	-409
10	TESTO14	-10535	-409
11	TESTO13	-10465	-409
12	TESTO12	-10395	-409
13	TESTO11	-10325	-409
14	TESTO10	-10255	-409
15	TESTO9	-10185	-409
16	TESTO8	-10115	-409
17	TESTO7	-10045	-409
18	TESTO6	-9975	-409
19	TESTO5	-9905	-409
20	TESTO4	-9835	-409
21	TESTO3	-9765	-409
22	TESTO2	-9695	-409
23	TESTO1	-9625	-409
24	TS8	-9555	-409
25	TS7	-9485	-409
26	TS6	-9415	-409
27	TS5	-9345	-409
28	TS4	-9275	-409
29	TS3	-9205	-409
30	TS2	-9135	-409
31	TS1	-9065	-409
32	TS0	-8995	-409
33	SHUT	-8925	-409
34	CM	-8855	-409
35	IM0/ID	-8785	-409
36	IM1	-8715	-409
37	IM2	-8645	-409
38	RESX	-8575	-409
39	VSYNC	-8505	-409
40	HSYNC	-8435	-409
41	DOTCLK	-8365	-409
42	ENABLE	-8295	-409
43	DB17	-8225	-409
44	DB16	-8155	-409
45	DB15	-8085	-409
46	DB14	-8015	-409
47	DB13	-7945	-409
48	DB12	-7875	-409
49	DB11	-7805	-409
50	DB10	-7735	-409
51	DB9	-7665	-409
52	DB8	-7595	-409
53	DB7	-7525	-409
54	DB6	-7455	-409
55	DB5	-7385	-409
56	DB4	-7315	-409
57	DB3	-7245	-409
58	DB2	-7175	-409
59	DB1	-7105	-409
60	DB0	-7035	-409

No	Name	X	Y
61	SD0	-6965	-409
62	DIN SDA	-6895	-409
63	nRD	-6825	-409
64	SCL	-6755	-409
65	D/CX	-6685	-409
66	nCS	-6615	-409
67	TE	-6545	-409
68	IOVCC	-6475	-409
69	IOVCC	-6405	-409
70	IOVCC	-6335	-409
71	IOVCC	-6265	-409
72	IOVCC	-6195	-409
73	IOVCC	-6125	-409
74	IOVCC	-6055	-409
75	VDD	-5985	-409
76	VDD	-5915	-409
77	VDD	-5845	-409
78	VDD	-5775	-409
79	VDD	-5705	-409
80	VDD	-5635	-409
81	VDD	-5565	-409
82	VDD	-5495	-409
83	VDD	-5425	-409
84	VDD	-5355	-409
85	VDD	-5285	-409
86	AGND	-5215	-409
87	AGND	-5145	-409
88	AGND	-5075	-409
89	AGND	-5005	-409
90	AGND	-4935	-409
91	AGND	-4865	-409
92	AGND	-4795	-409
93	AGND	-4725	-409
94	VGS	-4655	-409
95	VGS	-4585	-409
96	TEST1	-4515	-409
97	AGND	-4445	-409
98	AGND	-4375	-409
99	AGND	-4305	-409
100	AGND	-4235	-409
101	AGND	-4165	-409
102	AGND	-4095	-409
103	AGND	-4025	-409
104	AGND	-3955	-409
105	AGND	-3885	-409
106	AGND	-3815	-409
107	VCOM	-3745	-409
108	VCOM	-3675	-409
109	VCOM	-3605	-409
110	VCOM	-3535	-409
111	VCOM	-3465	-409
112	VCOM	-3395	-409
113	VCOM	-3325	-409
114	VCOM	-3255	-409
115	VCOM	-3185	-409
116	VCOM	-3115	-409
117	VCOM	-3045	-409
118	VCOM	-2975	-409
119	VCOM	-2905	-409
120	VCOM	-2835	-409

No	Name	X	Y
121	VCOM	-2765	-409
122	VCOM	-2695	-409
123	VCOMH	-2625	-409
124	VCOMH	-2555	-409
125	VCOMH	-2485	-409
126	VCOMH	-2415	-409
127	VCOMH	-2345	-409
128	VCOMH	-2275	-409
129	VCOMH	-2205	-409
130	VCOMH	-2135	-409
131	VCOMH	-2065	-409
132	VCOMH	-1995	-409
133	VCOML	-1925	-409
134	VCOML	-1855	-409
135	VCOML	-1785	-409
136	VCOML	-1715	-409
137	VCOML	-1645	-409
138	VCOML	-1575	-409
139	VCOML	-1505	-409
140	VREG1OUT	-1435	-409
141	VREG1OUT	-1365	-409
142	VREG1OUT	-1295	-409
143	VREG1OUT	-1225	-409
144	TEST2	-1155	-409
145	VCL	-1085	-409
146	VCL	-1015	-409
147	VCL	-945	-409
148	VCL	-875	-409
149	VCL	-805	-409
150	VCL	-735	-409
151	VCL	-665	-409
152	VCL	-595	-409
153	VCL	-525	-409
154	DDVDH	-455	-409
155	DDVDH	-385	-409
156	DDVDH	-315	-409
157	DDVDH	-245	-409
158	DDVDH	-175	-409
159	DDVDH	-105	-409
160	DDVDH	-35	-409
161	DDVDH	35	-409
162	DDVDH	105	-409
163	VCI1	175	-409
164	VCI1	245	-409
165	VCI1	315	-409
166	VCI1	385	-409
167	VCI1	455	-409
168	VCI1	525	-409
169	VCI1	595	-409
170	VCI1	665	-409
171	VCI1	735	-409
172	VCI1	805	-409
173	VCI1	875	-409
174	VCI	945	-409
175	VCI	1015	-409
176	VCI	1085	-409
177	VCI	1155	-409
178	VCI	1225	-409
179	VCI	1295	-409
180	VCI	1365	-409

No	Name	X	Y
181	VCI	1435	-409
182	VCI	1505	-409
183	VCI	1575	-409
184	VCI	1645	-409
185	VCI	1715	-409
186	VCI	1785	-409
187	VCI	1855	-409
188	VCI	1925	-409
189	VCI	1995	-409
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288	C21A	8925	-409
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334	G23	11010	389
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355	G65	10695	244
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359	G73	10635	244
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369	G93	10485	244
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376	G107	10380	389
377	G109	10365	244
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379	G113	10335	244
380	G115	10320	389
381	G117	10305	244
382	G119	10290	389
383	G121	10275	244
384	G123	10260	389
385	G125	10245	244
386	G127	10230	389
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410	G175	9870	389
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415	G185	9795	244
416	G187	9780	389
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418	G191	9750	389
419	G193	9735	244
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425	G205	9645	244
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445	G245	9345	244
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455	G265	9195	244
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457	G269	9165	244
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556	G467	7680	389
557	G469	7665	244
558	G471	7650	389
559	G473	7635	244
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561	G477	7605	244
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565	DUMMY	7395	244
566	DUMMY	7380	389
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573	S954	7275	244
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613	S914	6675	244
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635	S892	6345	244
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657	S870	6015	244
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659	S868	5985	244
660	S867	5970	389

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687	S840	5565	244
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693	S834	5475	244
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697	S830	5415	244
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703	S824	5325	244
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705	S822	5295	244
706	S821	5280	389
707	S820	5265	244
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709	S818	5235	244
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711	S816	5205	244
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713	S814	5175	244
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715	S812	5145	244
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717	S810	5115	244
718	S809	5100	389
719	S808	5085	244
720	S807	5070	389

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727	S800	4965	244
728	S799	4950	389
729	S798	4935	244
730	S797	4920	389
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732	S795	4890	389
733	S794	4875	244
734	S793	4860	389
735	S792	4845	244
736	S791	4830	389
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738	S789	4800	389
739	S788	4785	244
740	S787	4770	389
741	S786	4755	244
742	S785	4740	389
743	S784	4725	244
744	S783	4710	389
745	S782	4695	244
746	S781	4680	389
747	S780	4665	244
748	S779	4650	389
749	S778	4635	244
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753	S774	4575	244
754	S773	4560	389
755	S772	4545	244
756	S771	4530	389
757	S770	4515	244
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759	S768	4485	244
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765	S762	4395	244
766	S761	4380	389
767	S760	4365	244
768	S759	4350	389
769	S758	4335	244
770	S757	4320	389
771	S756	4305	244
772	S755	4290	389
773	S754	4275	244
774	S753	4260	389
775	S752	4245	244
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777	S750	4215	244
778	S749	4200	389
779	S748	4185	244
780	S747	4170	389

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786	S741	4080	389
787	S740	4065	244
788	S739	4050	389
789	S738	4035	244
790	S737	4020	389
791	S736	4005	244
792	S735	3990	389
793	S734	3975	244
794	S733	3960	389
795	S732	3945	244
796	S731	3930	389
797	S730	3915	244
798	S729	3900	389
799	S728	3885	244
800	S727	3870	389
801	S726	3855	244
802	S725	3840	389
803	S724	3825	244
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805	S722	3795	244
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807	S720	3765	244
808	S719	3750	389
809	S718	3735	244
810	S717	3720	389
811	S716	3705	244
812	S715	3690	389
813	S714	3675	244
814	S713	3660	389
815	S712	3645	244
816	S711	3630	389
817	S710	3615	244
818	S709	3600	389
819	S708	3585	244
820	S707	3570	389
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825	S702	3495	244
826	S701	3480	389
827	S700	3465	244
828	S699	3450	389
829	S698	3435	244
830	S697	3420	389
831	S696	3405	244
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845	S682	3195	244
846	S681	3180	389
847	S680	3165	244
848	S679	3150	389
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853	S674	3075	244
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863	S664	2925	244
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872	S655	2790	389
873	S654	2775	244
874	S653	2760	389
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887	S640	2565	244
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891	S636	2505	244
892	S635	2490	389
893	S634	2475	244
894	S633	2460	389
895	S632	2445	244
896	S631	2430	389
897	S630	2415	244
898	S629	2400	389
899	S628	2385	244
900	S627	2370	389

No	Name	X	Y
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903	S624	2325	244
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905	S622	2295	244
906	S621	2280	389
907	S620	2265	244
908	S619	2250	389
909	S618	2235	244
910	S617	2220	389
911	S616	2205	244
912	S615	2190	389
913	S614	2175	244
914	S613	2160	389
915	S612	2145	244
916	S611	2130	389
917	S610	2115	244
918	S609	2100	389
919	S608	2085	244
920	S607	2070	389
921	S606	2055	244
922	S605	2040	389
923	S604	2025	244
924	S603	2010	389
925	S602	1995	244
926	S601	1980	389
927	S600	1965	244
928	S599	1950	389
929	S598	1935	244
930	S597	1920	389
931	S596	1905	244
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933	S594	1875	244
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937	S590	1815	244
938	S589	1800	389
939	S588	1785	244
940	S587	1770	389
941	S586	1755	244
942	S585	1740	389
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944	S583	1710	389
945	S582	1695	244
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947	S580	1665	244
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958	S569	1500	389
959	S568	1485	244
960	S567	1470	389

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978	S549	1200	389
979	S548	1185	244
980	S547	1170	389
981	S546	1155	244
982	S545	1140	389
983	S544	1125	244
984	S543	1110	389
985	S542	1095	244
986	S541	1080	389
987	S540	1065	244
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990	S537	1020	389
991	S536	1005	244
992	S535	990	389
993	S534	975	244
994	S533	960	389
995	S532	945	244
996	S531	930	389
997	S530	915	244
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999	S528	885	244
1000	S527	870	389
1001	S526	855	244
1002	S525	840	389
1003	S524	825	244
1004	S523	810	389
1005	S522	795	244
1006	S521	780	389
1007	S520	765	244
1008	S519	750	389
1009	S518	735	244
1010	S517	720	389
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1013	S514	675	244
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1015	S512	645	244
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1017	S510	615	244
1018	S509	600	389
1019	S508	585	244
1020	S507	570	389

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1023	S504	525	244
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1025	S502	495	244
1026	S501	480	389
1027	S500	465	244
1028	S499	450	389
1029	S498	435	244
1030	S497	420	389
1031	S496	405	244
1032	S495	390	389
1033	S494	375	244
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1035	S492	345	244
1036	S491	330	389
1037	S490	315	244
1038	S489	300	389
1039	S488	285	244
1040	S487	270	389
1041	S486	255	244
1042	S485	240	389
1043	S484	225	244
1044	S483	210	389
1045	S482	195	244
1046	S481	180	389
1047	V1T(DUMMY)	165	244
1048	DUMMY	150	389
1049	DUMMY	-150	389
1050	V62T(DUMMY)	-165	244
1051	S480	-180	389
1052	S479	-195	244
1053	S478	-210	389
1054	S477	-225	244
1055	S476	-240	389
1056	S475	-255	244
1057	S474	-270	389
1058	S473	-285	244
1059	S472	-300	389
1060	S471	-315	244
1061	S470	-330	389
1062	S469	-345	244
1063	S468	-360	389
1064	S467	-375	244
1065	S466	-390	389
1066	S465	-405	244
1067	S464	-420	389
1068	S463	-435	244
1069	S462	-450	389
1070	S461	-465	244
1071	S460	-480	389
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1073	S458	-510	389
1074	S457	-525	244
1075	S456	-540	389
1076	S455	-555	244
1077	S454	-570	389
1078	S453	-585	244
1079	S452	-600	389
1080	S451	-615	244

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1084	S447	-675	244
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1086	S445	-705	244
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1088	S443	-735	244
1089	S442	-750	389
1090	S441	-765	244
1091	S440	-780	389
1092	S439	-795	244
1093	S438	-810	389
1094	S437	-825	244
1095	S436	-840	389
1096	S435	-855	244
1097	S434	-870	389
1098	S433	-885	244
1099	S432	-900	389
1100	S431	-915	244
1101	S430	-930	389
1102	S429	-945	244
1103	S428	-960	389
1104	S427	-975	244
1105	S426	-990	389
1106	S425	-1005	244
1107	S424	-1020	389
1108	S423	-1035	244
1109	S422	-1050	389
1110	S421	-1065	244
1111	S420	-1080	389
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1113	S418	-1110	389
1114	S417	-1125	244
1115	S416	-1140	389
1116	S415	-1155	244
1117	S414	-1170	389
1118	S413	-1185	244
1119	S412	-1200	389
1120	S411	-1215	244
1121	S410	-1230	389
1122	S409	-1245	244
1123	S408	-1260	389
1124	S407	-1275	244
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1135	S396	-1440	389
1136	S395	-1455	244
1137	S394	-1470	389
1138	S393	-1485	244
1139	S392	-1500	389
1140	S391	-1515	244

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1144	S387	-1575	244
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1159	S372	-1800	389
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1165	S366	-1890	389
1166	S365	-1905	244
1167	S364	-1920	389
1168	S363	-1935	244
1169	S362	-1950	389
1170	S361	-1965	244
1171	S360	-1980	389
1172	S359	-1995	244
1173	S358	-2010	389
1174	S357	-2025	244
1175	S356	-2040	389
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1177	S354	-2070	389
1178	S353	-2085	244
1179	S352	-2100	389
1180	S351	-2115	244
1181	S350	-2130	389
1182	S349	-2145	244
1183	S348	-2160	389
1184	S347	-2175	244
1185	S346	-2190	389
1186	S345	-2205	244
1187	S344	-2220	389
1188	S343	-2235	244
1189	S342	-2250	389
1190	S341	-2265	244
1191	S340	-2280	389
1192	S339	-2295	244
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1194	S337	-2325	244
1195	S336	-2340	389
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1197	S334	-2370	389
1198	S333	-2385	244
1199	S332	-2400	389
1200	S331	-2415	244

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No	Name	X	Y
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1207	S324	-2520	389
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1209	S322	-2550	389
1210	S321	-2565	244
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1212	S319	-2595	244
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1223	S308	-2760	389
1224	S307	-2775	244
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1226	S305	-2805	244
1227	S304	-2820	389
1228	S303	-2835	244
1229	S302	-2850	389
1230	S301	-2865	244
1231	S300	-2880	389
1232	S299	-2895	244
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1235	S296	-2940	389
1236	S295	-2955	244
1237	S294	-2970	389
1238	S293	-2985	244
1239	S292	-3000	389
1240	S291	-3015	244
1241	S290	-3030	389
1242	S289	-3045	244
1243	S288	-3060	389
1244	S287	-3075	244
1245	S286	-3090	389
1246	S285	-3105	244
1247	S284	-3120	389
1248	S283	-3135	244
1249	S282	-3150	389
1250	S281	-3165	244
1251	S280	-3180	389
1252	S279	-3195	244
1253	S278	-3210	389
1254	S277	-3225	244
1255	S276	-3240	389
1256	S275	-3255	244
1257	S274	-3270	389
1258	S273	-3285	244
1259	S272	-3300	389
1260	S271	-3315	244

No	Name	X	Y
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1263	S268	-3360	389
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1265	S266	-3390	389
1266	S265	-3405	244
1267	S264	-3420	389
1268	S263	-3435	244
1269	S262	-3450	389
1270	S261	-3465	244
1271	S260	-3480	389
1272	S259	-3495	244
1273	S258	-3510	389
1274	S257	-3525	244
1275	S256	-3540	389
1276	S255	-3555	244
1277	S254	-3570	389
1278	S253	-3585	244
1279	S252	-3600	389
1280	S251	-3615	244
1281	S250	-3630	389
1282	S249	-3645	244
1283	S248	-3660	389
1284	S247	-3675	244
1285	S246	-3690	389
1286	S245	-3705	244
1287	S244	-3720	389
1288	S243	-3735	244
1289	S242	-3750	389
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1297	S234	-3870	389
1298	S233	-3885	244
1299	S232	-3900	389
1300	S231	-3915	244
1301	S230	-3930	389
1302	S229	-3945	244
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1305	S226	-3990	389
1306	S225	-4005	244
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1309	S222	-4050	389
1310	S221	-4065	244
1311	S220	-4080	389
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1315	S216	-4140	389
1316	S215	-4155	244
1317	S214	-4170	389
1318	S213	-4185	244
1319	S212	-4200	389
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1329	S202	-4350	389
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1332	S199	-4395	244
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1337	S194	-4470	389
1338	S193	-4485	244
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1341	S190	-4530	389
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1343	S188	-4560	389
1344	S187	-4575	244
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1350	S181	-4665	244
1351	S180	-4680	389
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1367	S164	-4920	389
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1369	S162	-4950	389
1370	S161	-4965	244
1371	S160	-4980	389
1372	S159	-4995	244
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1376	S155	-5055	244
1377	S154	-5070	389
1378	S153	-5085	244
1379	S152	-5100	389
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1386	S145	-5205	244
1387	S144	-5220	389
1388	S143	-5235	244
1389	S142	-5250	389
1390	S141	-5265	244
1391	S140	-5280	389
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1393	S138	-5310	389
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1396	S135	-5355	244
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1398	S133	-5385	244
1399	S132	-5400	389
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1401	S130	-5430	389
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1437	S94	-5970	389
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1439	S92	-6000	389
1440	S91	-6015	244

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1447	S84	-6120	389
1448	S83	-6135	244
1449	S82	-6150	389
1450	S81	-6165	244
1451	S80	-6180	389
1452	S79	-6195	244
1453	S78	-6210	389
1454	S77	-6225	244
1455	S76	-6240	389
1456	S75	-6255	244
1457	S74	-6270	389
1458	S73	-6285	244
1459	S72	-6300	389
1460	S71	-6315	244
1461	S70	-6330	389
1462	S69	-6345	244
1463	S68	-6360	389
1464	S67	-6375	244
1465	S66	-6390	389
1466	S65	-6405	244
1467	S64	-6420	389
1468	S63	-6435	244
1469	S62	-6450	389
1470	S61	-6465	244
1471	S60	-6480	389
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1473	S58	-6510	389
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1477	S54	-6570	389
1478	S53	-6585	244
1479	S52	-6600	389
1480	S51	-6615	244
1481	S50	-6630	389
1482	S49	-6645	244
1483	S48	-6660	389
1484	S47	-6675	244
1485	S46	-6690	389
1486	S45	-6705	244
1487	S44	-6720	389
1488	S43	-6735	244
1489	S42	-6750	389
1490	S41	-6765	244
1491	S40	-6780	389
1492	S39	-6795	244
1493	S38	-6810	389
1494	S37	-6825	244
1495	S36	-6840	389
1496	S35	-6855	244
1497	S34	-6870	389
1498	S33	-6885	244
1499	S32	-6900	389
1500	S31	-6915	244

No	Name	X	Y
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1509	S22	-7050	389
1510	S21	-7065	244
1511	S20	-7080	389
1512	S19	-7095	244
1513	S18	-7110	389
1514	S17	-7125	244
1515	S16	-7140	389
1516	S15	-7155	244
1517	S14	-7170	389
1518	S13	-7185	244
1519	S12	-7200	389
1520	S11	-7215	244
1521	S10	-7230	389
1522	S9	-7245	244
1523	S8	-7260	389
1524	S7	-7275	244
1525	S6	-7290	389
1526	S5	-7305	244
1527	S4	-7320	389
1528	S3	-7335	244
1529	S2	-7350	389
1530	S1	-7365	244
1531	DUMMY	-7380	389
1532	DUMMY	-7395	244
1533	DUMMY	-7560	389
1534	DUMMY	-7575	244
1535	G480	-7590	389
1536	G478	-7605	244
1537	G476	-7620	389
1538	G474	-7635	244
1539	G472	-7650	389
1540	G470	-7665	244
1541	G468	-7680	389
1542	G466	-7695	244
1543	G464	-7710	389
1544	G462	-7725	244
1545	G460	-7740	389
1546	G458	-7755	244
1547	G456	-7770	389
1548	G454	-7785	244
1549	G452	-7800	389
1550	G450	-7815	244
1551	G448	-7830	389
1552	G446	-7845	244
1553	G444	-7860	389
1554	G442	-7875	244
1555	G440	-7890	389
1556	G438	-7905	244
1557	G436	-7920	389
1558	G434	-7935	244
1559	G432	-7950	389
1560	G430	-7965	244

No	Name	X	Y
1561	G428	-7980	389
1562	G426	-7995	244
1563	G424	-8010	389
1564	G422	-8025	244
1565	G420	-8040	389
1566	G418	-8055	244
1567	G416	-8070	389
1568	G414	-8085	244
1569	G412	-8100	389
1570	G410	-8115	244
1571	G408	-8130	389
1572	G406	-8145	244
1573	G404	-8160	389
1574	G402	-8175	244
1575	G400	-8190	389
1576	G398	-8205	244
1577	G396	-8220	389
1578	G394	-8235	244
1579	G392	-8250	389
1580	G390	-8265	244
1581	G388	-8280	389
1582	G386	-8295	244
1583	G384	-8310	389
1584	G382	-8325	244
1585	G380	-8340	389
1586	G378	-8355	244
1587	G376	-8370	389
1588	G374	-8385	244
1589	G372	-8400	389
1590	G370	-8415	244
1591	G368	-8430	389
1592	G366	-8445	244
1593	G364	-8460	389
1594	G362	-8475	244
1595	G360	-8490	389
1596	G358	-8505	244
1597	G356	-8520	389
1598	G354	-8535	244
1599	G352	-8550	389
1600	G350	-8565	244
1601	G348	-8580	389
1602	G346	-8595	244
1603	G344	-8610	389
1604	G342	-8625	244
1605	G340	-8640	389
1606	G338	-8655	244
1607	G336	-8670	389
1608	G334	-8685	244
1609	G332	-8700	389
1610	G330	-8715	244
1611	G328	-8730	389
1612	G326	-8745	244
1613	G324	-8760	389
1614	G322	-8775	244
1615	G320	-8790	389
1616	G318	-8805	244
1617	G316	-8820	389
1618	G314	-8835	244
1619	G312	-8850	389
1620	G310	-8865	244

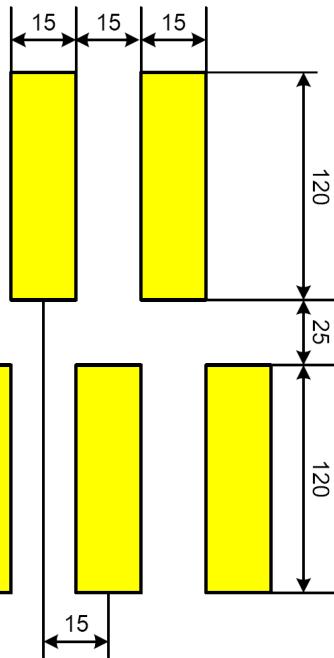
No	Name	X	Y
1621	G308	-8880	389
1622	G306	-8895	244
1623	G304	-8910	389
1624	G302	-8925	244
1625	G300	-8940	389
1626	G298	-8955	244
1627	G296	-8970	389
1628	G294	-8985	244
1629	G292	-9000	389
1630	G290	-9015	244
1631	G288	-9030	389
1632	G286	-9045	244
1633	G284	-9060	389
1634	G282	-9075	244
1635	G280	-9090	389
1636	G278	-9105	244
1637	G276	-9120	389
1638	G274	-9135	244
1639	G272	-9150	389
1640	G270	-9165	244
1641	G268	-9180	389
1642	G266	-9195	244
1643	G264	-9210	389
1644	G262	-9225	244
1645	G260	-9240	389
1646	G258	-9255	244
1647	G256	-9270	389
1648	G254	-9285	244
1649	G252	-9300	389
1650	G250	-9315	244
1651	G248	-9330	389
1652	G246	-9345	244
1653	G244	-9360	389
1654	G242	-9375	244
1655	G240	-9390	389
1656	G238	-9405	244
1657	G236	-9420	389
1658	G234	-9435	244
1659	G232	-9450	389
1660	G230	-9465	244
1661	G228	-9480	389
1662	G226	-9495	244
1663	G224	-9510	389
1664	G222	-9525	244
1665	G220	-9540	389
1666	G218	-9555	244
1667	G216	-9570	389
1668	G214	-9585	244
1669	G212	-9600	389
1670	G210	-9615	244
1671	G208	-9630	389
1672	G206	-9645	244
1673	G204	-9660	389
1674	G202	-9675	244
1675	G200	-9690	389
1676	G198	-9705	244
1677	G196	-9720	389
1678	G194	-9735	244
1679	G192	-9750	389
1680	G190	-9765	244

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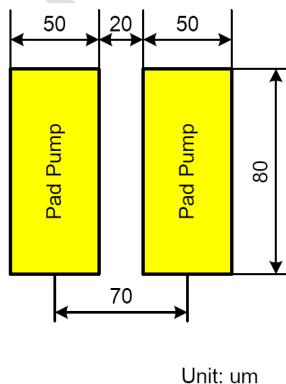
No	Name	X	Y
1681	G188	-9780	389
1682	G186	-9795	244
1683	G184	-9810	389
1684	G182	-9825	244
1685	G180	-9840	389
1686	G178	-9855	244
1687	G176	-9870	389
1688	G174	-9885	244
1689	G172	-9900	389
1690	G170	-9915	244
1691	G168	-9930	389
1692	G166	-9945	244
1693	G164	-9960	389
1694	G162	-9975	244
1695	G160	-9990	389
1696	G158	-10005	244
1697	G156	-10020	389
1698	G154	-10035	244
1699	G152	-10050	389
1700	G150	-10065	244
1701	G148	-10080	389
1702	G146	-10095	244
1703	G144	-10110	389
1704	G142	-10125	244
1705	G140	-10140	389
1706	G138	-10155	244
1707	G136	-10170	389
1708	G134	-10185	244
1709	G132	-10200	389
1710	G130	-10215	244
1711	G128	-10230	389
1712	G126	-10245	244
1713	G124	-10260	389
1714	G122	-10275	244
1715	G120	-10290	389
1716	G118	-10305	244
1717	G116	-10320	389
1718	G114	-10335	244
1719	G112	-10350	389
1720	G110	-10365	244
1721	G108	-10380	389
1722	G106	-10395	244
1723	G104	-10410	389
1724	G102	-10425	244
1725	G100	-10440	389
1726	G98	-10455	244
1727	G96	-10470	389
1728	G94	-10485	244
1729	G92	-10500	389
1730	G90	-10515	244
1731	G88	-10530	389
1732	G86	-10545	244
1733	G84	-10560	389
1734	G82	-10575	244
1735	G80	-10590	389
1736	G78	-10605	244
1737	G76	-10620	389
1738	G74	-10635	244
1739	G72	-10650	389
1740	G70	-10665	244

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S1 ~ S960
G1 ~ G480 (No. 321 ~ 1776)



I/O Pads
(No. 1 ~ 320)



6. Block Function Description

Interface

The RM68041 incorporates command method 18-/16-/9-/8-bits bus display command interface, which consists of 8 bits command registers and 8 bits parameter registers. Parameter registers consist of 8 bits write data register (WDR) and 8bit read data register (RDR).

WDR stores data to be written into GRAM or parameters temporarily while RDR stores data read out from GRAM temporarily. When data is written from microcomputer to GRAM, the RM68041 writes firstly to WDR, and then the data is written to GRAM automatically by internal operation. Because read out operation from GRAM is conducted through RDR, first read out data is invalid. Normal data is read out from 2nd read out data.

Register selection			
DCX	RDX	WRX	Operation
0	1	↑	Command
1	↑	1	Read parameter
1	1	↑	Write parameter

Address Counter (AC)

Address counter (AC) gives address to GRAM. When command setting address is written to CDR, the data is transferred from CDR to AC.

When data is written to GRAM, address counter (AC) increments by +1 or -1 automatically. AC after data is read out increments by +1 or -1 likewise. The RM68041 writes data to only rectangular area that was specified by GRAM.

Graphic RAM (GRAM)

The graphic RAM (GRAM) stores 345,600 bytes bit pattern data using 18 bits for one pixel, enabling maximum 320RGB x 480 dot graphic display.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a liquid crystal drive voltage, which corresponds to grayscale level set in the y correction register. The RM68041 displays 262,144 colors at the maximum.

Power Supply Circuit

The power supply circuit generates supply voltages to a-TFT panel, VREG1OUT, VGH, VGL, VCOMH and VCOML.

Timing Generating

The timing generator generates timing signals for internal circuits such as the internal GRAM. The timing for display operation such as RAM read operation and the timing for internal operation such as RAM access by MPU is outputted separately so that they do not interfere with each other.

Oscillator

The RM68041 incorporates RC oscillator circuit. The frame frequency is changeable by command settings.

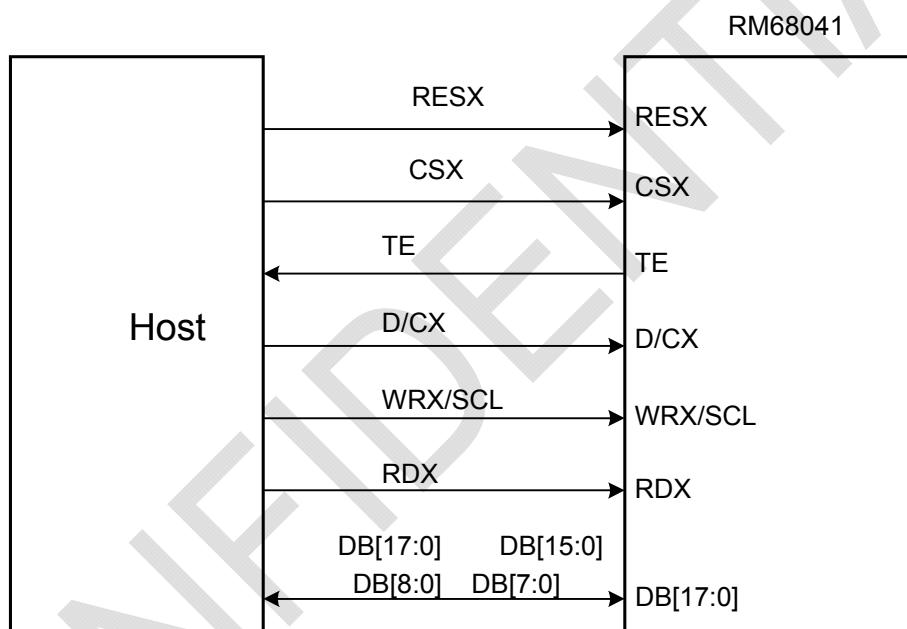
Panel Driver Circuit

The liquid crystal display driver circuit consists of 960 source drivers (S1~S960). Display pattern data is latched when 960 bytes data is input. This latched data controls source drivers and outputs drive waveform. The shift direction of 960-bit output from the source driver can be changed by setting commands. The gate driver consists of 480 gate drivers (G1~G480) and outputs either VGH or VGL level. The shift direction of gate driver is set by GS bit. Scan direction of gate driver is set by SM bit enabling users to set the RM68041 so that it suits mounting method.

7. Function Description

7.1. Display Bus Interface (DBI)

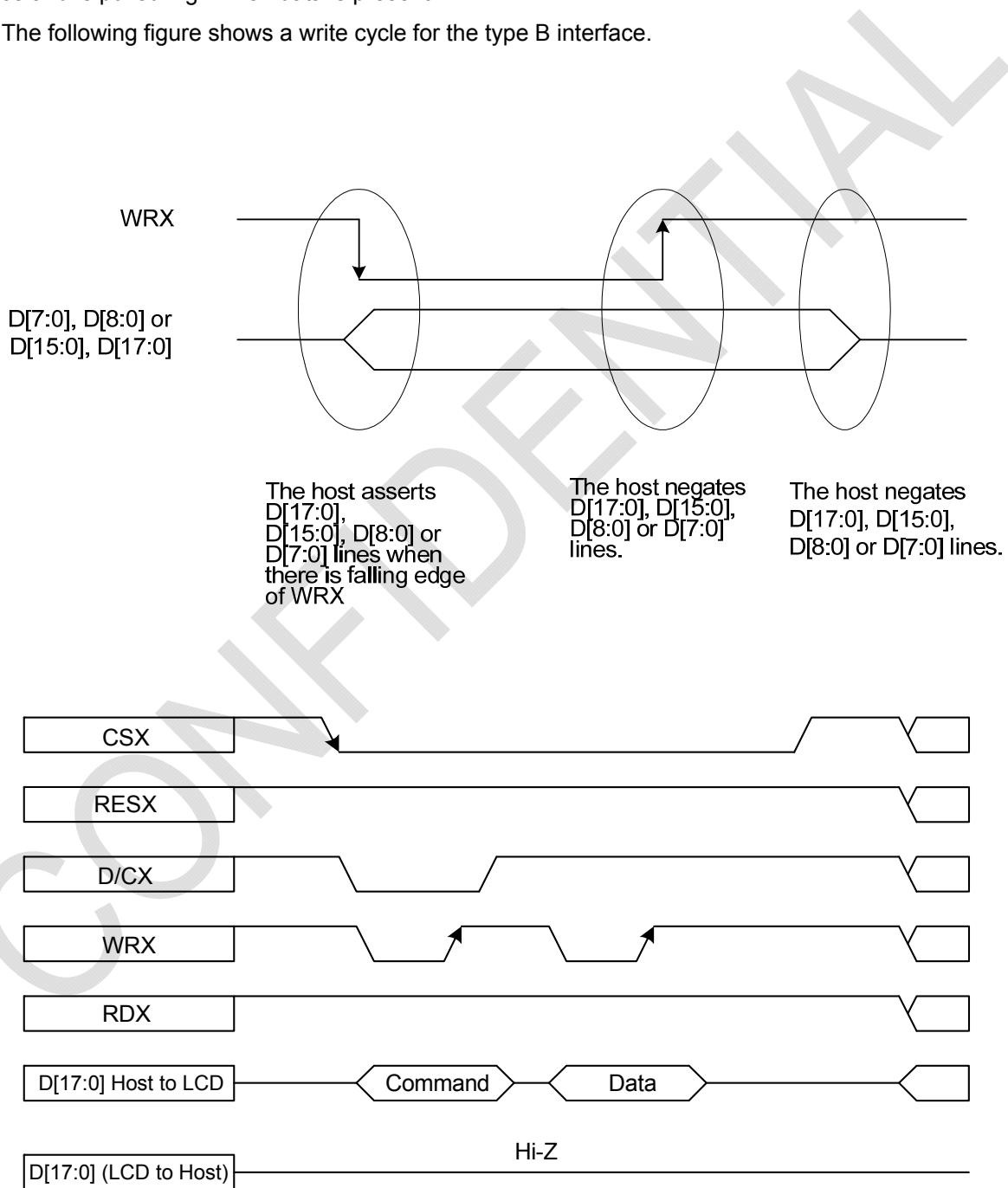
The RM68041 uses a 22-wires 18-bit parallel interface. The chip-select CSX (active low) enables and disables the DBI interface. RESX (active low) is an external reset signal. WRX is the data write, RDX is the data read and DB[17:0] is parallel DBI data. There are four 18/16/9/8-bit types interface supported for the display data transfer. The graphics controller chip reads the data at the rising edge of RDX signal. The D/CX is data/command flag. When D/CX = "1", D17 to D0 bits are display RAM data or command parameters. When D/CX = "0", D7 to D0 bits are commands.



7.1.1. Write Cycle

During a write cycle the host processor sends data to the display module via the interface. The Type B interface utilizes D/CX, RDX and WRX signals as well as all eight (D[7:0]), nine (D[8:0]), sixteen (D[15:0]) or eighteen (D[17:0]) information signals. WRX is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of WRX. D/CX is driven low while command information is on the interface and is pulled high when data is present.

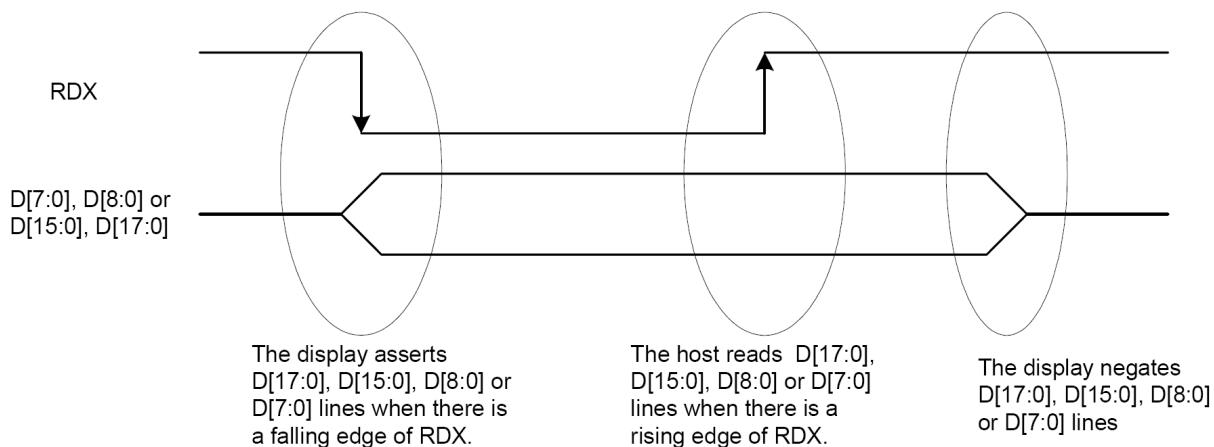
The following figure shows a write cycle for the type B interface.



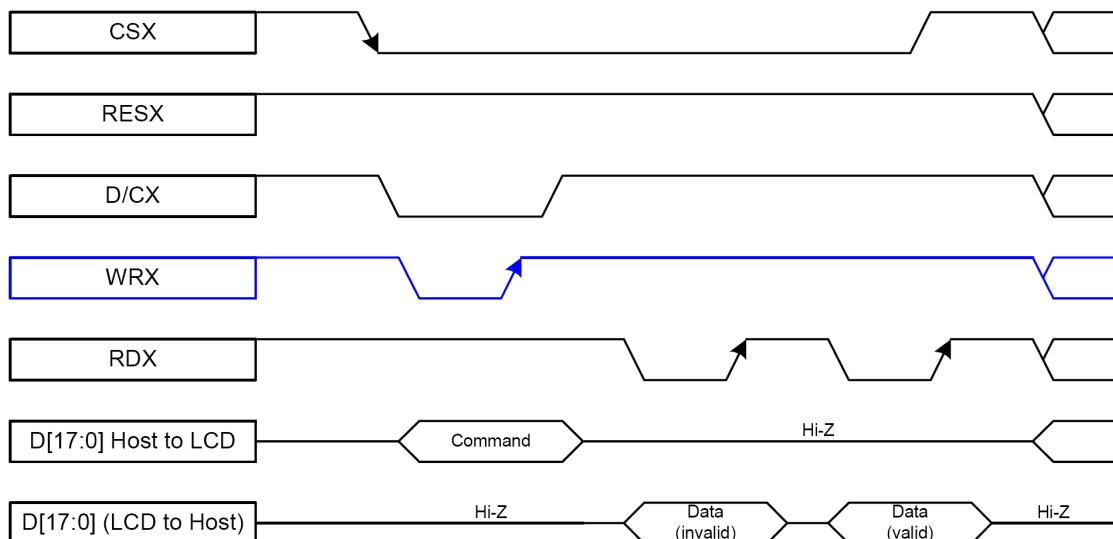
7.1.2. Read Cycle

During a read cycle the host processor reads data from the display module via the interface. The Type B interface utilizes D/CX, RDX and WRX signals as well as all eight (D[7:0]), nine (D[8:0]), sixteen (D[15:0]) or eighteen (D[17:0]) information signals. RDX is driven from high to low then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX. D/CX is driven high during the read cycle.

The following figure shows the read cycle for the type B interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read Data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

DBI Type B Interface

18-bit data bus DB[17:0] interface, IM[2:0] = 000

	Set_pixel_format	DFM	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Command/Parameter Write	*	*												D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	*	*												D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	Set_pixel_format	DFM	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

16-bit data bus DB[15:0] interface, IM[2:0] = 010

	Set_pixel_format	DFM	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Command/Parameter Write	*	*											D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	*	*											D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	Set_pixel_format	DFM	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
16bpp Frame Memory Write	3'h5	*	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Frame Memory Read	*	*	r4	r3	r2	r1	r0	g5	g4	g3	g2	g1	g0	b5	b4	b3	b2	b1	b0

	First Transfer				Second Transfer				Third Transfer								
Set_pixel_format	DFM	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]
18bpp Frame Memory Write	3'h6	0	R1[5:0]			G1[5:0]				B1[5:0]		R2[5:0]		G2[5:0]		B2[5:0]	
	1			R1[5:0]				G1[5:0]		B1[5:0]					R2[5:0]		

	First Transfer				Second Transfer				Third Transfer								
Set_pixel_format	DFM	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]
Frame Memory Read	0	r1[5:0]				g1[5:0]				b1[5:0]		r2[5:0]		g2[5:0]		b2[5:0]	
	1			r1[5:0]				g1[5:0]		b1[5:0]					r2[5:0]		

9-bit data bus DB[8:0] interface, IM[2:0] = 001

	Set_pixel_format	DFM	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*		D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	*	*		D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	First Transfer								Second Transfer											
Set_pixel_format	DFM	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
18bpp Frame Memory Write	3'h6	*	R[5]	R4	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	*	r[5]	r4	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

8-bit data bus DB[7:0] interface, IM[2:0] = 011

	Set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	*	*	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	Set_pixel_format	DFM	First Transfer						Second Transfer					
16bpp Frame Memory Write	3'h5	*	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]
Frame Memory Read	*	*	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[4]

	Set_pixel_format	DFM	First Transfer						Second Transfer						Third Transfer					
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

16-bit data extend to 18-bit

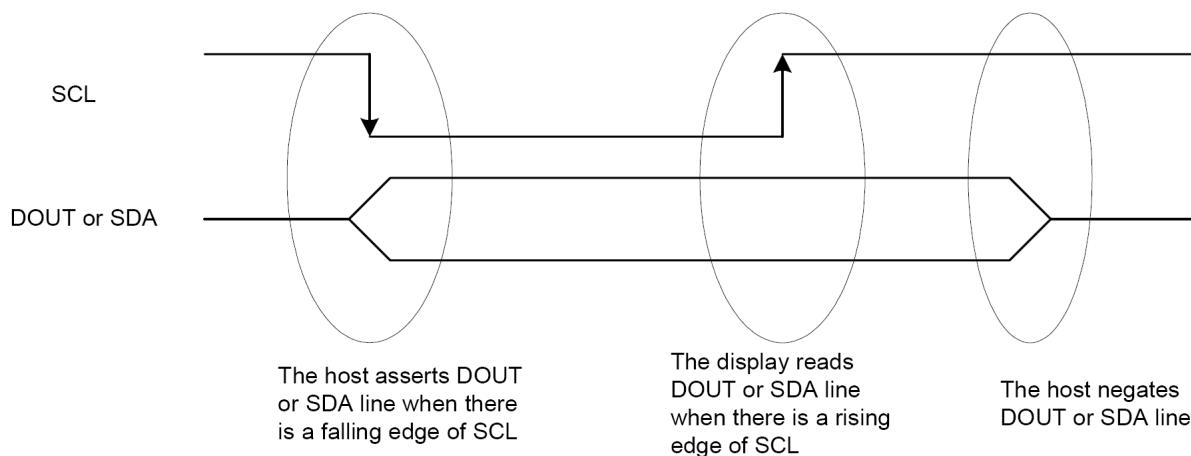
Frame Memory Data (18bpp)																			
Set_pixel_format	EPF[1:0]	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
	2'h0	R[4]	R[3]	R[2]	R[1]	R[0]	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	0
16bpp	2'h1	R[4]	R[3]	R[2]	R[1]	R[0]	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	1
	2'h2	R[4]	R[3]	R[2]	R[1]	R[0]	R4	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	B[4]

7.2. Serial Interface (Type C)

7.2.1. Write Cycle and Sequence

During a write cycle the host processor sends a single bit of data to the display module via the interface. The Type C interface utilizes CSX, SCL and SDA or DOUT signals. SCL is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of SCL.

The following figure shows the write cycle for the type C interface.

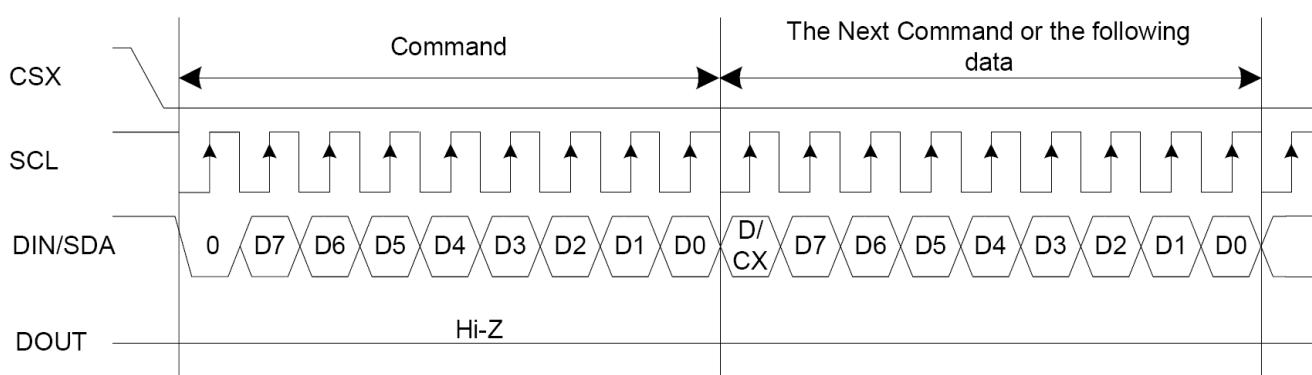


Note: SCL is an unsynchronized signal; it can be stopped.

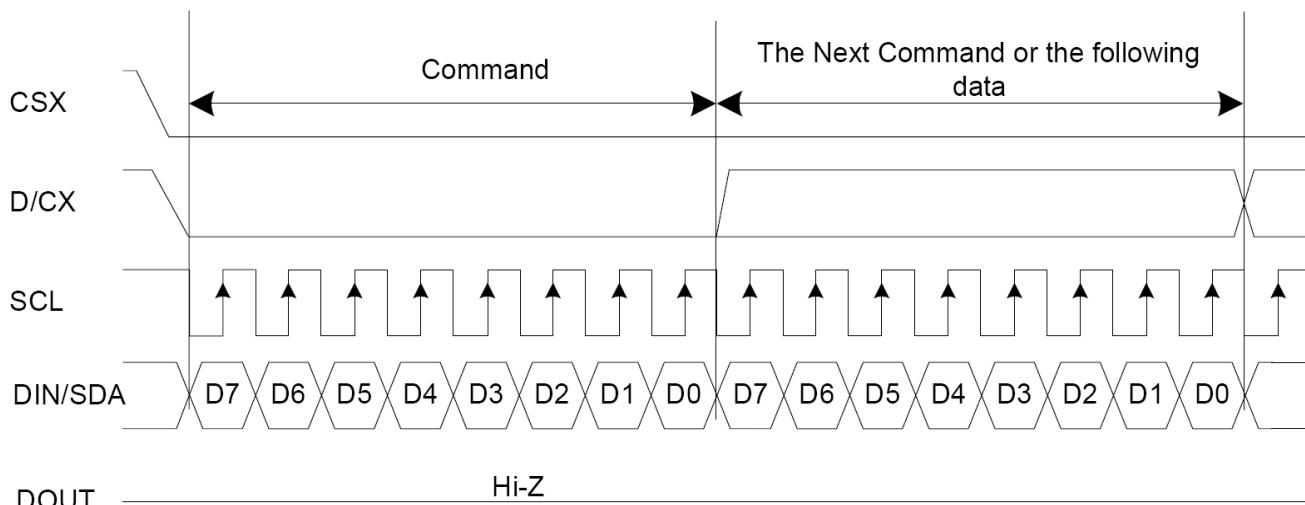
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During the write sequence the host processor writes one or more bytes of information to the display module via the interface. The write sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional D/CX signal is used a byte is eight write cycles long. D/CX is driven low while command information is on the interface and is pulled high when data is present.

The type C interface write sequences are described in the following figure.



DBI Type C Interface Write Sequence – Option 1



DBI Type C Interface Write Sequence – Option 3

Note:

- 1.) D7 is MSB and D0 is LSB of byte.
- 2.) When the Interface control register (C6h) SDA_EN is set as '1', the DIN/SDA pin is bi-directional and DOUT

pin is not used.

- 3.) When the Interface control register (C6h) SDA_EN is set as '0', the DIN/SDA pin is uni-direction and DIN and DOUT pins are used for data write and read.

DBI Type C Interface IM[2:0]=101/111

Set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
3bpp Frame Memory Write	3'h1	0	/	R1[0]	G1[0]	B1[0]	R2[0]	G2[0]	B2[0]	/	R3[0]	G3[0]	B3[0]	R4[0]	G4[0]	B4[0]	/	R5[0]	G5[0]	B5[0]	R6[0]	G6[0]	B6[0]				
	3'h1	1	/	R1[0]	G1[0]	B1[0]	/	R2[0]	G2[0]	B2[0]	/	R3[0]	G3[0]	B3[0]	/	R4[0]	G4[0]	B4[0]	/	R5[0]	G5[0]	B5[0]	R6[0]	G6[0]	B6[0]		
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]		G[5]	G[4]	G[3]	G[2]	G[1]	G[0]		B[5]	B[4]	B[3]	B[2]	B[1]	B[0]					
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]		g[5]	g[4]	g[3]	g[2]	g[1]	g[0]		b[5]	b[4]	b[3]	b[2]	b[1]	b[0]					

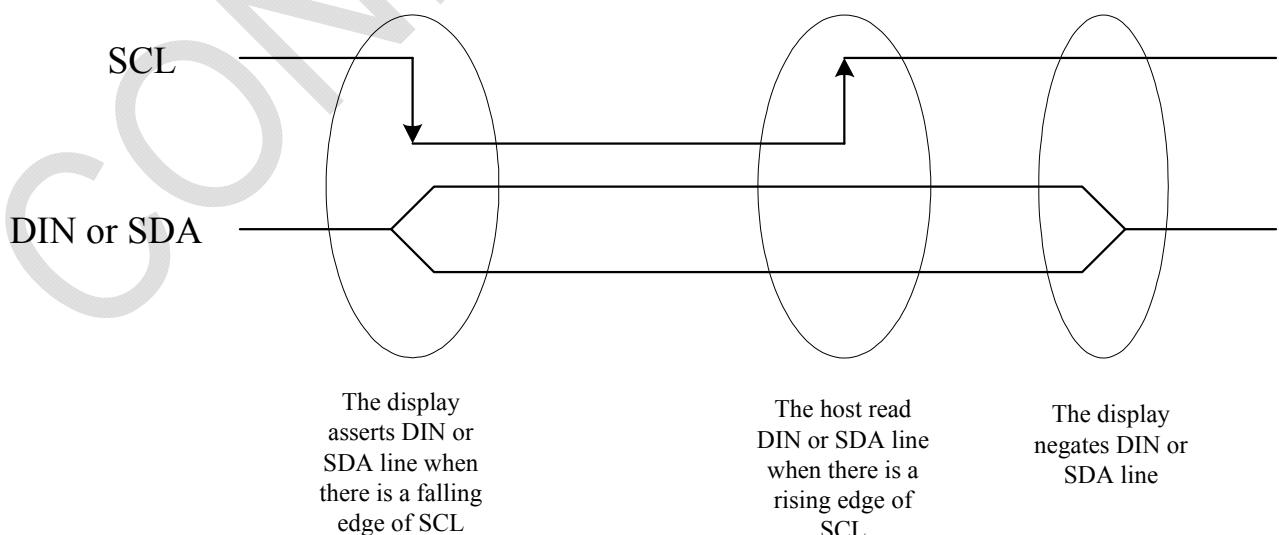
3/16-bit data extend to 18-bit

		Frame Memory Data (18bpp)																			
Set_pixel_format	EPF[1:0]	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
18bpp	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]		
3bpp	*	R[0]	R[0]	R[0]	R[0]	R[0]	R[0]	G[0]	G[0]	G[0]	G[0]	G[0]	G[0]	B[0]	B[0]	B[0]	B[0]	B[0]	B[0]		

7.2.2. Read Cycle and Sequence

During a read cycle the host processor reads a single bit of data from the display module via the interface. The Type C interface utilizes CSX, SCL and DIN signals. SCL is driven from high to low then pulled back to high during the read cycle. The display module provides information during the read cycle while the host processor reads the display module information on the rising edge of SCL. D/CX is driven during the read cycle if it is used in option 3.

The following figure shows the read cycle for the type C interface.

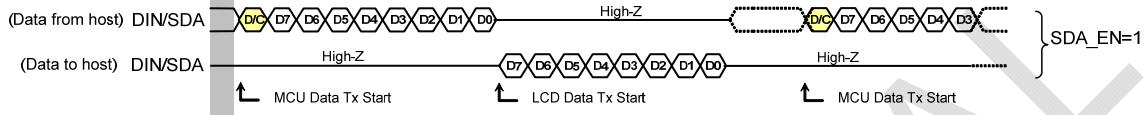
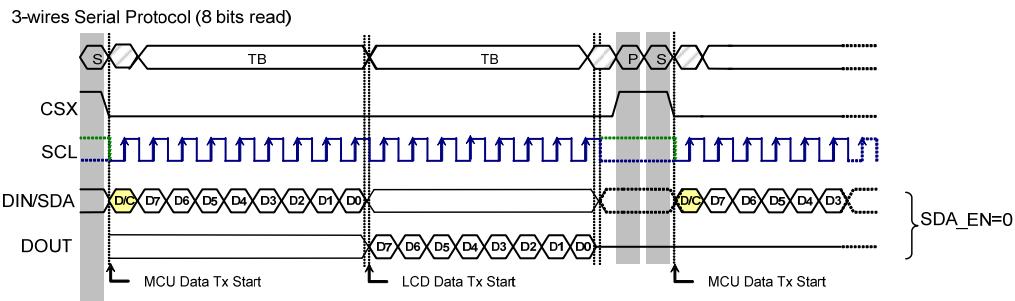


Note: SCL is an unsynchronized signal; it can be stopped.

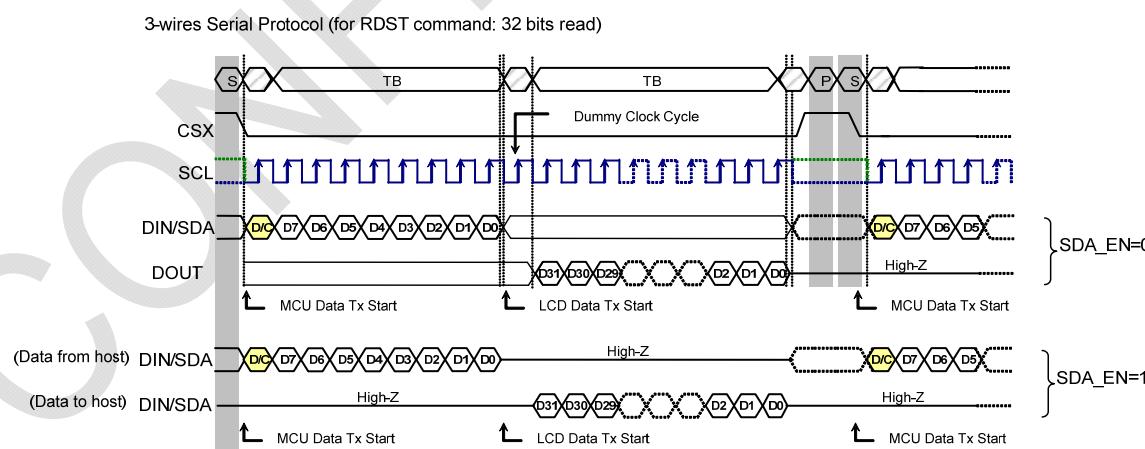
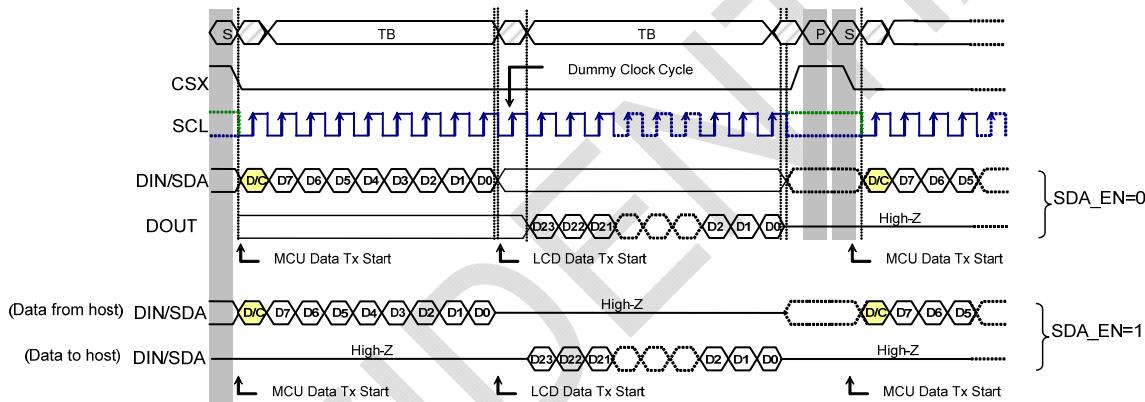
During the read sequence the host processor reads one or more bytes of information from the display module via the interface. The read sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional D/CX signal is used a byte is eight read cycles long. D/CX is driven low while command information is on the interface and is pulled high when data is present.

The type C interface read sequences are shown in the following figures.

(i) 3-wires serial interface:

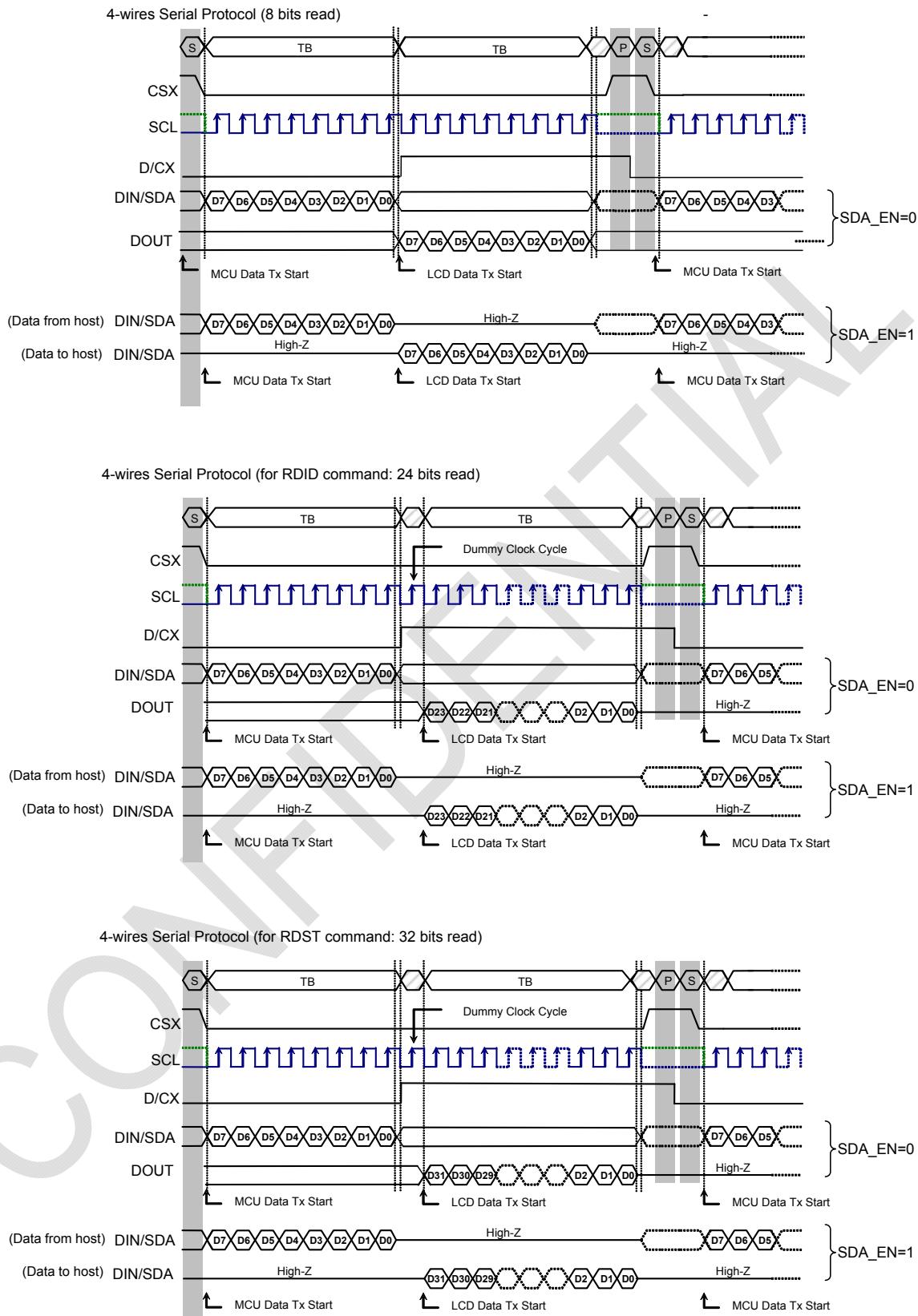


3-wires Serial Protocol (for RDID command: 24 bits read)



Note: D7 is MSB and D0 is LSB of byte.

(ii) 4-wires serial interface:

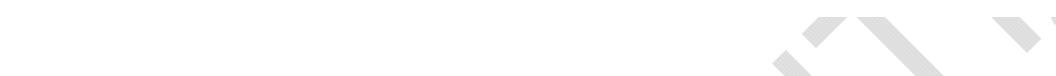
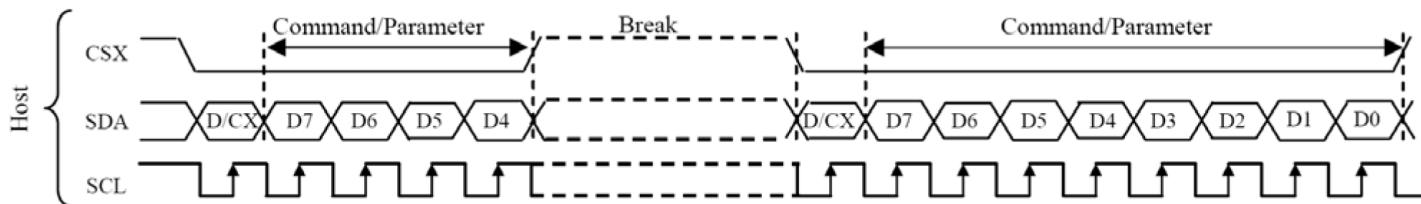


7.2.3. Break and Pause Sequences

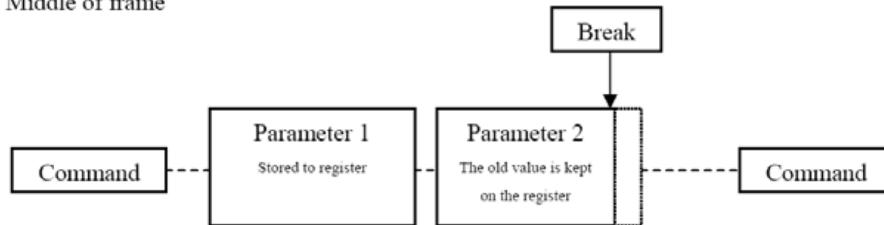
The host processor can break a read or write sequence by pulling the CSX signal high during a

command or data byte. The display module shall reset its interface so it will be ready to receive the same byte when CSX is again driven low.

The host processor can pause a read or write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the read or write sequence at the point where the sequence was paused.



1. Middle of frame

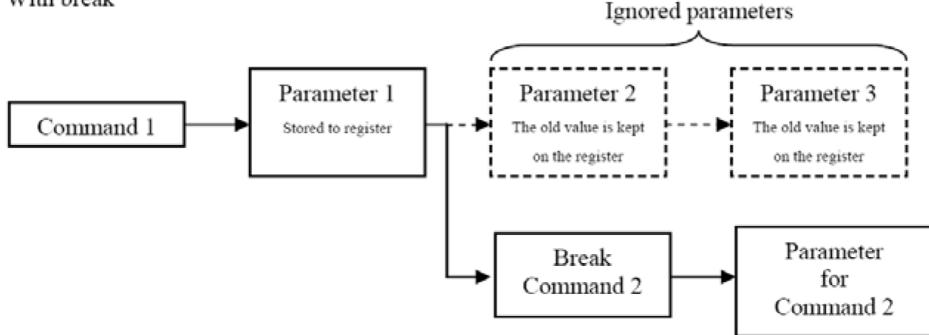


2. Between frames

Without break



With break



Break can be e.g. another command or noise pulse.

7.3. Display Pixel Interface (DPI)

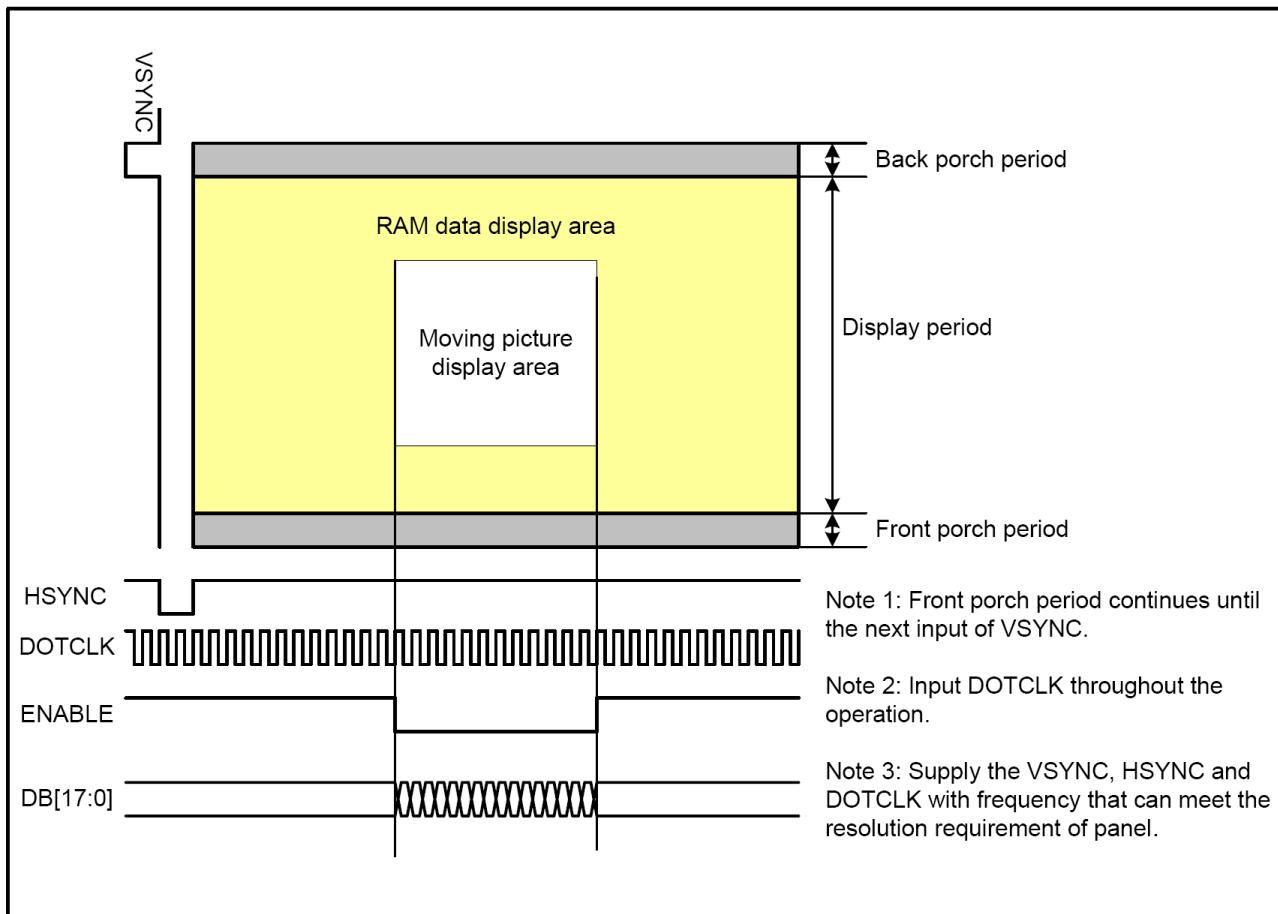
In normal operation, systems based on DPI architecture rely on the host processor to continuously provide complete frames of image data at a sufficient frame rate to avoid flicker or other visible artifacts.

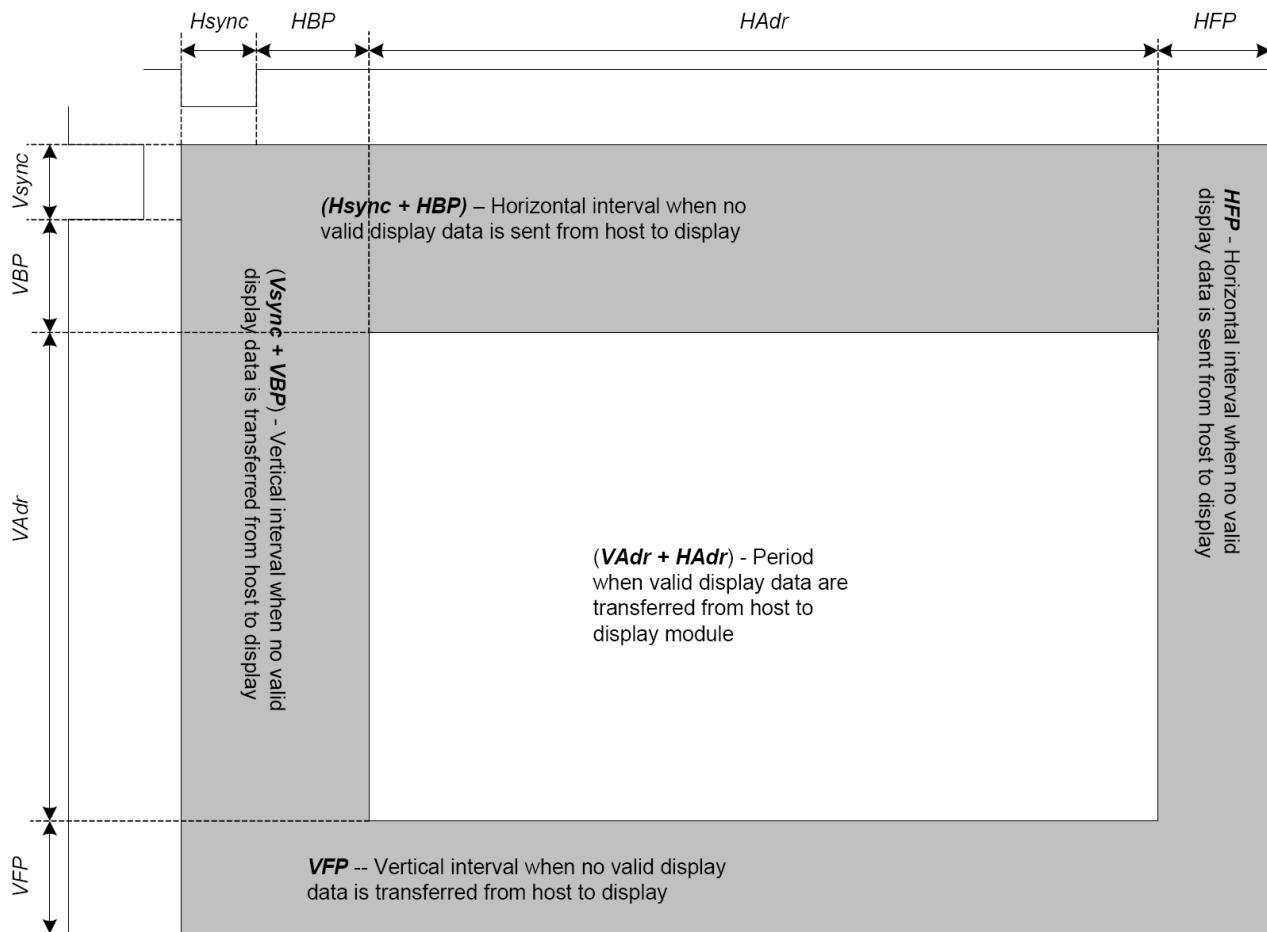
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The displayed image, or frame, is comprised of a rectangular array of pixels. The frame is transmitted from the host processor to a display module as a sequence of pixels, with each horizontal line of the image data sent as a group of consecutive pixels.

Vsync indicates the beginning of each frame of the displayed image. Hsync signals the beginning of each horizontal line of pixels.

Each pixel value (16 or 18-bit data) is transferred from the host processor to the display module during one pixel period. The rising edge of PCLK is used by the display module to capture pixel data. Since PCLK runs continuously, control signal DE is required to indicate when valid pixel data is being transmitted on the pixel data signals.





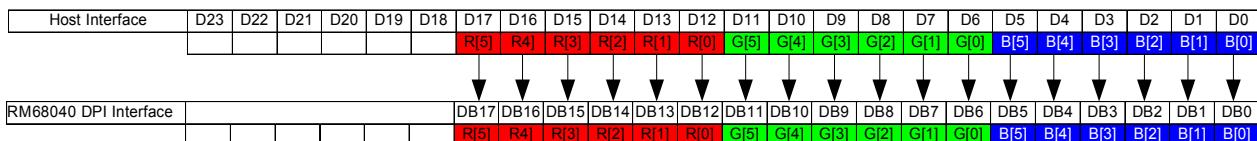
Parameters	Symbols	Condition	Min.	Typ.	Max.	Units	
PCLK	Cycle	PCLKCYC	-	88	-	ns	
Horizontal	Synchronization	Hsync	-	10	-	PCLK	
Horizontal	Back	Porch	HBP	-	20	-	PCLK
Horizontal	Address	HAdr	-	320	-	PCLK	
Horizontal	Front	Porch	HFP	-	40	-	PCLK
Vertical	Synchronization	Vsync	-	2	-	Line	
Vertical	Back	Porch	VBP	-	2	-	Line
Vertical	Address	VAdr	-	480	-	Line	
Vertical	Front	Porch	VFP	-	4	-	Line
Vsync	setup	time	VSST	-	Hz		
Vsync	hold	time	VSHT	-	Hz		
Hsync	setup	time	HSST	-	Hz		
Hsync	hold	time	HSHT	-	Hz		
Data	setup	time	DST	-	Hz		
Data	hold	time	DHT	-	Hz		
Vertical	Frequency(*)	60	-	Hz			
Horizontal	Frequency(*)	-	29.282	-	KHz		
PCLK	Frequency(*)	-	11.42Mhz	TBD	MHz		

Notes:

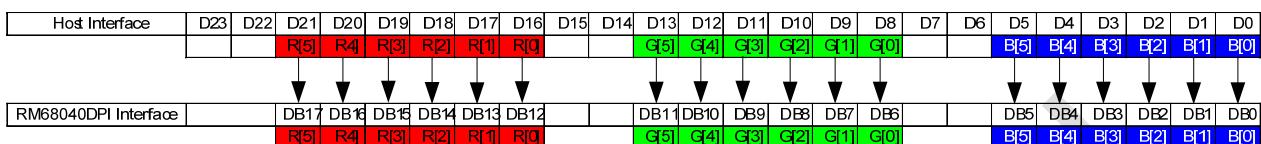
1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
3. Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

18bit DPI Interface Connection: set_pixel_format D[6:4]=3'h6 : 18bpp

Configuration 1

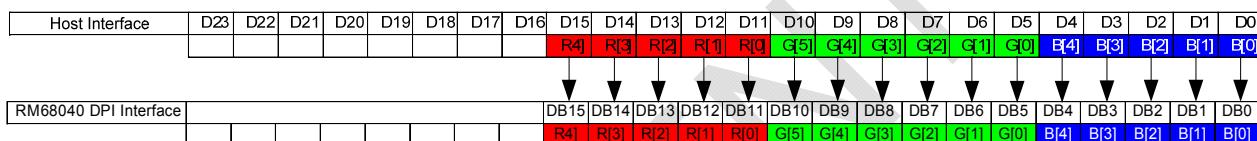


Configuration 2

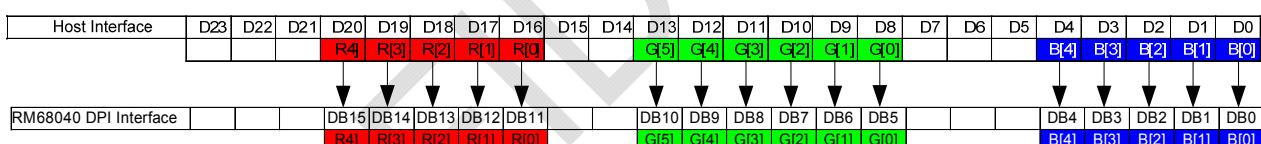


16bit DPI Interface Connection: set_pixel_format D[6:4]=3'h5 : 16bpp

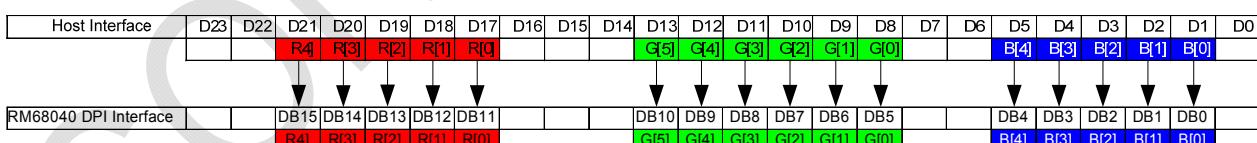
Configuration 1



Configuration 2



Configuration 3



16-bit data extend to 18-bit

Frame Memory Data (18bpp)																			
Set_pixel_format	EPF[1:0]	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
16bpp	2'h0	R[4]	R[3]	R[2]	R[1]	R[0]	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	0
	2'h1	R[4]	R[3]	R[2]	R[1]	R[0]	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	1
	2'h2	R[4]	R[3]	R[2]	R[1]	R[0]	RED	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	B[4]

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8. Command

8.1. Command List

Operational Code (Hex)	Command	Command(C) /Read(R) /Write(W)	Number Of Parameter	MIPI DCS Type1 Requirement	RM68041 Implementation
00h	nop	C	0	Yes	Yes
01h	soft_reset	C	0	Yes	Yes
06h	get_red_channel	R	1	No	No
07h	get_green_channel	R	1	No	No
08h	get_blue_channel	R	1	No	No
0Ah	get_power_mode	R	1	Yes	Yes
0Bh	get_address_mode	R	1	Yes (Bit[7:0])	Yes (Bit[7:3] , Only)
0Ch	get_pixel_format	R	1	Yes	Yes
0Dh	get_display_mode	R	1	Yes	Yes
0Eh	get_signal_mode	R	1	Yes	Yes
0Fh	get_diagnostic_result	R	1	Bit7/6 : Yes Bit5/4 : Optional	Yes (Bit7/6 Only)
10h	enter_sleep_mode	C	0	Yes	Yes
11h	exit_sleep_mode	C	0	Yes	Yes
12h	enter_partial_mode	C	0	Yes	Yes
13h	enter_normal_mode	C	0	Yes	Yes
20h	exit_invert_mode	C	0	Yes	Yes
21h	enter_invert_mode	C	0	Yes	Yes
26h	set_gamma_curve	W	1	Yes	No
28h	set_display_off	C	0	Yes	Yes
29h	set_display_on	C	0	Yes	Yes
2Ah	set_column_address	W	4	Yes	Yes
2Bh	set_page_address	W	4	Yes	Yes
2Ch	write_memory_start	W	Variable	Yes	Yes
2Dh	wite_LUT	W	Variable	Optional	No
2Eh	read_memory_start	R	Variable	Yes	Yes
30h	set_partial_area	W	4	Yes	Yes
33h	set_scroll_area	W	6	Yes	Yes
34h	set_tear_off	C	0	Yes	Yes
35h	set_tear_on	W	1	Yes	Yes
36h	set_address_mode	W	1	Yes (Bit7-0)	Yes (Bit[7:3], Bit[1:0] Only)
37h	set_scroll_start	W	2	Yes	Yes
38h	exit_idle_mode	C	0	Yes	Yes

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Operational Code (Hex)	Command	Command(C) /Read(R) /Write(W)	Number Of Parameter	MIPI DCS Type1 Requirement	RM68041 Implementation
39h	enter_idle_mode	C	0	Yes	Yes
3Ah	set_pixel_format	W	1	Yes	Yes
3Ch	write_memory_continue	W	Variable	Yes	Yes
3Eh	read_memory_continue	R	Variable	Yes	Yes
44h	set_tear_scanline	W	2	Yes	Yes
45h	get_scanline	R	2	Yes	Yes
A1h	read_DDB_start	R	5	Yes	Yes

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Operational Code (Hex)	Function	Command(C) Read(R)/Write(W)	Number Of Parameter
B0h	Command Access Protect	W/R	1
B1h	Low Power Mode Control	W/R	1
B3h	Frame Memory Access and Interface setting	W/R	5
B4h	Display Mode and Frame Memory Write Mode setting	W/R	1
BFh	Device code Read	R	4
C0h	Panel Driving Setting	W/R	7
C1h	Display Timing Setting for Normal Mode	W/R	3
C2h	Display Timing Setting for Partial Mode	W/R	3
C3h	Display Timing Setting for Idle Mode	W/R	3
C5h	Frame rate and Inversion Control	W/R	1
C6h	Interface Control	W/R	1
C8h	Gamma Setting	W	12
D0h	Power Setting	W/R	3
D1h	VCOM Control	W/R	3
D2h	Power Setting for Normal Mode	W/R	2
D3h	Power Setting for Partial Mode	W/R	2
D4h	Power Setting for Idle Mode	W/R	2
E0h	NV Memory Write	W/R	1
E1h	NV Memory Control	W/R	1
E2h	NV Memory Status	W/R	3
E3h	NV Memory Protection	W/R	2
B0~FF Except above command	LSI TEST Registers	W/R	Variable

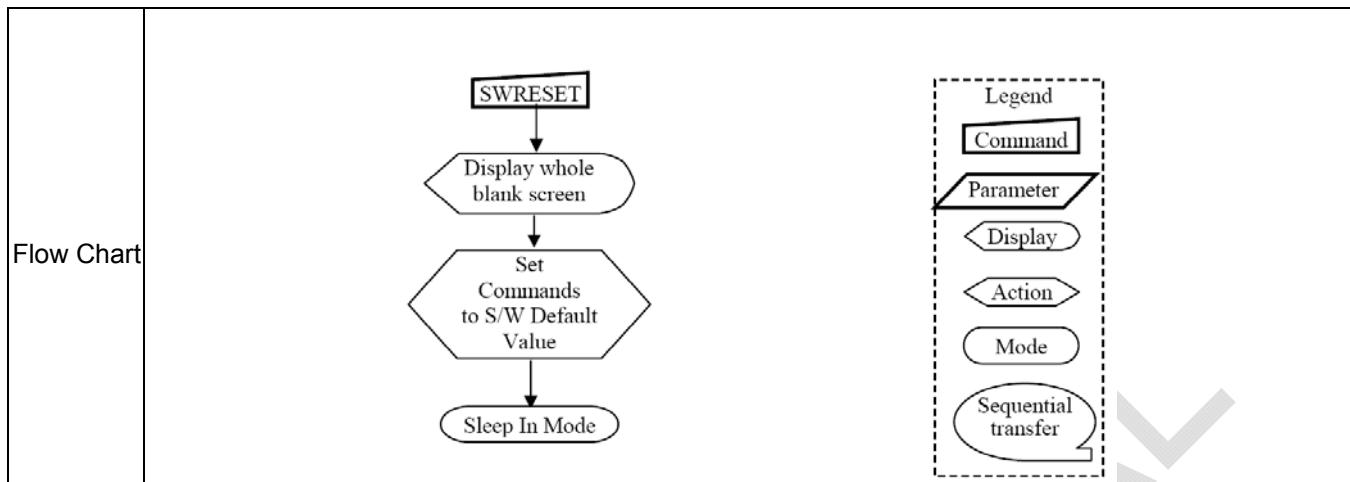
8.2. Command Description

8.2.1. NOP (00h)

NOP (No Operation)																										
00H	D/CX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	X	0	0	0	0	0	0	0	0	00													
Parameter	NO PARAMETER																									
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands. X = Don't care.																									
Restriction	None																									
Register Availability	<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																									
Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In	Yes																									
<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></tbody></table>														Status	Default Value	Power On Sequence	N/A	SW Reset	N/A	HW Reset	N/A					
Status	Default Value																									
Power On Sequence	N/A																									
SW Reset	N/A																									
HW Reset	N/A																									
Flow Chart	None																									

8.2.2. Soft_reset (01h)

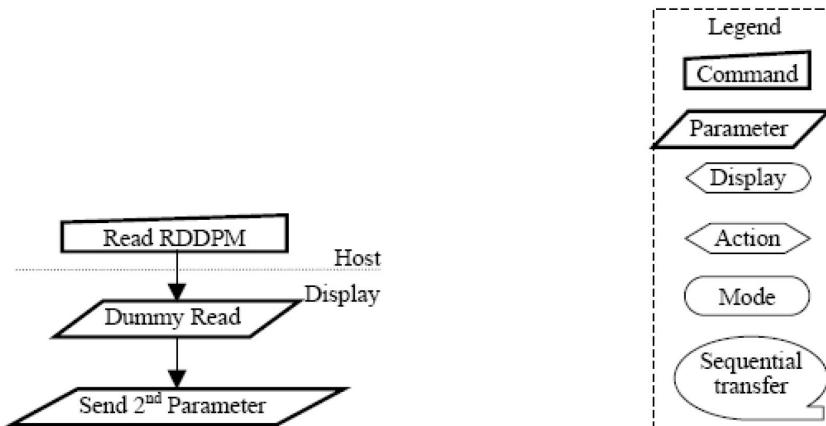
Soft_reset																									
01H	D/CX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	X	0	0	0	0	0	0	0	1	01												
Parameter	NO PARAMETER																								
Description	<p>When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)</p> <p>Note: The Frame Memory contents are affected by this command.</p> <p>X = Don't care</p>																								
Restriction	<p>Software Reset Command cannot be sent during Sleep Out sequence.</p> <p>Any new command is cannot be sent for 10-frame period until the RM68041 enters Sleep-In mode.</p> <p>Do not send any command.</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>SW Reset</td> <td>N/A</td> </tr> <tr> <td>HW Reset</td> <td>N/A</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	N/A	SW Reset	N/A	HW Reset	N/A				
Status	Default Value																								
Power On Sequence	N/A																								
SW Reset	N/A																								
HW Reset	N/A																								



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8.2.3. Get_power_mode (0Ah)

0AH		Get_power_mode																																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																												
Command	0	1	↑	x	0	0	0	0	1	0	1	0	0A																												
1st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x																												
2nd parameter	1	↑			D7	D6	D5	D4	D3	D2	D1	D0	xx																												
Description	<p>This command indicates the current status of the display as described in the table below:</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Comment</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>Not Defined</td> <td>Set to '0'</td> </tr> <tr> <td>D6</td> <td>Idle Mode On/Off</td> <td></td> </tr> <tr> <td>D5</td> <td>Partial Mode On/Off</td> <td></td> </tr> <tr> <td>D4</td> <td>Sleep In/Out</td> <td></td> </tr> <tr> <td>D3</td> <td>Display Normal Mode On/Off</td> <td></td> </tr> <tr> <td>D2</td> <td>Display On/Off</td> <td></td> </tr> <tr> <td>D1</td> <td>Not Defined</td> <td>Set to '0'</td> </tr> <tr> <td>D0</td> <td>Not Defined</td> <td>Set to '0'</td> </tr> </tbody> </table> <p>Bit D7 – Booster Voltage Status '0' = Booster Off or has a fault. '1' = Booster On and working OK (Meets Nokia's optical requirements).</p> <p>Bit D6 - Idle Mode On/Off '0' = Idle Mode Off. '1' = Idle Mode On.</p> <p>Bit D5 – Partial Mode On/Off '0' = Partial Mode Off. '1' = Partial Mode On.</p> <p>Bit D4 – Sleep In/Out '0' = Sleep In Mode. '1' = Sleep Out Mode.</p> <p>Bit D3 – Display Normal Mode On/Off '0' = Display Normal Mode Off. '1' = Display Normal Mode On.</p> <p>Bit D2 – Display On/Off '0' = Display is Off.</p>														Bit	Description	Comment	D7	Not Defined	Set to '0'	D6	Idle Mode On/Off		D5	Partial Mode On/Off		D4	Sleep In/Out		D3	Display Normal Mode On/Off		D2	Display On/Off		D1	Not Defined	Set to '0'	D0	Not Defined	Set to '0'
Bit	Description	Comment																																							
D7	Not Defined	Set to '0'																																							
D6	Idle Mode On/Off																																								
D5	Partial Mode On/Off																																								
D4	Sleep In/Out																																								
D3	Display Normal Mode On/Off																																								
D2	Display On/Off																																								
D1	Not Defined	Set to '0'																																							
D0	Not Defined	Set to '0'																																							

	<p>'1' = Display is On.</p> <p>Bit D1 – Not Defined 'This bit is not applicable for this project, so it is set to '0'</p> <p>Bit D0 – Not Defined 'This bit is not applicable for this project, so it is set to '0'</p> <p>X = Don't care</p>												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>08HEX</td></tr> <tr> <td>SW Reset</td><td>08HEX</td></tr> <tr> <td>HW Reset</td><td>08HEX</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	08HEX	SW Reset	08HEX	HW Reset	08HEX				
Status	Default Value												
Power On Sequence	08HEX												
SW Reset	08HEX												
HW Reset	08HEX												
Flow Chart	 <pre> graph TD A[Read RDDPM] --> B{Dummy Read} B --> C[Send 2nd Parameter] style A fill:#fff,stroke:#000 style B fill:#fff,stroke:#000 style C fill:#fff,stroke:#000 </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

8.2.4. Get_address_mode (0Bh)

0BH		Get_address_mode												
		D/CX	RDX	WRX	D17-0	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command		0	1	↑	x	0	0	0	0	1	0	1	1	0B
1st parameter		1	↑	1	x	x	x	x	x	x	x	x	x	xx
2nd parameter		1	↑	1	x	D7	D6	D5	D4	D3	0	0	0	xx
Description	This command indicates the current status of the display as described in the table below:													
	Bit	Description			Comment									
	D7	Page Address Order												
	D6	Column Address Order												
	D5	Page/Column Order												
	D4	Line Address Order												
	D3	RGB/BGR Order												
	D2	Reserved			Set to '0'									
	D1	Reserved			Set to '0'									
	D0	Reserved			Set to '0'									
Bit D7 – Page Address Order '0' = Top to Bottom '1' = Bottom to Top Bit D6 – Column Address Order '0' = Left to Right '1' = Right to Left Bit D5 - Page/Column Order '0' = Normal Mode '1' = Reverse Mode Note: For Bits D7 to D5, also refer to Section 8.2.3 MCU to memory write/read direction. Bit D4 – Line Address Order '0' = LCD Refresh Top to Bottom '1' = LCD Refresh Bottom to Top Bit D3 – RGB/BGR Order '0' = RGB														

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	'1' = BGR												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00HEX</td> </tr> <tr> <td>SW Reset</td> <td>No Change</td> </tr> <tr> <td>HW Reset</td> <td>00HEX</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00HEX	SW Reset	No Change	HW Reset	00HEX				
Status	Default Value												
Power On Sequence	00HEX												
SW Reset	No Change												
HW Reset	00HEX												
Flow Chart	<pre> graph TD A[Read RDDMADCTL] --> B{Dummy Read} B --> C[Send 2nd Parameter] style A fill:#fff,stroke:#000 style B fill:#fff,stroke:#000 style C fill:#fff,stroke:#000 style B fill:#fff,stroke:#000 style C fill:#fff,stroke:#000 </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

8.2.5. Get_pixel_format (0Ch)

0CH		Get_pixel_format																																																																																													
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																		
Command	0	1	↑	x	0	0	0	0	1	1	0	0	0C																																																																																		
1 st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x																																																																																		
2 nd parameter	1	↑	1	x	0	D6	D5	D4	0	D2	D1	D0	xx																																																																																		
Description	This command indicates the current status of the display as described in the table below: <table border="1"> <thead> <tr> <th>Bit</th><th colspan="8">Description</th></tr> </thead> <tbody> <tr> <td>D7</td><td colspan="8" style="text-align: center;">DPI Pixel Format(RGB Interface Color Format)</td></tr> <tr> <td>D6</td><td colspan="8" style="text-align: center;">DBI Pixel Format(Control Interface Color Format)</td></tr> <tr> <td>D5</td><td colspan="8" style="text-align: center;"></td></tr> <tr> <td>D4</td><td colspan="8" style="text-align: center;"></td></tr> <tr> <td>D3</td><td colspan="8" style="text-align: center;"></td></tr> <tr> <td>D2</td><td colspan="8" style="text-align: center;"></td></tr> <tr> <td>D1</td><td colspan="8" style="text-align: center;"></td></tr> <tr> <td>D0</td><td colspan="8" style="text-align: center;"></td></tr> </tbody> </table>														Bit	Description								D7	DPI Pixel Format(RGB Interface Color Format)								D6	DBI Pixel Format(Control Interface Color Format)								D5									D4									D3									D2									D1									D0								
Bit	Description																																																																																														
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	<table border="1"> <thead> <tr> <th>Pixel Format</th><th>D6/D2</th><th>D5/D1</th><th>D4/D0</th></tr> </thead> <tbody> <tr> <td>Reserved</td><td>0</td><td>0</td><td>0</td></tr> <tr> <td>3 bits / pixel</td><td>0</td><td>0</td><td>1</td></tr> <tr> <td>Reserved</td><td>0</td><td>1</td><td>0</td></tr> <tr> <td>Reserved</td><td>0</td><td>1</td><td>1</td></tr> <tr> <td>Reserved</td><td>1</td><td>0</td><td>0</td></tr> <tr> <td>16 bits / pixel</td><td>1</td><td>0</td><td>1</td></tr> <tr> <td>18 bits / pixel</td><td>1</td><td>1</td><td>0</td></tr> <tr> <td>Reserved</td><td>1</td><td>1</td><td>1</td></tr> </tbody> </table>														Pixel Format	D6/D2	D5/D1	D4/D0	Reserved	0	0	0	3 bits / pixel	0	0	1	Reserved	0	1	0	Reserved	0	1	1	Reserved	1	0	0	16 bits / pixel	1	0	1	18 bits / pixel	1	1	0	Reserved	1	1	1																																													
Pixel Format	D6/D2	D5/D1	D4/D0																																																																																												
Reserved	0	0	0																																																																																												
3 bits / pixel	0	0	1																																																																																												
Reserved	0	1	0																																																																																												
Reserved	0	1	1																																																																																												
Reserved	1	0	0																																																																																												
16 bits / pixel	1	0	1																																																																																												
18 bits / pixel	1	1	0																																																																																												
Reserved	1	1	1																																																																																												

	Status	Availability
Register Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

	Flow Chart	Legend
	<pre>graph TD; A[Read RDDCOLMOD] -- Host --> B{Dummy Read}; B -- Display --> C{Send 2nd Parameter}</pre> <p>The flowchart illustrates a sequence of operations. It begins with a rectangular box labeled "Read RDDCOLMOD" connected by a horizontal dotted line to a downward-pointing arrow. This arrow points to a diamond-shaped box labeled "Dummy Read". From "Dummy Read", another downward-pointing arrow leads to a second diamond-shaped box labeled "Send 2nd Parameter". To the right of the flowchart is a legend enclosed in a dashed box, defining symbols for Command (rectangle), Parameter (trapezoid), Display (diamond), Action (triangle), Mode (oval), and Sequential transfer (oval with a tail).</p>	<p>Legend</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer

8.2.6. Get_display_mode (0Dh)

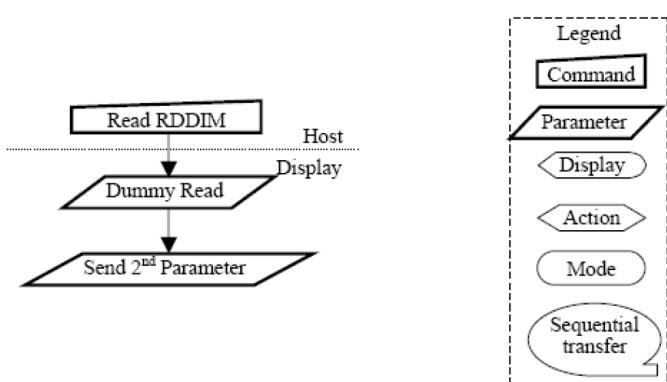
0DH		Get_display_mode																																																																		
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																							
Command	0	1	↑	x	0	0	0	0	1	1	0	1	0D																																																							
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x																																																							
2nd Parameter	1	↑	1	x	0	0	0	0	0	0	0	0	xx																																																							
Description	<p>The display module returns the display image mode status.</p> <table border="1"><thead><tr><th>Bit</th><th colspan="4">Description</th><th>Symbol</th></tr></thead><tbody><tr><td>D7</td><td colspan="4">Vertical Scrolling Status</td><td>VSSON</td></tr><tr><td>D6</td><td colspan="4">Reserved</td><td></td></tr><tr><td>D5</td><td colspan="4">Inversion On/Off</td><td>DSPINVON</td></tr><tr><td>D4</td><td colspan="4">Reserved</td><td></td></tr><tr><td>D3</td><td colspan="4">Reserved</td><td></td></tr><tr><td>D2</td><td colspan="4">Gamma Curve Selection</td><td></td></tr><tr><td>D1</td><td colspan="4">Gamma Curve Selection</td><td></td></tr><tr><td>D0</td><td colspan="4">Gamma Curve Selection</td><td></td></tr></tbody></table>														Bit	Description				Symbol	D7	Vertical Scrolling Status				VSSON	D6	Reserved					D5	Inversion On/Off				DSPINVON	D4	Reserved					D3	Reserved					D2	Gamma Curve Selection					D1	Gamma Curve Selection					D0	Gamma Curve Selection				
Bit	Description				Symbol																																																															
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D2	Gamma Curve Selection																																																																			
D1	Gamma Curve Selection																																																																			
D0	Gamma Curve Selection																																																																			
	<p>This command indicates the current status of the display as described in the table below:</p> <p>Bit D7 – Vertical Scrolling On/Off</p> <p>‘0’ = Vertical Scrolling is Off.</p> <p>‘1’ = Vertical Scrolling is On.</p> <p>Bit D6 – Reserved</p> <p>Bit D5 – Inversion On/Off</p> <p>‘0’ = Inversion is Off.</p> <p>‘1’ = Inversion is On.</p> <p>Bit D4 – Reserved</p> <p>Bit D3 – Reserved</p> <p>Bits D2, D1, D0 – Gamma Curve Selection</p> <p>These bits are not applicable for this project, so they are set to ‘000’</p>																																																																			

	Status	Availability
Register Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
	Flow Chart	Legend
	<pre>graph TD; A[Read RDDIM] --> B[Dummy Read]; B --> C[Send 2nd Parameter]</pre> <p>The flowchart illustrates a three-step process. Step 1: "Read RDDIM" (Host). Step 2: "Dummy Read" (Display). Step 3: "Send 2nd Parameter" (Display). Arrows indicate the sequential flow from the Host step to the Display steps.</p> <p>Legend:</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer	<p>Legend</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer

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8.2.7. Get_signal_mode (0Eh)

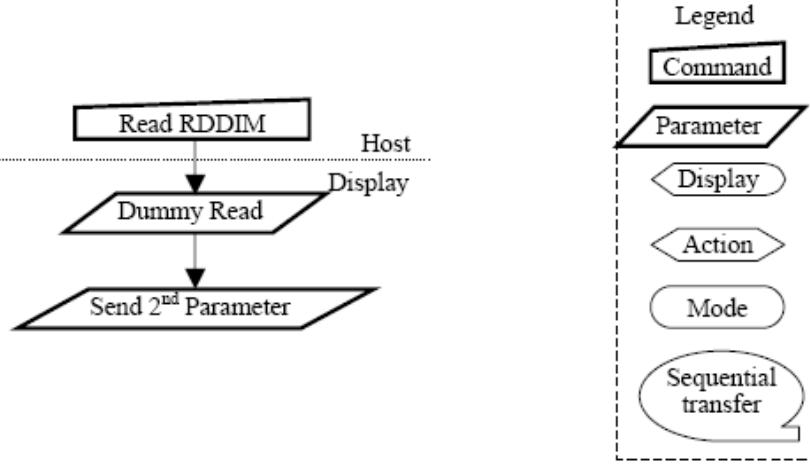
0EH	RDDSM (Read Display Signal Mode)																																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																											
Command	0	1	↑	x	0	0	0	0	1	1	1	0	0E																											
1 st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x																											
2 nd parameter	1	↑	1	x	D7	D6	0	0	0	0	0	0	xx																											
Description	<p>The display module returns the Display Signal Mode.</p> <table border="1"> <thead> <tr> <th>Bit</th><th>Description</th><th>Symbol</th></tr> </thead> <tbody> <tr> <td>D7</td><td>Tearing Effect Line On/Off</td><td>TEON</td></tr> <tr> <td>D6</td><td>Tearing Effect Line Output Mode</td><td>TELOM</td></tr> <tr> <td>D5</td><td>Reserved</td><td></td></tr> <tr> <td>D4</td><td>Reserved</td><td></td></tr> <tr> <td>D3</td><td>Reserved</td><td></td></tr> <tr> <td>D2</td><td>Reserved</td><td></td></tr> <tr> <td>D1</td><td>Reserved</td><td></td></tr> <tr> <td>D0</td><td>Reserved</td><td></td></tr> </tbody> </table> <p>This command indicates the current status of the display as described in the table below:</p> <p>Bit D7 – Tearing Effect Line On/Off</p> <p>‘0’ = Tearing Effect Line Off.</p> <p>‘1’ = Tearing Effect On.</p> <p>Bit D6 – Tearing Effect Line Output Mode, see section 8.3 for mode definitions.</p> <p>‘0’ = Mode 1.</p> <p>‘1’ = Mode 2.</p> <p>Bit D[5:0] – Reserved</p>													Bit	Description	Symbol	D7	Tearing Effect Line On/Off	TEON	D6	Tearing Effect Line Output Mode	TELOM	D5	Reserved		D4	Reserved		D3	Reserved		D2	Reserved		D1	Reserved		D0	Reserved	
Bit	Description	Symbol																																						
D7	Tearing Effect Line On/Off	TEON																																						
D6	Tearing Effect Line Output Mode	TELOM																																						
D5	Reserved																																							
D4	Reserved																																							
D3	Reserved																																							
D2	Reserved																																							
D1	Reserved																																							
D0	Reserved																																							

	<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Register Availability													
Flow Chart	 <pre>graph TD; A[Read RDDIM] --> B[Dummy Read]; B --> C[Send 2nd Parameter]</pre> <p>Legend:</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer												

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8.2.8. Get_diagnostic_result (0Fh)

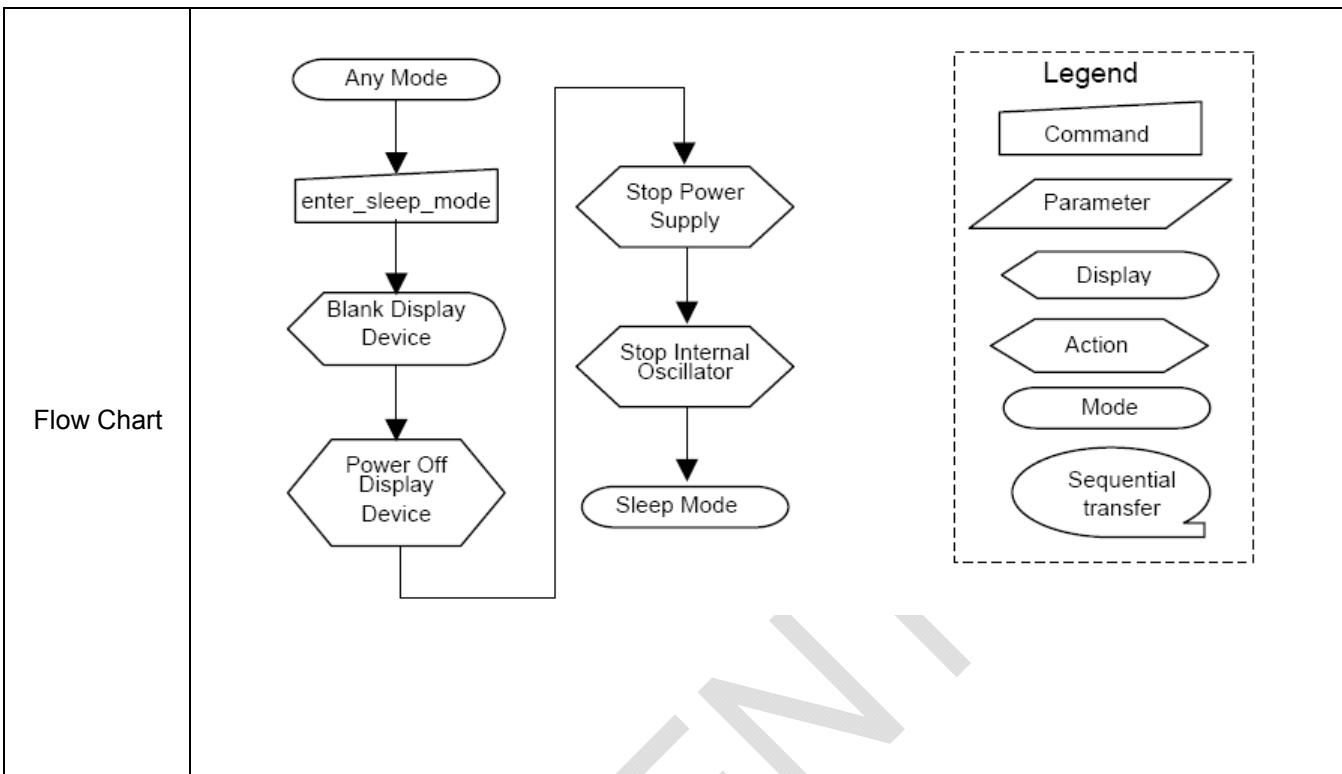
0FH		Get_diagnostic_result																										
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	0	1	↑	x	0	0	0	0	1	1	1	1	0F															
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x															
2nd Parameter	1	↑	1	x	D7	D6	0	0	0	0	0	0	xx															
Description	The display module returns the self-diagnostic results following a Sleep Out command.																											
Bit	Description								Symbol																			
D7	Register Loading Detection								SDR																			
D6	Functionality Detection								FUNCD																			
D5	Chip attachment Detection								Set '0'																			
D4	Display Glass Break Detection								Set '0'																			
D3	Reserved								Set '0'																			
D2	Reserved								Set '0'																			
D1	Reserved								Set '0'																			
D0	Reserved								Set '0'																			
Bit D7 – Register Loading Detection																												
Bit D6 – Functionality Detection																												
Bit D5 – Chip Attachment Detection																												
Set to '0' if feature unimplemented.																												
Bit D4 – Display Glass Break Detection																												
Set to '0' if feature unimplemented.																												
Bits D[3:0] – Reserved																												
Set to '0'.																												

	Status	Availability
Register Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Flow Chart		<p>Legend</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer

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8.2.9. Enter_sleep_mode (10h)

Enter_sleep_mode																									
10H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	0	1	0	0	0	0	10												
Parameter	No Parameter																								
Description	<p>This command causes the display module to enter the Sleep mode.</p> <p>This command causes the LCD module to enter the Sleep mode. In this mode, the DC/DC converter, internal oscillator and panel scanning stop. DBI or DSI Command Mode remains operational and the frame memory maintains its contents. The host processor continues to send PCLK, HS and VS information to Type 2 and Type 3 display modules for two frames after this command is sent when the display module is in Normal mode.</p>																								
Restriction	<p>This command has no effect when the display module is already in Sleep mode.</p> <p>The host processor must wait five milliseconds before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize. The host processor must wait 120 milliseconds after sending an exit_sleep_mode command before sending an enter_sleep_mode command.</p>																								
Register Availability	<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr><tr><td>SW Reset</td><td>Sleep In Mode</td></tr><tr><td>HW Reset</td><td>Sleep In Mode</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Sleep In Mode	SW Reset	Sleep In Mode	HW Reset	Sleep In Mode				
Status	Default Value																								
Power On Sequence	Sleep In Mode																								
SW Reset	Sleep In Mode																								
HW Reset	Sleep In Mode																								



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8.2.10. Exit_sleep_mode (11h)

Exit_sleep_mode																									
11H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	0	1	0	0	0	1	11												
Parameter	No Parameter																								
Description	This command causes the display module to exit Sleep mode. All blocks inside the display module are enabled. The host processor sends PCLK, HS and VS information to Type 2 and Type 3 display modules two frames before this command is sent when the display module is in Normal Mode.																								
Restriction	This command shall not cause any visible effect on the display device when the display module is not in Sleep mode. The host processor must wait five milliseconds after sending this command before sending another command. This delay allows the supply voltages and clock circuits to stabilize. The host processor must wait 120 milliseconds after sending an exit_sleep_mode command before sending an enter_sleep_mode command. The display module loads the display module's default values to the registers when exiting the Sleep mode. There shall not be any abnormal visual effect on the display device when loading the registers if the factory default and register values are the same or when the display module is not in Sleep mode. The display module runs the self-diagnostic functions after this command is received. See section 5.3 for a description of the self-diagnostic functions.																								
Register Availability	<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								

Default		<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Sleep In Mode</td></tr> <tr> <td>SW Reset</td><td>Sleep In Mode</td></tr> <tr> <td>HW Reset</td><td>Sleep In Mode</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	Sleep In Mode	SW Reset	Sleep In Mode	HW Reset	Sleep In Mode	
Status	Default Value										
Power On Sequence	Sleep In Mode										
SW Reset	Sleep In Mode										
HW Reset	Sleep In Mode										
<pre> graph TD Start((Sleep Mode)) --> ExitSleep[exit_sleep_mode] ExitSleep --> StartOsc[Start Internal Oscillator] StartOsc --> StartPower[Start Power Supply] StartPower --> PowerOn[Power On Display Device] PowerOn --> Blank[Blank Display Device] Blank --> Display[Display Memory contents] Display --> End((Sleep Mode Off)) </pre> <div style="border: 1px dashed black; padding: 5px; margin-top: 10px;"> Legend <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div>											

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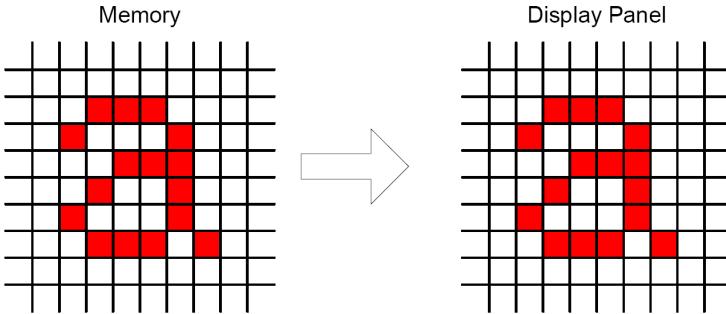
8.2.11. Enter_Partial_mode (12h)

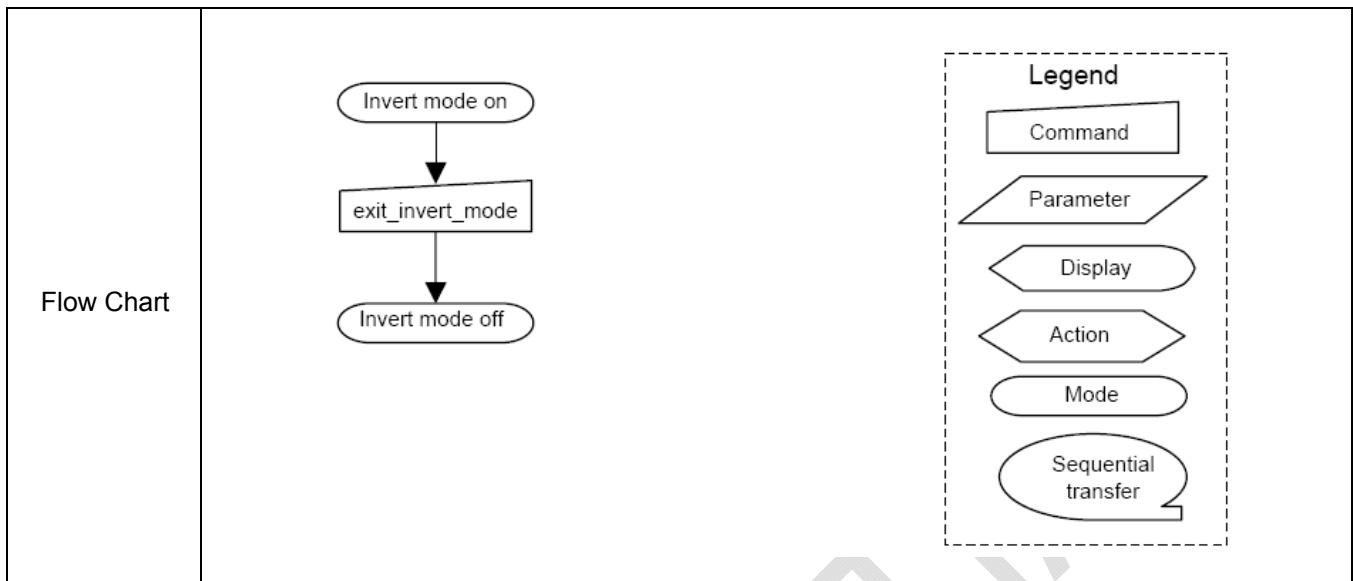
12H	Enter_Partial_mode																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	0	1	0	0	1	0	12												
Parameter	No Parameter																								
Description	<p>This command causes the display module to enter the Partial Display Mode. The Partial Display Mode window is described by the set_partial_area (30h) command.</p> <p>To leave Partial Display Mode, the enter_normal_mode (13h) command should be written. The host processor continues to send PCLK, HS and VS information to Type 2 display modules for two frames after this command is sent when the display module is in Normal Display Mode.</p>																								
Restriction	This command has no effect when Partial Display Mode is already active.																								
Register Availability	<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Normal display mode On</td></tr><tr><td>SW Reset</td><td>Normal display mode On</td></tr><tr><td>HW Reset</td><td>Normal display mode On</td></tr></tbody></table>													Status	Default Value	Power On Sequence	Normal display mode On	SW Reset	Normal display mode On	HW Reset	Normal display mode On				
Status	Default Value																								
Power On Sequence	Normal display mode On																								
SW Reset	Normal display mode On																								
HW Reset	Normal display mode On																								
Flow Chart	Refer to Partial Area (30h)																								

8.2.12. Enter_normal_mode (13h)

Enter_normal_mode																										
13H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	x	0	0	0	1	0	0	1	1	1	13												
Parameter	No Parameter																									
Description	<p>This command causes the display module to enter the Normal mode. Normal Mode is defined as Partial Display mode and Scroll mode are off.</p> <p>The host processor sends PCLK, HS and VS information to Type 2 display modules two frames before this command is sent when the display module is in Partial Display Mode.</p>																									
Restriction	This command has no effect when Normal Display mode is already active.																									
Register Availability	<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																									
Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In	Yes																									
Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Normal Display Mode On</td></tr><tr><td>SW Reset</td><td>Normal Display Mode On</td></tr><tr><td>HW Reset</td><td>Normal Display Mode On</td></tr></tbody></table>														Status	Default Value	Power On Sequence	Normal Display Mode On	SW Reset	Normal Display Mode On	HW Reset	Normal Display Mode On				
Status	Default Value																									
Power On Sequence	Normal Display Mode On																									
SW Reset	Normal Display Mode On																									
HW Reset	Normal Display Mode On																									
Flow Chart	Refer to the description of set_partial_area(30h) and set_scroll_area(33h)																									

8.2.13. Exit_invert_mode (20h)

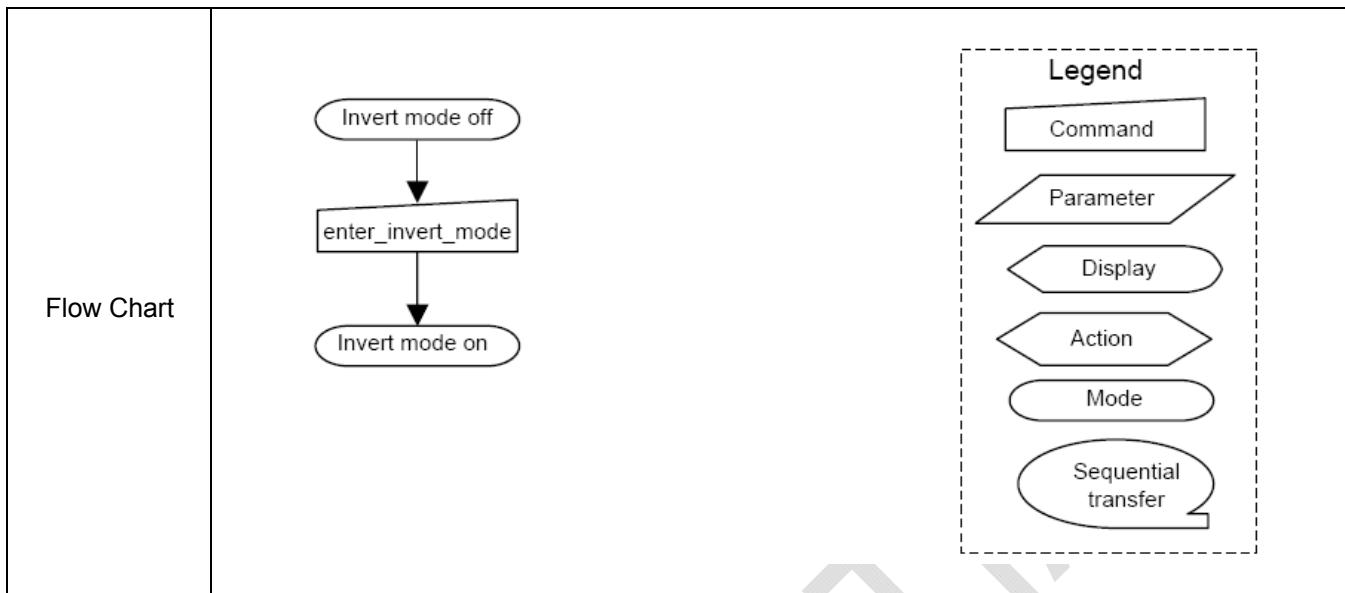
20H		Exit_invert_mode																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	x	0	0	1	0	0	0	0	0	20													
Parameter	No Parameter																									
Description	<p>This command causes the display module to stop inverting the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.</p> 																									
Restriction	This command has no effect when the display module is not inverting the display image.																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																									
Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In	Yes																									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Exit_invert_mode</td> </tr> <tr> <td>SW Reset</td> <td>Exit_invert_mode</td> </tr> <tr> <td>HW Reset</td> <td>Exit_invert_mode</td> </tr> </tbody> </table>														Status	Default Value	Power On Sequence	Exit_invert_mode	SW Reset	Exit_invert_mode	HW Reset	Exit_invert_mode				
Status	Default Value																									
Power On Sequence	Exit_invert_mode																									
SW Reset	Exit_invert_mode																									
HW Reset	Exit_invert_mode																									



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8.2.14. Enter_invert_mode (21h)

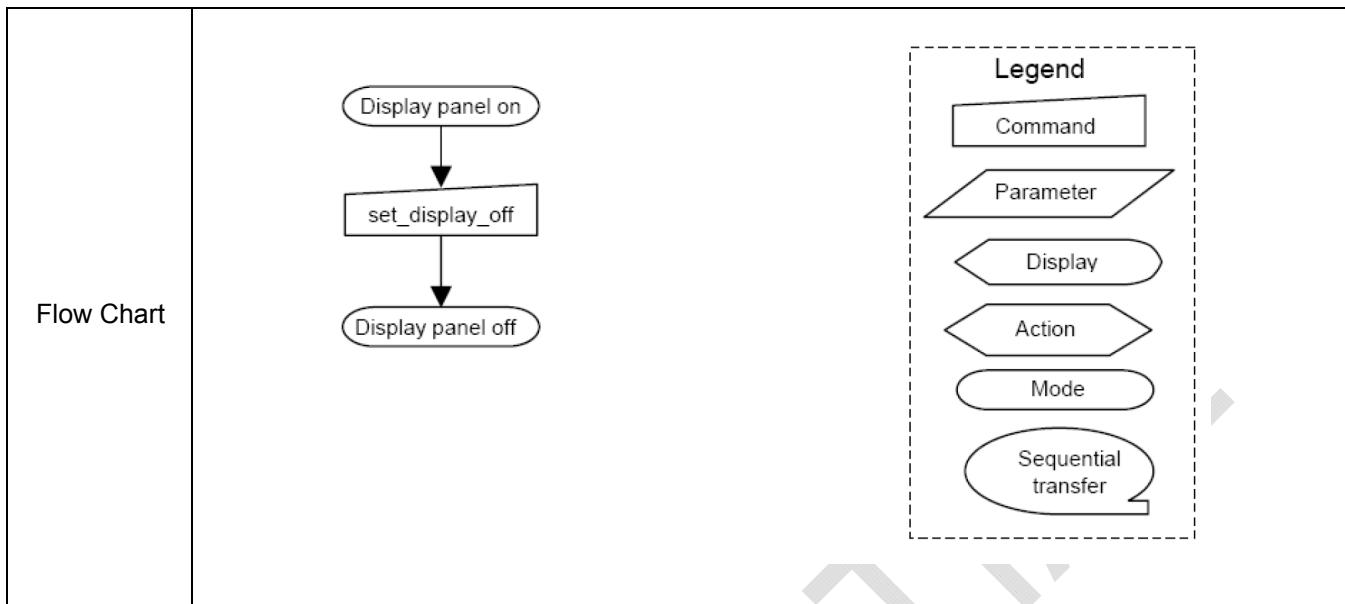
21H		Enter_invert_mode																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	0	0	0	0	1	21												
Parameter	No Parameter																								
Description	This command causes the display module to invert the image data only on the display device. The frame memory contents remain unchanged. No status bits are changed.																								
Restriction	This command has no effect when module is already in inversion on mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
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Sleep In	Yes																								
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Status	Default Value																								
Power On Sequence	Exit_invert_mode																								
SW Reset	Exit_invert_mode																								
HW Reset	Exit_invert_mode																								



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8.2.15. Set_display_off (28h)

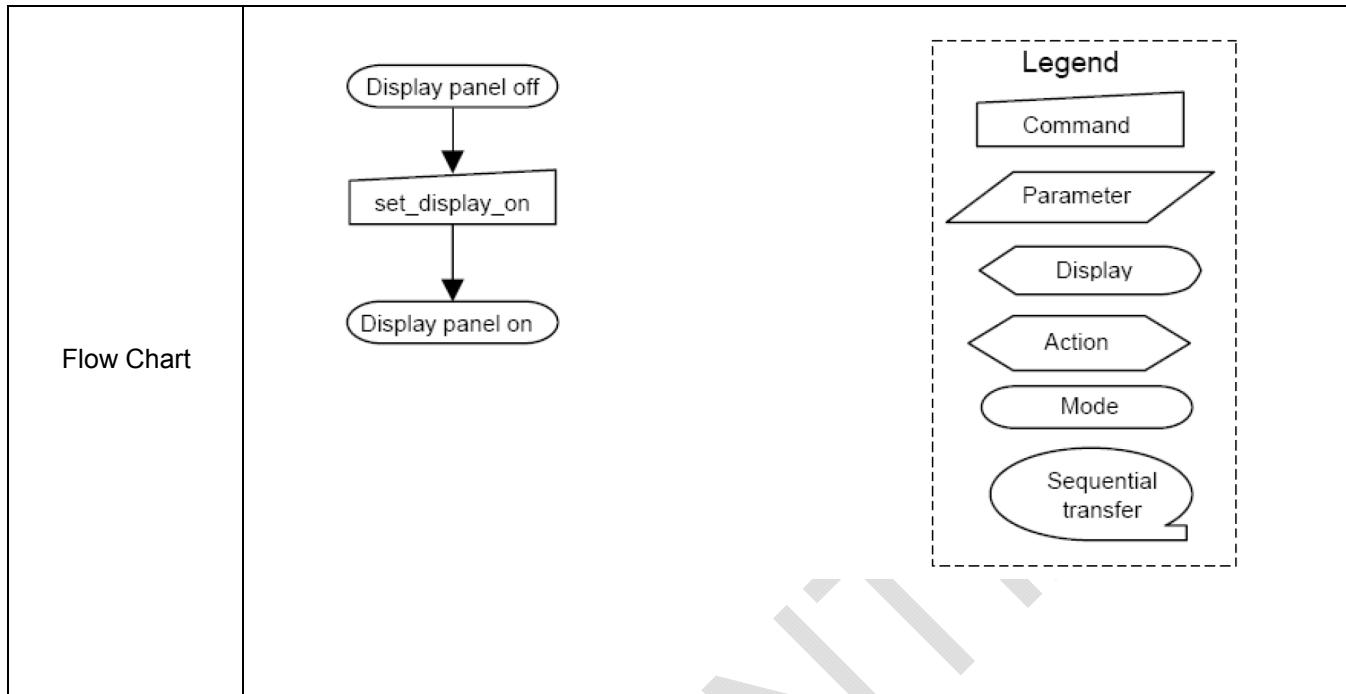
28H		Set_display_off																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	0	1	0	0	0	28												
Parameter	No Parameter																								
Description	<p>This command causes the display module to stop displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.</p>																								
Restriction	This command has no effect when module is already in display off mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Off</td> </tr> <tr> <td>SW Reset</td> <td>Display Off</td> </tr> <tr> <td>HW Reset</td> <td>Display Off</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Display Off	SW Reset	Display Off	HW Reset	Display Off				
Status	Default Value																								
Power On Sequence	Display Off																								
SW Reset	Display Off																								
HW Reset	Display Off																								



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8.2.16. Set_display_on (29h)

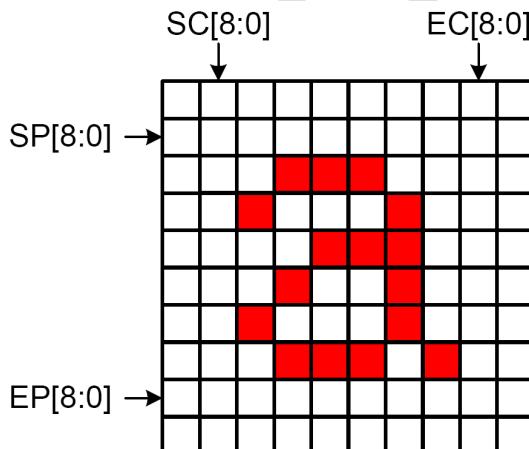
29H		Set_display_on																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	0	1	0	0	1	29												
Parameter	No Parameter																								
Description	This command causes the display module to start displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.																								
Restriction	This command has no effect when module is already in display on mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Off</td> </tr> <tr> <td>SW Reset</td> <td>Display Off</td> </tr> <tr> <td>HW Reset</td> <td>Display Off</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Display Off	SW Reset	Display Off	HW Reset	Display Off				
Status	Default Value																								
Power On Sequence	Display Off																								
SW Reset	Display Off																								
HW Reset	Display Off																								



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8.2.14. Set_column_address (2Ah)

2AH		Set_column_address																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	x	0	0	1	0	1	0	1	0	2A													
1 st parameter	1	1	↑	x	0	0	0	0	0	0	0	SC8	Note1													
2 nd parameter	1	1	↑	x	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0														
3 rd parameter	1	1	↑	x	0	0	0	0	0	0	0	EC8	Note 2													
4 th parameter	1	1	↑	x	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0														
Description	This command defines the column extent of the frame memory accessed by the host processor with the read_memory_continue and write_memory_continue commands. No status bits are changed.																									
Restriction	SC [8:0] always must be equal to or less than EC[8:0]. If SC[8:0] or EC[8:0] is greater than the available frame memory, the parameter is not updated.																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																									
Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In	Yes																									



	Status	Default Value
Default	Power On Sequence	SC[8:0]=0000HEX SE[8:0]=013FHEX
	SW Reset	SC[8:0]=0000HEX If Set_address_mode(36h) B5=0 : EC[8:0]=013FHEX If Set_address_mode(36h) B5=1 : EC[8:0]=01DFHEX
	HW Reset	SC[8:0]=000HEX SE[8:0]=013FHEX
Flow chart	<pre> graph TD A[set_column_address] --> B{1st&2nd parameter SC[8:0] 3rd&4th parameter EC[8:0]} B --> C[set_page_address] C --> D{1st&2nd parameter SP[8:0] 3rd&4th parameter EP[8:0]} D --> E[Write_memory_start] E --> F((Image Data D1[8:0], D2[8:0], Dn[8:0])) F --> G[Next Command] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 	As required

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8.2.15. Set_page_address (2Bh)

2BH		Set_page_address																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	x	0	0	1	0	1	0	1	1	2B													
1 st parameter	1	1	↑	x	0	0	0	0	0	0	0	SP8	xxx													
2 nd parameter	1	1	↑	x	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0														
3 rd parameter	1	1	↑	x	0	0	0	0	0	0	0	EP8	xxx													
4 th parameter	1	1	↑	x	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0														
Description	This command defines the page extent of the frame memory accessed by the host processor with the write_memory_continue and read_memory_continue command. No status bits are changed.																									
Restriction	SP [8:0] always must be equal to or less than EP [8:0]. If SP[8:0] or EP[8:0] is greater than the available frame memory then the parameter is not updated.																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																									
Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In	Yes																									

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	Status	Default Value	
Default	Power On Sequence	SP[8:0]=0000HEX	EP[8:0]=01DFHEX
	SW Reset	SP[8:0]=0000HEX	If Set_address_mode(36h) B5=0 : EP[8:0]=01DFHEX If Set_address_mode(36h) B5=1 : EP[8:0]=013FHEX
	HW Reset	SP[8:0]=0000HEX	EP[8:0]=01DFHEX

Flow chart	<pre> graph TD A[set_column_address] --> B{1st&2nd parameter SC[8:0] 3rd&4th parameter EC[8:0]} B --> C[set_page_address] C --> D{1st&2nd parameter SP[8:0] 3rd&4th parameter EP[8:0]} D --> E[Write_memory_start] E --> F((Image Data D1[8:0], D2[8:0] ..., Dn[8:0])) F --> G[Next Command] </pre>	
	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 	

8.2.19. Write_memory_start (2Ch)

2CH		Write_memory_start												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	xx	0	0	1	0	1	1	0	0	2C	
1 st pixel data	1	1	↑	D1[17..8]	D17	D16	D15	D14	D13	D12	D11	D10	00000..3FFF	
:	1	1	↑	Dx[17..8]	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00000..3FFF	
N th pixel data	1	1	↑	Dn[17..8]	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00000..3FFF	
Description	<p>This command transfers image data from the host processor to the display module's frame memory starting at the pixel location specified by preceding set_column_address (2Ah) and set_page_address (2Bh) commands.</p> <p>If set_address_mode (36h) B5 = 0:</p> <p>The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds $(EC - SC + 1) * (EP - SP + 1)$ the extra pixels are ignored.</p> <p>If set_address_mode (36h) B5 = 1:</p> <p>The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds $(EC - SC + 1) * (EP - SP + 1)$ the extra pixels are ignored.</p>													
Restriction	<p>A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write location. Otherwise, data written with write_memory_start and any following write_memory_continue commands is written to undefined locations.</p>													

Register Availability		<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default		Status	Default Value										
		Power On Sequence	Contents of memory is set randomly										
		SW Reset	Contents of memory is not cleared										
		HW Reset	Contents of memory is not cleared										
Flow chart		<pre> graph TD A[Write_memory_start] --> B{Image Data D1[17:0], D2[17:0] ..., Dn[17:0]} B --> C[Next Command] </pre>	Legend <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 										

8.2.20. Read_memory_start (2Eh)

2EH		RAMRD (Memory Read)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	x	0	0	1	0	1	1	1	0	2E	
1 st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x	
2 nd parameter	1	↑	1	D1[17..8] 1	D17	D16	D15	D14	D13	D12	D11	D10	00000..3FF	
:	1	↑	1	Dx[17..8] 1	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00000..3FF	
(N+1)th parameter	1	↑	1	Dn[17..8] 1	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00000..3FF	
Description	<p>This command transfers image data from the display module's frame memory to the host processor starting at the pixel location specified by preceding set_column_address and set_page_address commands.</p> <p>If set_address_mode B5 = 0:</p> <p>The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.</p> <p>If set_address_mode B5 = 1:</p> <p>The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.</p>													
Restriction	Regardless of the color mode set in set_pixel_format, the pixel format returned by read_memory_start is always 18-bit so there is no restriction on the length of data.													

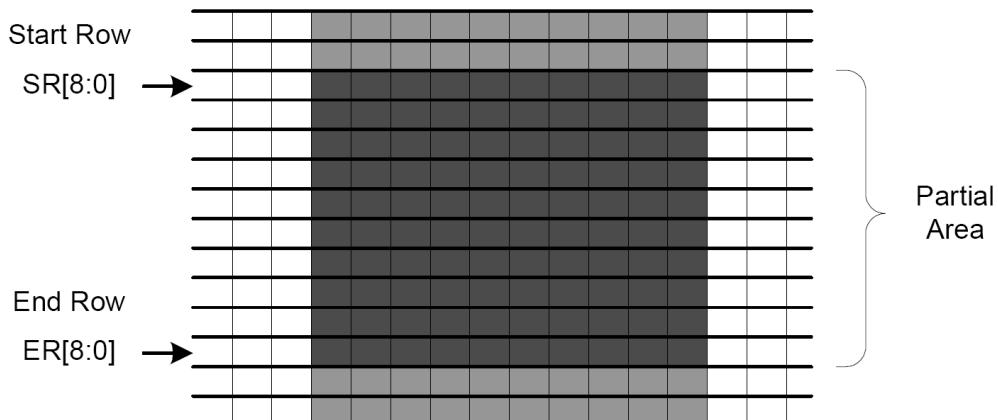
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes
Status	Availability											
Normal Mode On, Idle Mode Off, Sleep Out	Yes											
Normal Mode On, Idle Mode On, Sleep Out	Yes											
Partial Mode On, Idle Mode Off, Sleep Out	Yes											
Partial Mode On, Idle Mode On, Sleep Out	Yes											
<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr> <tr> <td>SW Reset</td><td>Contents of memory is not cleared</td></tr> <tr> <td>HW Reset</td><td>Contents of memory is not cleared</td></tr> </tbody> </table>		Status	Default Value	Power On Sequence	Contents of memory is set randomly	SW Reset	Contents of memory is not cleared	HW Reset	Contents of memory is not cleared			
Status	Default Value											
Power On Sequence	Contents of memory is set randomly											
SW Reset	Contents of memory is not cleared											
HW Reset	Contents of memory is not cleared											
<pre> graph TD A[Read_memory_start] --> B{Dummy Read} B --> C((Image Data D1[17:0], D2[17:0], Dn[17:0])) C --> D[Next Command] </pre>												
<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

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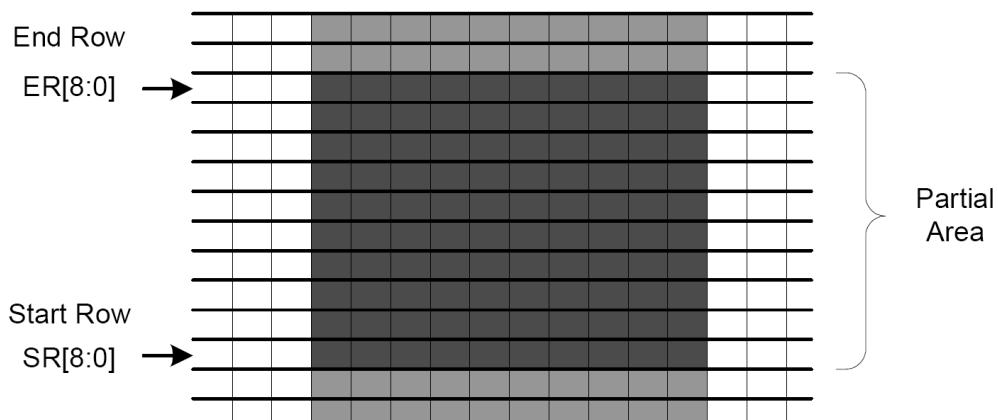
8.2.21. Set_partial_area (30h)

30H	Set_partial_area													
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	x	0	0	1	1	0	0	0	0	30	
1 st parameter	1	1	↑	x	0	0	0	0	0	0	0	SR8	000..1DFh	
2 nd parameter	1	1	↑	x	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0		
3 rd parameter	1	1	↑	x	0	0	0	0	0	0	0	ER8	000..1DFh	
4 th parameter	1	1	↑	x	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0		
Description	This command defines the Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the following figure. SR and ER refer to the Frame Memory													

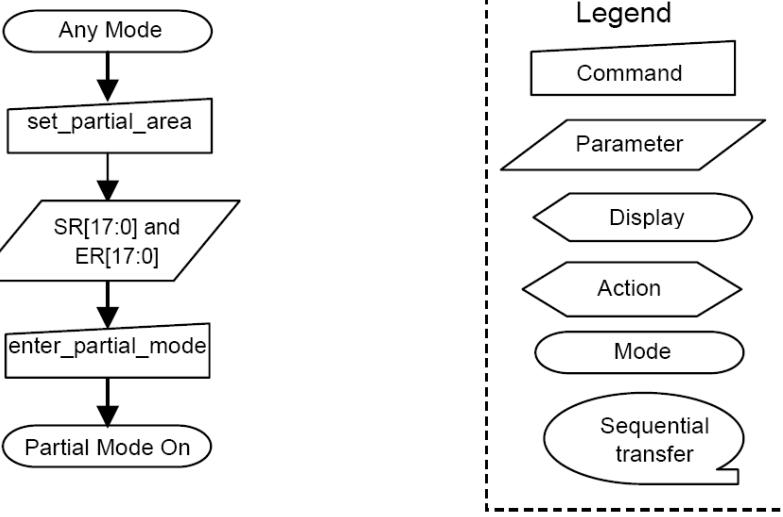
If End Row > Start Row and set_address_mode B4 = 0:

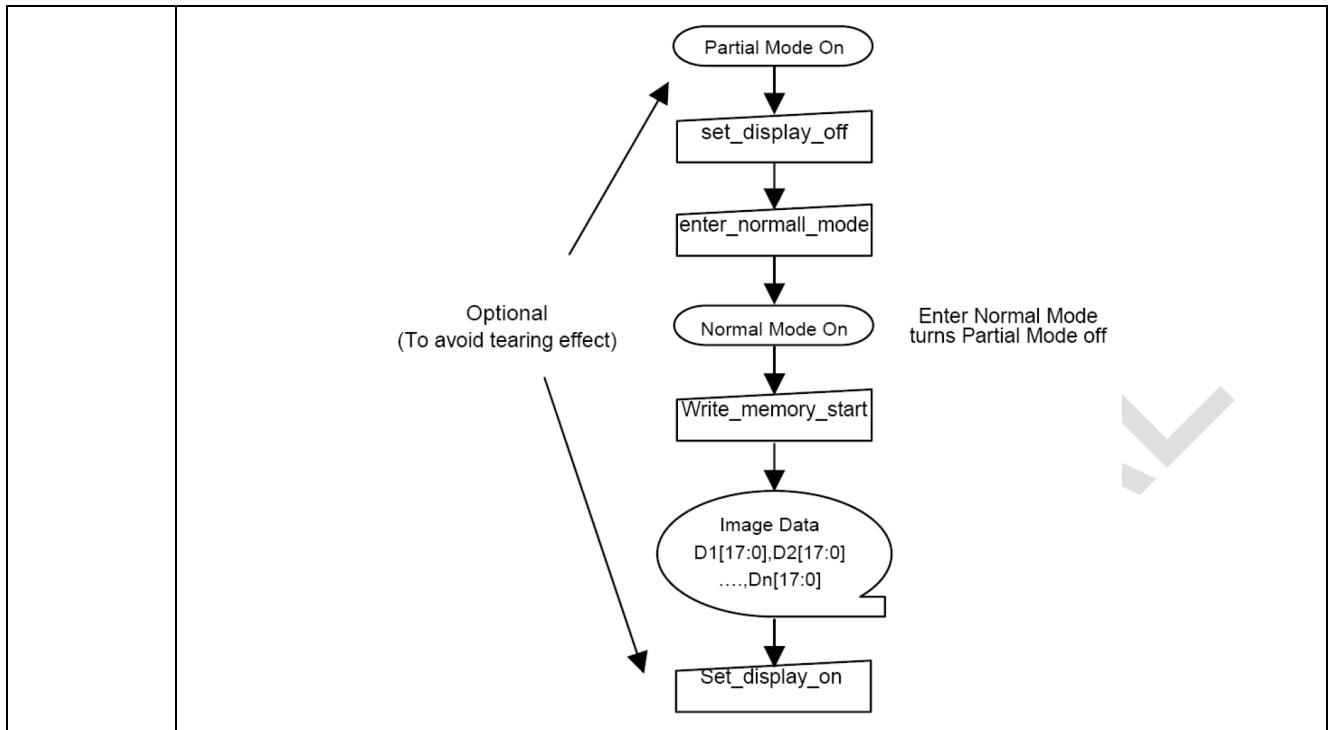


If End Row > Start Row and set_address_mode B4 = 1:



	<p>End Row < Start Row (set_address_mode(36h) B4=0)</p> <p>ER[8:0]</p> <p>SR[8:0]</p> <p>Partial Area</p> <p>Partial Area</p>
	<p>End Row < Start Row (set_address_mode(36h) B4=1)</p> <p>Start Row</p> <p>SR[8:0]</p> <p>End Row</p> <p>ER[8:0]</p> <p>Partial Area</p> <p>Partial Area</p>
Restriction	SR[15:0] and ER[15:0] cannot be 0000h nor exceed the last vertical line number (01DFh).

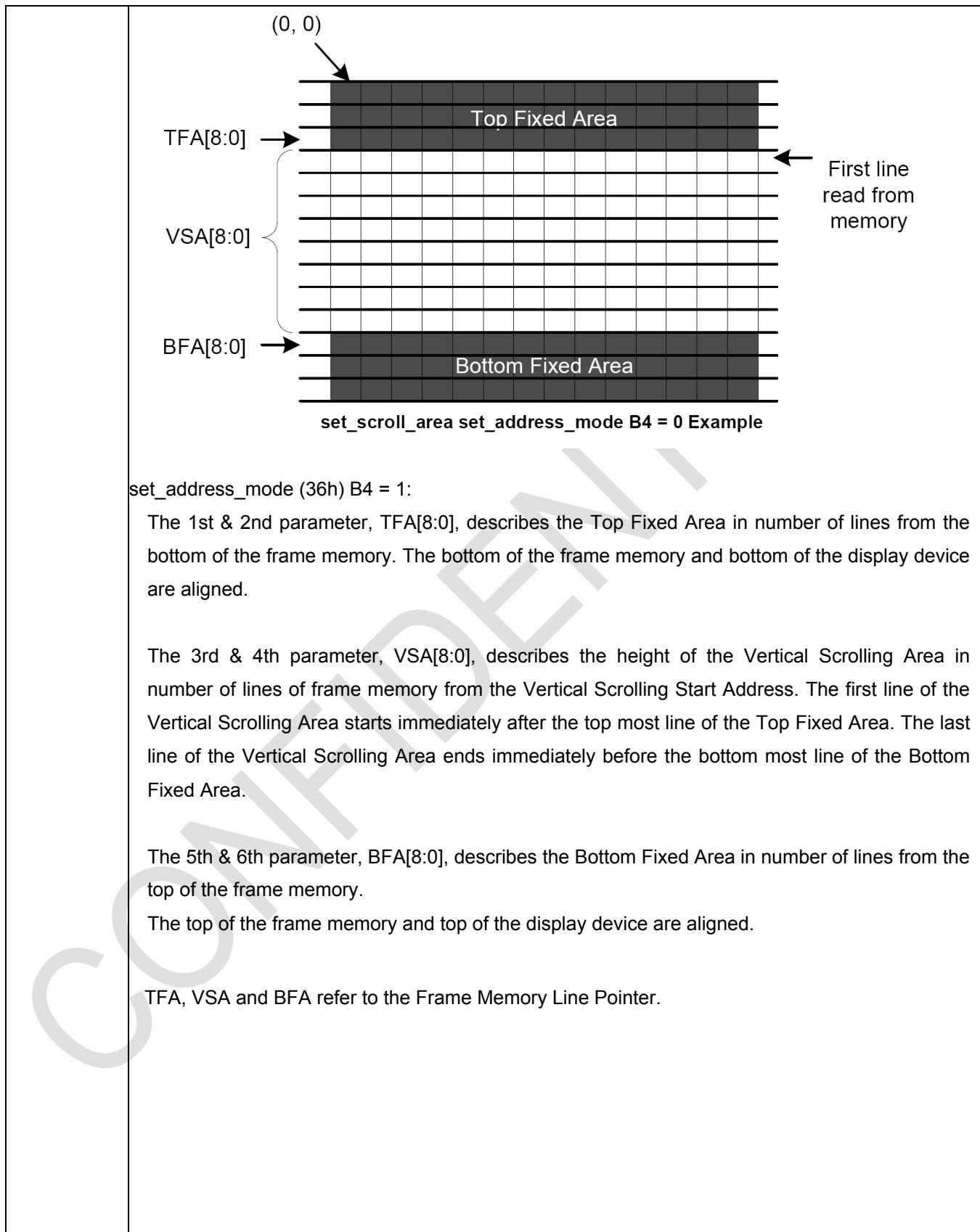
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes
Status	Availability											
Normal Mode On, Idle Mode Off, Sleep Out	Yes											
Normal Mode On, Idle Mode On, Sleep Out	Yes											
Partial Mode On, Idle Mode Off, Sleep Out	Yes											
Partial Mode On, Idle Mode On, Sleep Out	Yes											
<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>SR[8:0]=0000HEX ER[8:0]=01DFHEX</td></tr> <tr> <td>SW Reset</td><td>SR[8:0]=0000HEX ER[8:0]=01DFHEX</td></tr> <tr> <td>HW Reset</td><td>SR[8:0]=0000HEX ER[8:0]=01DFHEX</td></tr> </tbody> </table>		Status	Default Value	Power On Sequence	SR[8:0]=0000HEX ER[8:0]=01DFHEX	SW Reset	SR[8:0]=0000HEX ER[8:0]=01DFHEX	HW Reset	SR[8:0]=0000HEX ER[8:0]=01DFHEX			
Status	Default Value											
Power On Sequence	SR[8:0]=0000HEX ER[8:0]=01DFHEX											
SW Reset	SR[8:0]=0000HEX ER[8:0]=01DFHEX											
HW Reset	SR[8:0]=0000HEX ER[8:0]=01DFHEX											
<p>1. To Enter Partial Mode</p>  <pre> graph TD AnyMode([Any Mode]) --> SetPartialArea[set_partial_area] SetPartialArea --> SR17_0{SR[17:0] and ER[17:0]} SR17_0 -- True --> EnterPartialMode[enter_partial_mode] EnterPartialMode --> PartialModeOn([Partial Mode On]) SR17_0 -- False --> SetPartialArea </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												
<p>2. To Leave Partial Mode</p>												

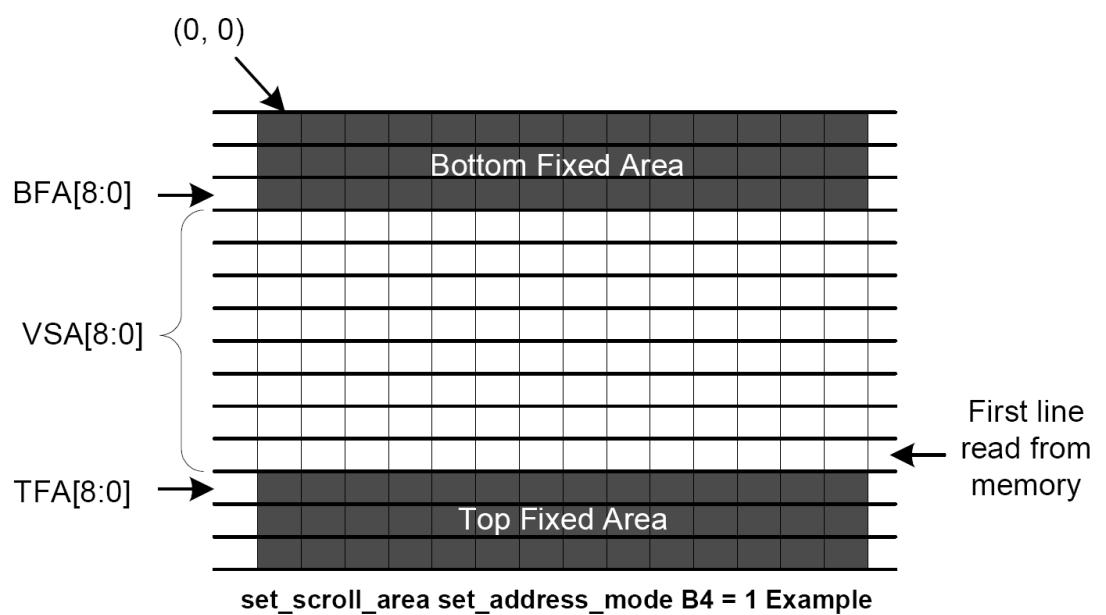


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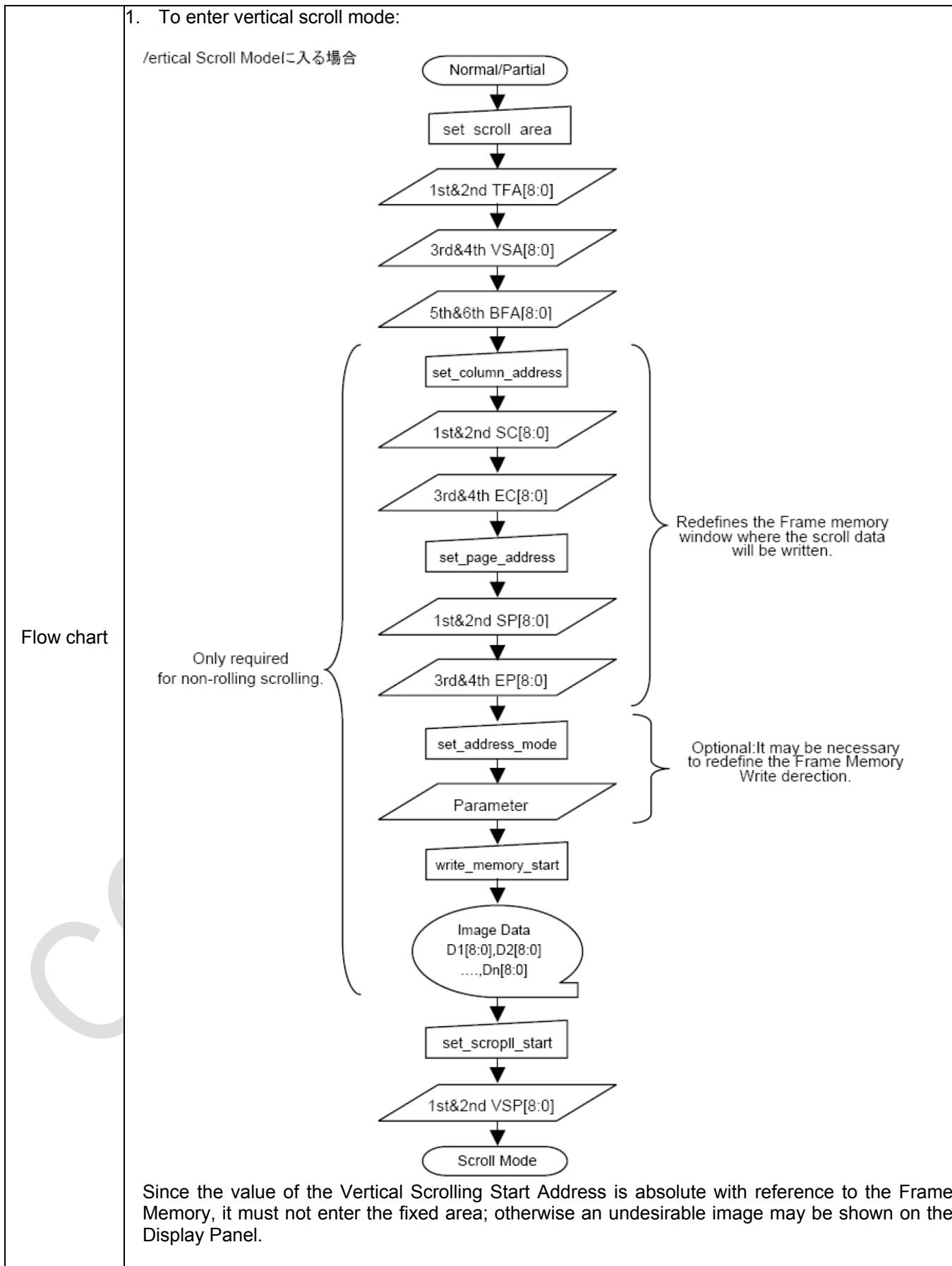
8.2.22. Set_scroll_area (33h)

33H	Set_scroll_area													
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	x	0	0	1	1	0	0	1	1	33	
1 st parameter	1	1	↑	x	0	0	0	0	0	0	0	TFA[8]	0000 ... 01E0	
2 nd parameter	1	1	↑	x	TFA[7]	TFA[6]	TFA[5]	TFA[4]	TFA[3]	TFA[2]	TFA[1]	TFA[0]		
3 rd parameter	1	1	↑	x	0	0	0	0	0	0	0	VSA[8]	0000 ... 01E0	
4 th parameter	1	1	↑	x	VSA[7]	VSA[6]	VSA[5]	VSA[4]	VSA[3]	VSA[2]	VSA[1]	VSA[0]		
5 th parameter	1	1	↑	x	0	0	0	0	0	0	0	BFA[8]	0000 ... 01E0	
6 th parameter	1	1	↑	x	BFA[7]	BFA[6]	BFA[5]	BFA[4]	BFA[3]	BFA[2]	BFA[1]	BFA[0]		
Description	<p>This command defines the display vertical scrolling area.</p> <p>set_address_mode (36h) B4 = 0:</p> <p>The 1st & 2nd parameter, TFA[8:0], describes the Top Fixed Area in number of lines from the top of the frame memory. The top of the frame memory and top of the display device are aligned. The 3rd & 4th parameter, VSA[8:0], describes the height of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the bottom most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the top most line of the Bottom Fixed Area.</p> <p>The 5th & 6th parameter, BFA[8:0], describes the Bottom Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned.</p> <p>TFA, VSA and BFA refer to the Frame Memory Line Pointer.</p>													



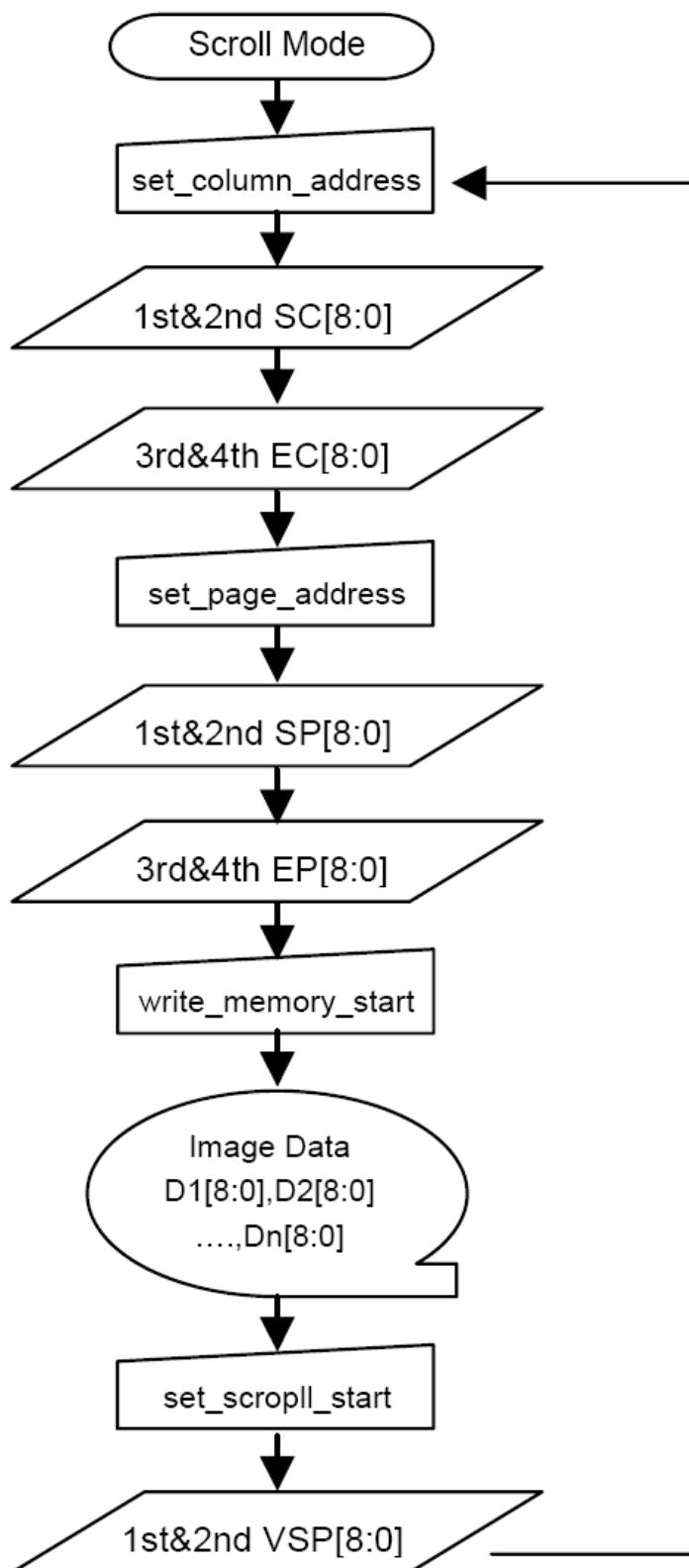


Restriction	The sum of TFA, VSA and BFA must equal the number of the display device's horizontal lines (pages), otherwise Scrolling mode is undefined. In Vertical Scroll Mode, set_address_mode B5 should be set to '0' – this only affects the Frame Memory Write.																		
Register Availability	<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>			Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes				
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Partial Mode On, Idle Mode Off, Sleep Out	Yes																		
Partial Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"><thead><tr><th>Status</th><th colspan="3">Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>TFA[8:0]=0000HEX</td><td>VSA[8:0]=01E0HEX</td><td>BFA[8:0]=0000HEX</td></tr><tr><td>SW Reset</td><td>TFA[8:0]=0000HEX</td><td>VSA[8:0]=01E0HEX</td><td>BFA[8:0]=0000HEX</td></tr><tr><td>HW Reset</td><td>TFA[8:0]=0000HEX</td><td>VSA[8:0]=01E0HEX</td><td>BFA[8:0]=0000HEX</td></tr></tbody></table>			Status	Default Value			Power On Sequence	TFA[8:0]=0000HEX	VSA[8:0]=01E0HEX	BFA[8:0]=0000HEX	SW Reset	TFA[8:0]=0000HEX	VSA[8:0]=01E0HEX	BFA[8:0]=0000HEX	HW Reset	TFA[8:0]=0000HEX	VSA[8:0]=01E0HEX	BFA[8:0]=0000HEX
Status	Default Value																		
Power On Sequence	TFA[8:0]=0000HEX	VSA[8:0]=01E0HEX	BFA[8:0]=0000HEX																
SW Reset	TFA[8:0]=0000HEX	VSA[8:0]=01E0HEX	BFA[8:0]=0000HEX																
HW Reset	TFA[8:0]=0000HEX	VSA[8:0]=01E0HEX	BFA[8:0]=0000HEX																

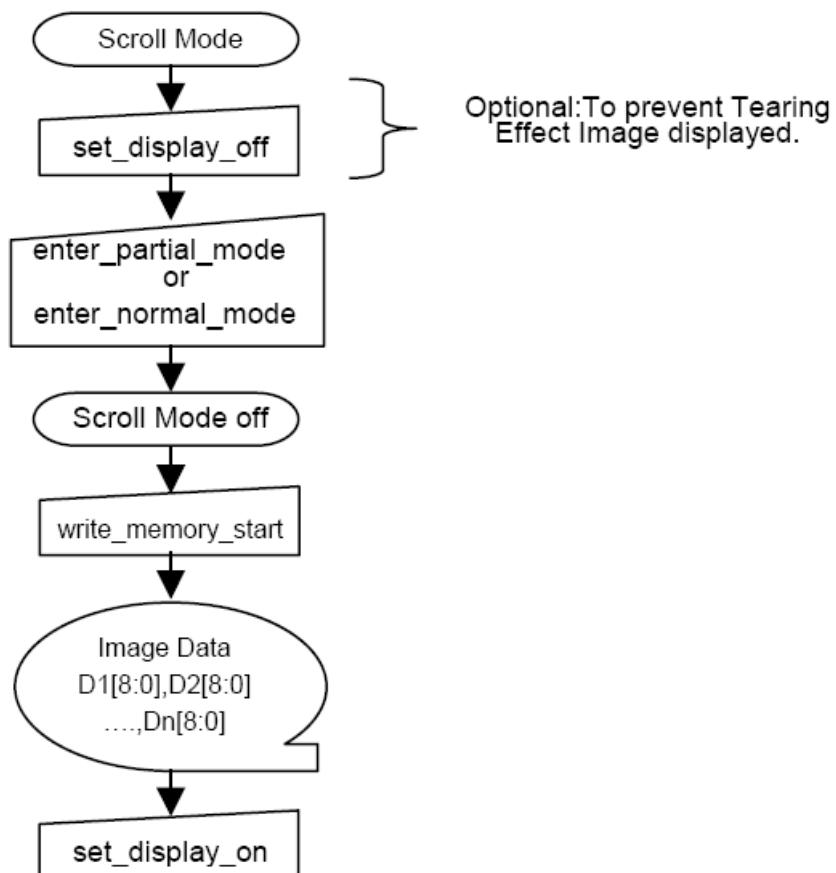


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2. Continuous scroll:



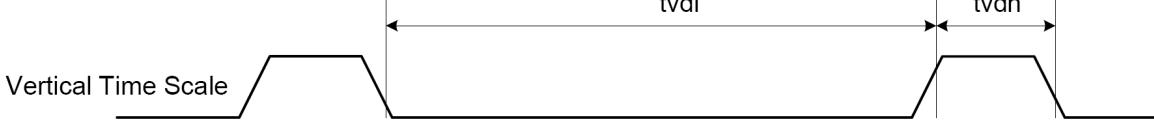
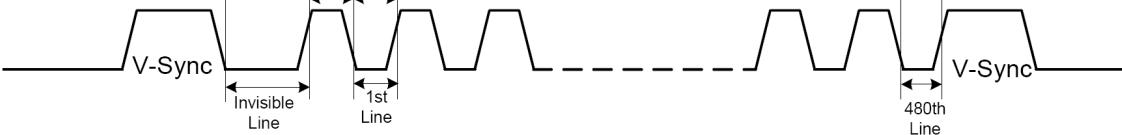
3. To leave vertical scroll mode:



8.2.23. Set_tear_off (34h)

34H		Set_tear_off																																				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																									
Command	0	1	↑	x	0	0	1	1	0	1	0	0	34																									
Parameter	NO PARAMETER																																					
Description	This command turns off the display module's Tearing Effect output signal on the TE signal line.																																					
Restriction	This command has no effect when the Tearing Effect output is already off.																																					
Register Availability	<table border="1"> <thead> <tr> <th colspan="2">Status</th><th colspan="2">Availability</th></tr> </thead> <tbody> <tr> <td colspan="2">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="2">Yes</td></tr> <tr> <td colspan="2">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="2">Yes</td></tr> <tr> <td colspan="2">Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="2">Yes</td></tr> <tr> <td colspan="2">Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="2">Yes</td></tr> <tr> <td colspan="2">Sleep In</td><td colspan="2" rowspan="2">Yes</td></tr> </tbody> </table>														Status		Availability		Normal Mode On, Idle Mode Off, Sleep Out		Yes		Normal Mode On, Idle Mode On, Sleep Out		Yes		Partial Mode On, Idle Mode Off, Sleep Out		Yes		Partial Mode On, Idle Mode On, Sleep Out		Yes		Sleep In		Yes	
Status		Availability																																				
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Status		Default Value																																				
Power On Sequence		OFF																																				
SW Reset		OFF																																				
HW Reset		OFF																																				
Flow Chart	<pre> graph TD A([TE output On or Off]) --> B[Set_tear_off] B --> C([TE output off]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																																					

8.2.24. Set_tear_on (35h)

35H	Set_tear_on																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	1	0	1	0	1	35												
1 st parameter	1	1	↑	x	x	x	x	x	x	x	x	TELOM	xx												
Description	<p>This command turns on the tearing Effect output signal on the TE signal line. The TE signal is not affected by changing set_address_mode (36h) bit B4 (Line Address Order).</p> <p>The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.</p> <p>If TELOM = 0:</p> <p>The Tearing Effect Output line consists of V-Blanking information only.</p>  <p>If TELOM = 1:</p> <p>The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information.</p>  <p>The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</p>																								
Restriction	This command has no effect when Tearing Effect output is already ON.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Sleep In	Yes																								

Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></tbody></table>	Status	Default Value	Power On Sequence	OFF	SW Reset	OFF	HW Reset	OFF	
Status	Default Value									
Power On Sequence	OFF									
SW Reset	OFF									
HW Reset	OFF									
<pre>graph TD; A([TE output On or Off]) --> B[Set_tear_on]; B --> C{TELOM}; C --> D([TE output On]);</pre>	<p>Legend</p> <ul style="list-style-type: none">CommandParameterDisplayActionModeSequential transfer									
Flow Chart										

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8.2.25. Set_address_mode (36h)

36H		Set_address_mode												
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command		0	1	↑	x	0	0	1	1	0	1	1	0	36
1 st parameter		1	1	↑	x	B7	B6	B5	B4	B3	0	B1	B0	xx
Description	This command defines read/write scanning direction of frame memory. This command makes no change on the other driver status.													
	Bit	Description							Comment					
	B7	Page Address Order												
	B6	Column Address Order												
	B5	Page/Column Selection												
	B4	Vertical Order												
	B3	RGB/BGR Order												
	B2	Display data latch data order							Set to '0'					
	B1	Horizontal Flip												
	B0	Vertical Flip												
Bit B7 – Page Address Order '0' = Top to Bottom '1' = Bottom to Top Bit B6 – Column Address Order '0' = Left to Right '1' = Right to Left Bit B5 – Page/Column Order '0' = Normal Mode '1' = Reverse Mode Bit B4 –Line Address Order '0' = LCD Refresh Top to Bottom '1' = LCD Refresh Bottom to Top Bit B3 – RGB/BGR Order '0' = Pixels sent in RGB order '1' = Pixels sent in BGR order Bit B2 –Display Data Latch Data Order This bit is not applicable for this project, so it is set to '0'. (Not supported) Bit B1 – Horizontal Flip														

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'0' = Normal display

'1' = Flipped display

Bit B0 – Vertical Flip

'0' = Normal display

'1' = Flipped display

X = Don't care

B5	B6	B7	Image in Frame Memory
0	0	0	
0	0	1	
0	1	0	
0	1	1	

B5	B6	B7	Image in Frame Memory
1	0	0	
1	0	1	
1	1	0	
1	1	1	

B3 = 0



B3 = 1

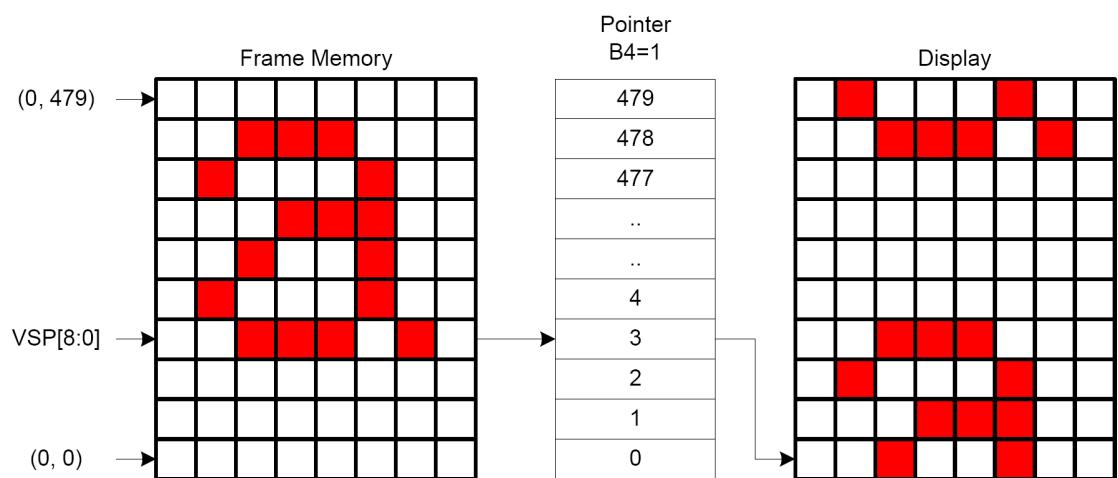


Restriction													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>0000 0000HEX</td> </tr> <tr> <td>SW Reset</td> <td>No Change</td> </tr> <tr> <td>HW Reset</td> <td>0000 0000HEX</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	0000 0000HEX	SW Reset	No Change	HW Reset	0000 0000HEX				
Status	Default Value												
Power On Sequence	0000 0000HEX												
SW Reset	No Change												
HW Reset	0000 0000HEX												
Flow chart	<pre> graph TD A([Address mode]) --> B[Set_address_mode] B --> C{B7,B6,B5,B4,B0} C --> D([New Address mode]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

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8.2.26. Set_scroll_start (37h)

37H	Set_scroll_start																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command	0	1	↑	x	0	0	1	1	0	1	1	1	37											
1 st parameter	1	1	↑	x	0	0	0	0	0	0	0	VSP8	xx											
2 nd parameter	1	1	↑	x	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0	xx											
Description	<p>This command sets the start of the vertical scrolling area in the frame memory. The vertical scrolling area is fully defined when this command is used with the set_scroll_area command.</p> <p>The set_scroll_start command has one parameter, the Vertical Scroll Pointer. The VSP defines the line in the frame memory that is written to the display device as the first line of the vertical scroll area.</p> <p>The displayed image also depends on the setting of the Line Address Order bit, B4, in the set_address_mode register. See the examples below.</p> <p>If set_address_mode (R36h) B4 = 0:</p> <p>Example:</p> <p>When Top Fixed Area = Bottom Fixed Area = 0, Vertical Scrolling Area = 480 and VSP = 3.</p> <table border="1"> <tr><td>0</td></tr> <tr><td>1</td></tr> <tr><td>2</td></tr> <tr><td>3</td></tr> <tr><td>4</td></tr> <tr><td>..</td></tr> <tr><td>..</td></tr> <tr><td>477</td></tr> <tr><td>478</td></tr> <tr><td>479</td></tr> </table> <p>If set_address_mode (R36h) B4 = 1:</p> <p>Example:</p> <p>When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 480 and VSP='3'.</p>	0	1	2	3	4	477	478	479													
0																								
1																								
2																								
3																								
4																								
..																								
..																								
477																								
478																								
479																								



Note: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.

Restriction	Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h) – otherwise undesirable image will be displayed on the Panel.												
Register Availability	<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	No	Partial Mode On, Idle Mode On, Sleep Out	No	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
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Sleep In	Yes												
Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>0000HEX</td></tr><tr><td>SW Reset</td><td>0000HEX</td></tr><tr><td>HW Reset</td><td>0000HEX</td></tr></tbody></table>	Status	Default Value	Power On Sequence	0000HEX	SW Reset	0000HEX	HW Reset	0000HEX				
Status	Default Value												
Power On Sequence	0000HEX												
SW Reset	0000HEX												
HW Reset	0000HEX												
Flow chart	Refer to the description set_scroll_area (33h)												

8.2.27. Exit_idle_mode (38h)

Exit_idle_mode																									
38H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	0	1	1	1	0	0	0	38												
Parameter	NO PARAMETER																								
Description	This command causes the display module to exit Idle mode.																								
Restriction	This command has no effect when the display module is not in Idle mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	Idle Mode Off																								
SW Reset	Idle Mode Off																								
HW Reset	Idle Mode Off																								
Flow Chart	<pre> graph TD A([Idle mode on]) --> B[Exit_idle_mode] B --> C([Idle mode off]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

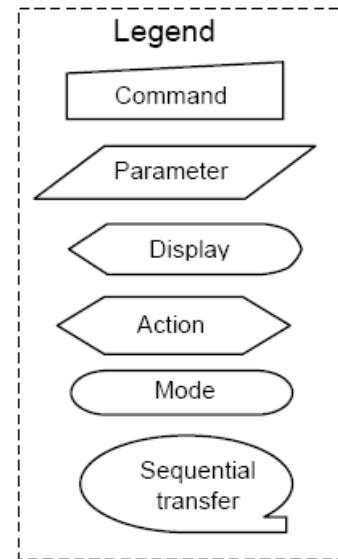
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8.2.28. Enter_idle_mode (39h)

39H		Enter_idle_mode																																															
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
Command	0	1	↑	x	0	0	1	1	1	0	0	1	39																																				
Parameter	NO PARAMETER																																																
Description	<p>This command causes the display module to enter Idle Mode.</p> <p>In Idle Mode, color expression is reduced. Colors are shown on the display device using the MSB of each of the R, G and B color components in the frame memory.</p> <table border="1"> <tr> <th></th> <th>R5 R4 R3 R2 R1 R0</th> <th>G5 G4 G3 G2 G1 G0</th> <th>B5 B4 B3 B2 B1 B0</th> </tr> <tr> <td>Black</td> <td>0XXXXXX</td> <td>0XXXXXX</td> <td>0XXXXXX</td> </tr> <tr> <td>Blue</td> <td>0XXXXXX</td> <td>0XXXXXX</td> <td>1XXXXXX</td> </tr> <tr> <td>Red</td> <td>1XXXXXX</td> <td>0XXXXXX</td> <td>0XXXXXX</td> </tr> <tr> <td>Magenta</td> <td>1XXXXXX</td> <td>0XXXXXX</td> <td>1XXXXXX</td> </tr> <tr> <td>Green</td> <td>0XXXXXX</td> <td>1XXXXXX</td> <td>0XXXXXX</td> </tr> <tr> <td>Cyan</td> <td>0XXXXXX</td> <td>1XXXXXX</td> <td>1XXXXXX</td> </tr> <tr> <td>Yellow</td> <td>1XXXXXX</td> <td>1XXXXXX</td> <td>0XXXXXX</td> </tr> <tr> <td>White</td> <td>1XXXXXX</td> <td>1XXXXXX</td> <td>1XXXXXX</td> </tr> </table>														R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B2 B1 B0	Black	0XXXXXX	0XXXXXX	0XXXXXX	Blue	0XXXXXX	0XXXXXX	1XXXXXX	Red	1XXXXXX	0XXXXXX	0XXXXXX	Magenta	1XXXXXX	0XXXXXX	1XXXXXX	Green	0XXXXXX	1XXXXXX	0XXXXXX	Cyan	0XXXXXX	1XXXXXX	1XXXXXX	Yellow	1XXXXXX	1XXXXXX	0XXXXXX	White	1XXXXXX	1XXXXXX	1XXXXXX
	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B2 B1 B0																																														
Black	0XXXXXX	0XXXXXX	0XXXXXX																																														
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Green	0XXXXXX	1XXXXXX	0XXXXXX																																														
Cyan	0XXXXXX	1XXXXXX	1XXXXXX																																														
Yellow	1XXXXXX	1XXXXXX	0XXXXXX																																														
White	1XXXXXX	1XXXXXX	1XXXXXX																																														
Restriction	This command has no effect when module is already in idle mode.																																																
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																								
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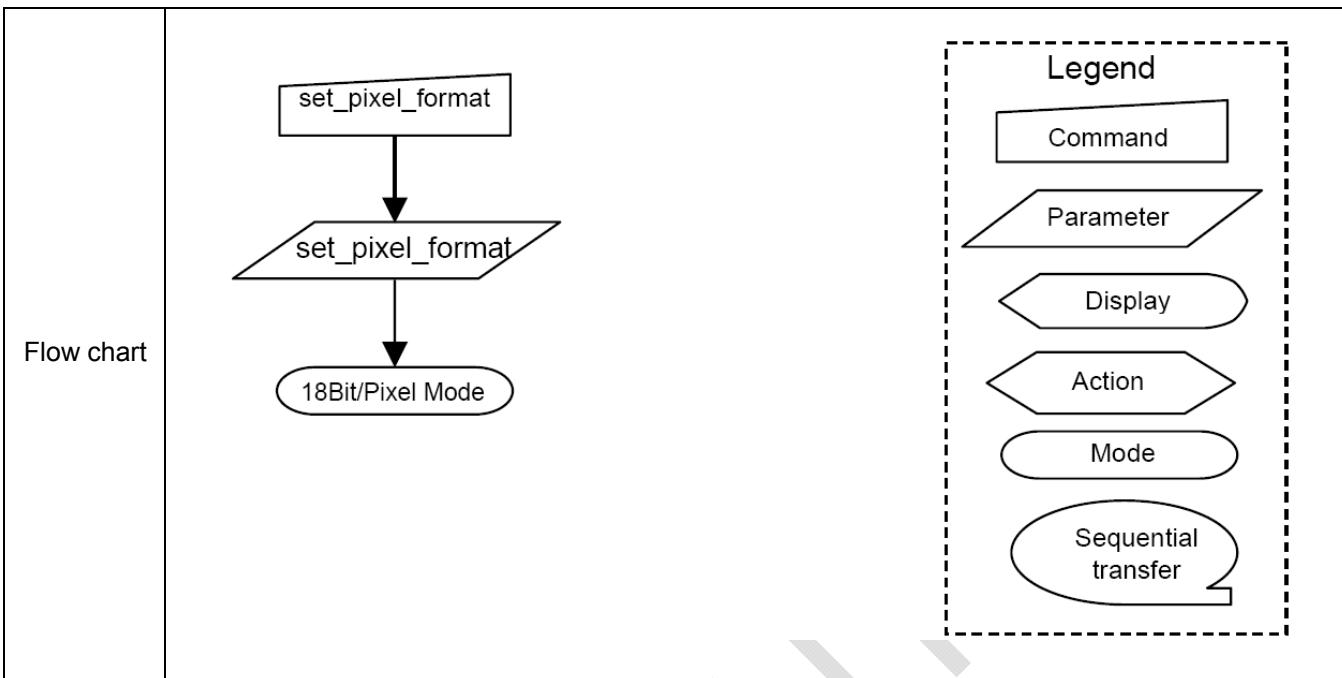
Default		<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Idle Mode Off</td></tr><tr><td>SW Reset</td><td>Idle Mode Off</td></tr><tr><td>HW Reset</td><td>Idle Mode Off</td></tr></tbody></table>	Status	Default Value	Power On Sequence	Idle Mode Off	SW Reset	Idle Mode Off	HW Reset	Idle Mode Off	
Status	Default Value										
Power On Sequence	Idle Mode Off										
SW Reset	Idle Mode Off										
HW Reset	Idle Mode Off										
<pre>graph TD; A([Idle mode off]) --> B[enter_idle_mode]; B --> C([Idle mode on]);</pre>											



8.2.29. Set_pixel_format (3Ah)

Set_pixel_format																																																	
3AH	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
Command	0	1	↑	x	0	0	1	1	1	0	1	0	3A																																				
1 st parameter	1	1	↑	x	x	D6	D5	D4	x	D2	D1	D0	3A																																				
Description	<p>This command sets the pixel format for the RGB image data used by the interface.</p> <p>Bits D[6:4] – DPI Pixel Format Definition</p> <p>Bits D[2:0] – DBI Pixel Format Definition</p> <p>Bits D7 and D3 are not used.</p> <p>If a particular interface, either DBI or DPI, is not used then the corresponding bits in the parameter are ignored.</p> <table border="1"> <thead> <tr> <th>Control Interface Color Format</th> <th>D6/D2</th> <th>D5/D1</th> <th>D4/D0</th> </tr> </thead> <tbody> <tr> <td>Not defined</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>3bit/pixel (8 color)</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>Not defined</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>Not defined</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>Not defined</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>16bit/pixel (65,536 colors)</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>18bit/pixel (262,144 colors)</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>Not defined</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>													Control Interface Color Format	D6/D2	D5/D1	D4/D0	Not defined	0	0	0	3bit/pixel (8 color)	0	0	1	Not defined	0	1	0	Not defined	0	1	1	Not defined	1	0	0	16bit/pixel (65,536 colors)	1	0	1	18bit/pixel (262,144 colors)	1	1	0	Not defined	1	1	1
Control Interface Color Format	D6/D2	D5/D1	D4/D0																																														
Not defined	0	0	0																																														
3bit/pixel (8 color)	0	0	1																																														
Not defined	0	1	0																																														
Not defined	0	1	1																																														
Not defined	1	0	0																																														
16bit/pixel (65,536 colors)	1	0	1																																														
18bit/pixel (262,144 colors)	1	1	0																																														
Not defined	1	1	1																																														
Restriction	There is no visible effect until the Frame Memory is written to.																																																
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																								
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8.2.30. Write_Memory_Continue (3Ch)

Write_Memory_Continue													
3CH	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	1	1	0	0	3C
1 st parameter	1	1	↑	D1[17..8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	000 3FF
X st parameter	1	1	↑	Dx[17..8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	000 3FF
N st parameter	1	1	↑	Dn[17..8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	000 3FF
Description	<p>This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command.</p> <p>If set_address_mode B5 = 0:</p> <p>Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds $(EC - SC + 1) * (EP - SP + 1)$ the extra pixels are ignored.</p> <p>If set_address_mode B5 = 1:</p> <p>Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds $(EC - SC + 1) * (EP - SP + 1)$ the extra pixels are ignored.</p> <p>Frame Memory Access and Interface setting (B3h), WEMODE=0</p> <p>When the transfer number of data exceeds $(EC-SC+1)*(EP-SP+1)$, the exceeding data will be ignored.</p>												

	<p>Frame Memory Access and Interface setting (B3h), WEMODE=1</p> <p>When the transfer number of data exceeds $(EC-SC+1) \times (EP-SP+1)$, the column and page number will be reset, and the exceeding data will be written into the following column and page.</p>												
Restriction	A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined address.												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>All zero</td></tr> <tr> <td>SW Reset</td><td>No change</td></tr> <tr> <td>HW Reset</td><td>All zero</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	All zero	SW Reset	No change	HW Reset	All zero				
Status	Default Value												
Power On Sequence	All zero												
SW Reset	No change												
HW Reset	All zero												
Flow chart	<pre> graph TD A[Write_memory_continue] --> B{Image Data D1[17:0], D2[17:0] ..., Dn[17:0]} B --> C[Next Command] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

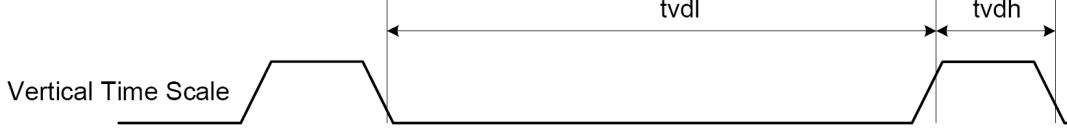
8.2.31. Read_Memory_Continue (3Eh)

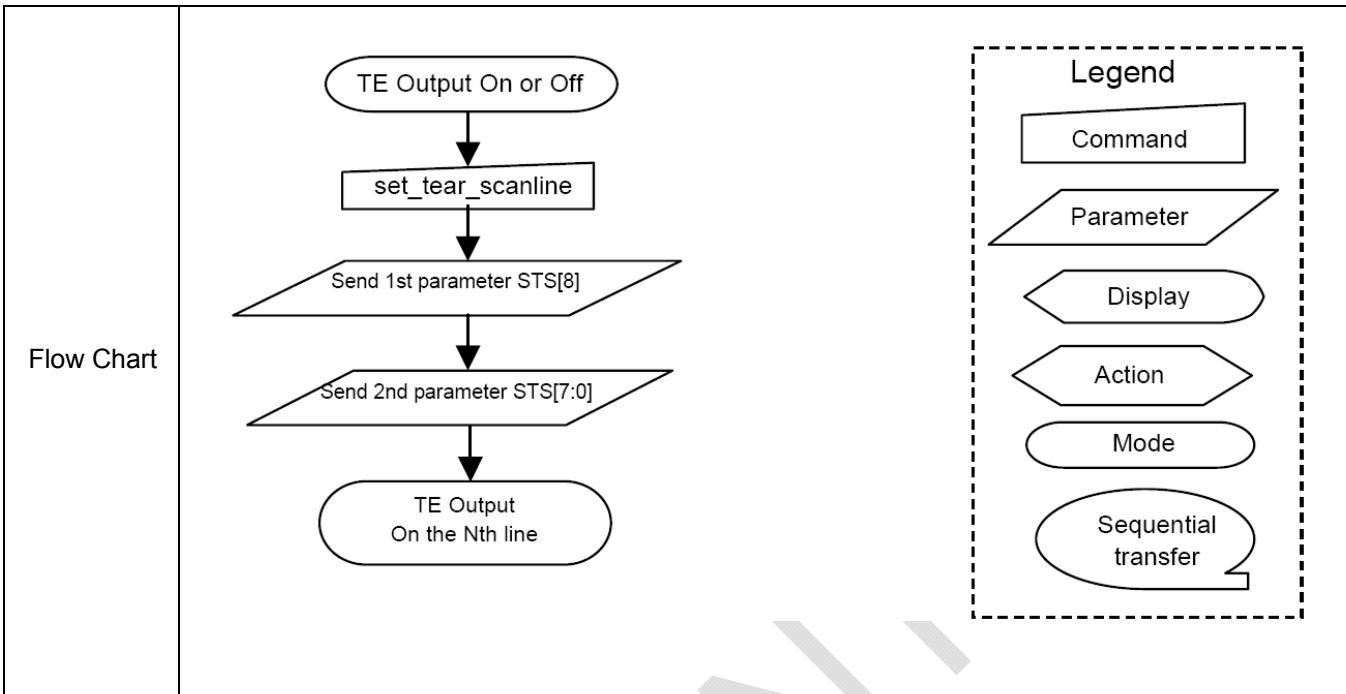
3EH	Read_Memory_Continue												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	1	1	1	0	3E
1 st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2 nd parameter	1	↑	1	D1[17..8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	000 3FF
X st parameter	1	↑	1	Dx[17..8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	000 3FF
N st parameter	1	↑	1	Dn[17..8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	000 3FF
Description	<p>This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue or read_memory_start command.</p> <p>If set_address_mode B5 = 0: Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.</p> <p>If set_address_mode B5 = 1: Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.</p>												
Restriction	<p>Regardless of the color mode set in set_pixel_format, the pixel format returned by read_memory_continue is always 18 bits so there is no restriction on the length of data.</p> <p>A read_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the read location. Otherwise, data read with read_memory_continue is undefined.</p>												

Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes
Status	Availability											
Normal Mode On, Idle Mode Off, Sleep Out	Yes											
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Partial Mode On, Idle Mode Off, Sleep Out	Yes											
Partial Mode On, Idle Mode On, Sleep Out	Yes											
<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Random data</td></tr> <tr> <td>SW Reset</td><td>No change</td></tr> <tr> <td>HW Reset</td><td>Random data</td></tr> </tbody> </table>		Status	Default Value	Power On Sequence	Random data	SW Reset	No change	HW Reset	Random data			
Status	Default Value											
Power On Sequence	Random data											
SW Reset	No change											
HW Reset	Random data											
<pre> graph TD A[Read_memory_start] --> B{Dummy Read} B --> C((Image Data D1[17:0], D2[17:0] ..., Dn[17:0])) C --> D[Next Command] </pre>												
<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

Flow chart

8.2.32. Set_Tear_Scanline (44h)

Set_Tear_Scanline																									
44H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	1	0	0	0	1	0	0	44												
1 st parameter	1	1	↑	xx	0	0	0	0	0	0	0	STS[8:1]	0x												
2 nd parameter	1	1	↑	xx	STS[7]	STS[6]	STS[5]	STS[4]	STS[3]	STS[2]	STS[1]	STS[0]	xx												
Description	<p>This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line N. The TE signal is not affected by changing set_address_mode bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.</p>  <p>The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</p>																								
Restriction																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>STS[8:0]=8'h0000</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>STS[8:0]=8'h0000</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	STS[8:0]=8'h0000	SW Reset	No change	HW Reset	STS[8:0]=8'h0000				
Status	Default Value																								
Power On Sequence	STS[8:0]=8'h0000																								
SW Reset	No change																								
HW Reset	STS[8:0]=8'h0000																								



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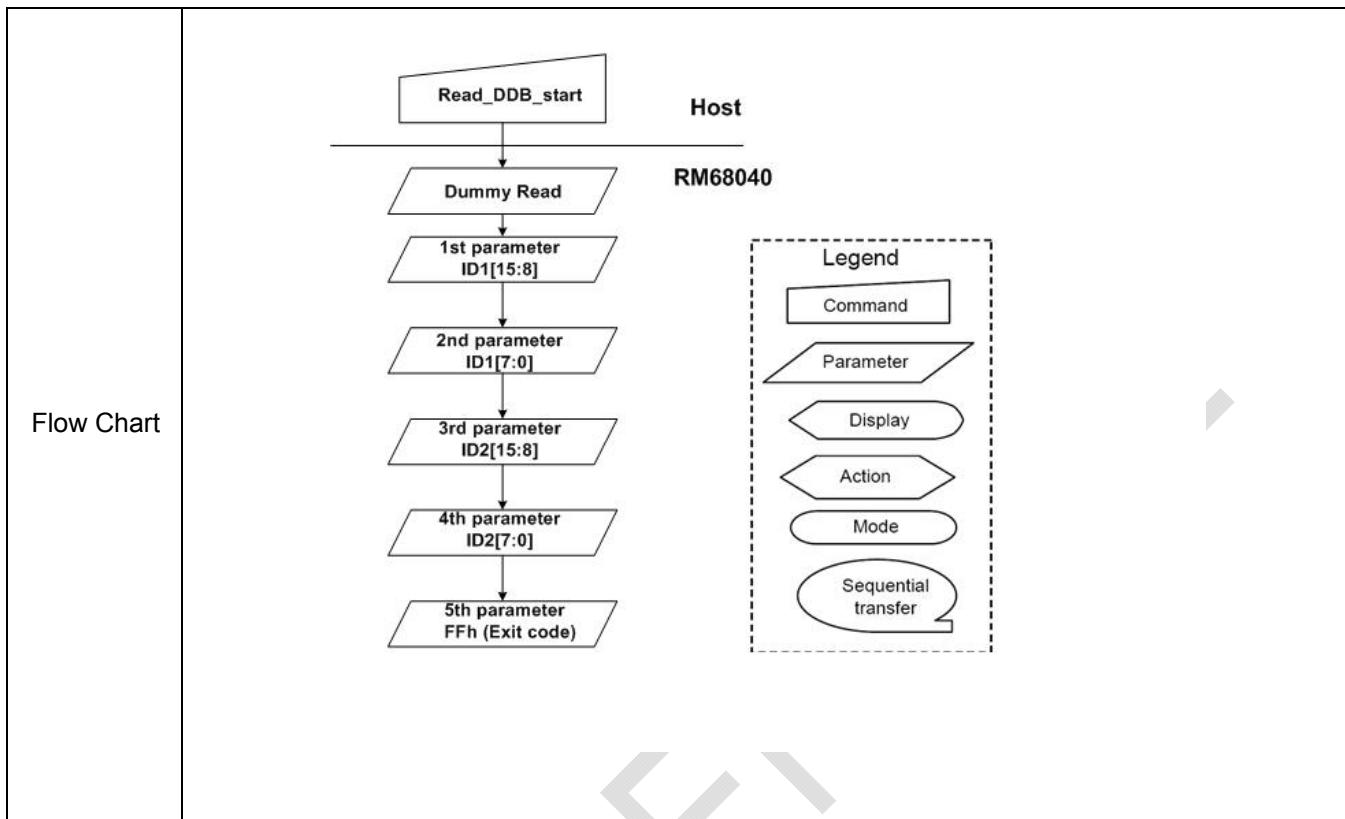
8.2.33. Get_Scanline (45h)

45H		Get_Tear_Scanline																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	0	1	0	0	0	1	0	1	45												
1 st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x												
2 nd parameter	1	↑	1	xx	0	0	0	0	0	0	0	GTS[0] 1	0x												
3 rd parameter	1	↑	1	xx	GTS[7]	GTS[6]	GTS[5]	GTS[4]	GTS[3]	GTS[2]	GTS[1]	GTS[0]	xx												
Description	<p>The display returns the current scan line, N, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0.</p> <p>When in Sleep Mode, the value returned by get_scanline is undefined.</p>																								
Restriction	None.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Flow Chart	<pre> graph TD A[get_scanline] --> B{Wait 3us} B --> C[Dummy Read] C --> D[Send 1st parameter GTS[9:8]] D --> E[Send 2nd parameter GTS[7:0]] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

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8.2.34. Read_DDB_Start (A1h)

A1H	Read_DDB_Start																									
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	x	1	0	1	0	0	0	0	1	A1													
1 st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x													
2 nd parameter	1	↑	1	xx	ID1[15]	ID1[14]	ID1[13]	ID1[12]	ID1[11]	ID1[10]	ID1[9]	ID1[8]	xx													
3 rd parameter	1	↑	1	xx	ID1[7]	ID1[6]	ID1[5]	ID1[4]	ID1[3]	ID1[2]	ID1[1]	ID1[0]	xx													
4 th parameter	1	↑	1	xx	ID2[15]	ID2[14]	ID2[13]	ID2[12]	ID2[11]	ID2[10]	ID2[9]	ID2[8]	xx													
5 th parameter	1	↑	1	xx	ID2[7]	ID2[6]	ID2[5]	ID2[4]	ID2[3]	ID2[2]	ID2[1]	ID2[0]	xx													
6 th parameter	1	↑	1	xx	1	1	1	1	1	1	1	1	FF													
Description	1st parameter: Dummy read 2nd parameter: Supplier ID code ID1[15:8] 3rd parameter: Supplier ID code ID1[7:0] 4th parameter: Supplier Elective Data ID2[15:8] 5th parameter: Supplier Elective Data ID2[7:0]																									
Restriction																										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																									
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Sleep In	Yes																									



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8.2.35. Command Access Protect (B0h)

B0H	Command Access Protect																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	xx	1	0	1	1	0	0	0	0	B0												
1 st parameter	1	1	↑	xx	0	0	0	0	0	0	MCAP[1]	MCAP[0]	xx												
Description	MCAP[1:0]		User	Protect command			Manufacturer Command																		
	00h ~ AFh			B0h			B1h ~ DFh		E0h~EFh		F0h~FFh														
	2'h0		Yes	Yes			Yes		Yes		Yes														
	2'h1		Yes	Yes			Yes		Yes		No														
	2'h2		Yes	Yes			Yes		No		No														
	2'h3		Yes	Yes			No		No		No														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>MCAP[1:0]=2'h0</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>MCAP[1:0]=2'h0</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	MCAP[1:0]=2'h0	SW Reset	No change	HW Reset	MCAP[1:0]=2'h0					
Status	Default Value																								
Power On Sequence	MCAP[1:0]=2'h0																								
SW Reset	No change																								
HW Reset	MCAP[1:0]=2'h0																								
<pre> graph TD A([Sleep Mode]) --> B[Low Power Mode Control] B --> C{DSTB=1} C --> D([Deepstandby Mode]) </pre>																									
<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																									

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8.2.36. Frame Memory Access and Interface Setting (B3h)

B3H	Frame Memory Access and Interface Setting																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	xx	1	0	1	1	0	0	1	1	B3												
1 st parameter	1	1	↑	xx	0	0	0	0	0	0	WEMODE	0	xx												
2 nd parameter	1	1	↑	xx	0	0	0	0	0	TEI[2]	TEI[10]	TEI[0]	xx												
3 rd parameter	1	1	↑	xx	0	0	0	0	0	DENC[2]	DENC[1]	DENC[0]	xx												
4 th parameter	1	1	↑	xx	0	0	EPF[1]	EPF[0]	0	0	0	DFM	xx												
Description	WEMODE: Memory write control																								
	<p>WEMODE=0: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.</p> <p>WEMODE=1: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.</p>																								
	TEI[2:0]: RM68041 starts to output TE signal in the output interval set by TEI[2:0] bits.																								
	<table border="1"> <thead> <tr> <th>TEI[2:0]</th><th>Output Interval</th></tr> </thead> <tbody> <tr> <td>000</td><td>1 frame</td></tr> <tr> <td>001</td><td>2 frame</td></tr> <tr> <td>011</td><td>4 frame</td></tr> <tr> <td>101</td><td>6 frame</td></tr> <tr> <td>Others</td><td>Setting Prohibited</td></tr> </tbody> </table>														TEI[2:0]	Output Interval	000	1 frame	001	2 frame	011	4 frame	101	6 frame	Others
TEI[2:0]	Output Interval																								
000	1 frame																								
001	2 frame																								
011	4 frame																								
101	6 frame																								
Others	Setting Prohibited																								
	DENC[2:0]: Set the GRAM write cycle through the RGB interface																								
	<table border="1"> <thead> <tr> <th>DENC[2:0]</th><th>GRAM Write Cycle (Frame periods)</th></tr> </thead> <tbody> <tr> <td>000</td><td>1 Frame</td></tr> <tr> <td>001</td><td>2 Frames</td></tr> <tr> <td>010</td><td>3 Frames</td></tr> </tbody> </table>														DENC[2:0]	GRAM Write Cycle (Frame periods)	000	1 Frame	001	2 Frames	010	3 Frames			
DENC[2:0]	GRAM Write Cycle (Frame periods)																								
000	1 Frame																								
001	2 Frames																								
010	3 Frames																								

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	011	4 Frames	
	100	5 Frames	
	101	6 Frames	
	110	7 Frames	
	111	8 Frames	

DFM: The bit is used to define image data write/read format to the Frame Memory in DBI Type B (16bit bus interface) and DBI Type C serial interface operation.

EPF[1:0] Set the data format when 16bbp (R,G,B) to 18 bbp (r, g, b) is stored in the internal GRAM.

EPF[1:0]	Expand 16bbp (R,G,B) to 18 bbp (R, G, B)
00	<p>“0” is inputted to LSB</p> <p>r[5:0] = {R[4:0], 0}</p> <p>g[5:0] = {G[5:0]}</p> <p>b[5:0] = {B[4:0], 0}</p> <p>Exception:</p> <p>R[4:0], B[4:0]=5'h1F r[5:0], b[5:0] = 6'h3F</p>
01	<p>“1” is inputted to LSB</p> <p>r[5:0] = {R[4:0], 1}</p> <p>g[5:0] = {G[5:0]}</p> <p>b[5:0] = {B[4:0], 1}</p> <p>Exception:</p> <p>R[4:0], B[4:0]=5'h00 r[5:0], b[5:0] = 6'h00</p>
10	<p>MSB is inputted to LSB</p> <p>r[5:0] = {R[4:0], R[4]}</p> <p>g[5:0] = {G[5:0]}</p> <p>b[5:0] = {B[4:0], B[4]}</p>

	11	Setting disabled													
Register Availability		<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
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Normal Mode On, Idle Mode On, Sleep Out	Yes														
Partial Mode On, Idle Mode Off, Sleep Out	Yes														
Partial Mode On, Idle Mode On, Sleep Out	Yes														
Sleep In	Yes														
Default		<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>WEMODE=1, TEI[2:0]=3'h0, DENC[2:0]=3'h0, DFM=1'h0, EPF[1:0]=2'h0</td></tr><tr><td>SW Reset</td><td>No change</td></tr><tr><td>HW Reset</td><td>WEMODE=1, TEI[2:0]=3'h0, DENC[2:0]=3'h0, DFM=1'h0, EPF[1:0]=2'h0</td></tr></tbody></table>	Status	Default Value	Power On Sequence	WEMODE=1, TEI[2:0]=3'h0, DENC[2:0]=3'h0, DFM=1'h0, EPF[1:0]=2'h0	SW Reset	No change	HW Reset	WEMODE=1, TEI[2:0]=3'h0, DENC[2:0]=3'h0, DFM=1'h0, EPF[1:0]=2'h0					
Status	Default Value														
Power On Sequence	WEMODE=1, TEI[2:0]=3'h0, DENC[2:0]=3'h0, DFM=1'h0, EPF[1:0]=2'h0														
SW Reset	No change														
HW Reset	WEMODE=1, TEI[2:0]=3'h0, DENC[2:0]=3'h0, DFM=1'h0, EPF[1:0]=2'h0														

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8.2.37. Display Mode and Frame Memory Write Mode Setting (B4h)

B4H	Display Mode and Frame Memory Write Mode Setting																												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																
Command	0	1	↑	xx	1	0	1	1	0	1	0	0	B4																
1 st parameter	1	1	↑	xx	0	0	0	RM	0	0	0	DM	xx																
	DM Select the display operation mode.																												
Description	DM	Display Interface																											
	0	Internal system clock																											
	1	DPI (RGB) interface																											
	The DM setting allows switching between internal clock operation mode and external display interface operation mode.																												
Description	RM Select the interface to access the GRAM.																												
	Set RM to "1" when writing display data by the RGB interface.																												
	RM	Interface for RAM Access																											
Description	0	DBI Interface (CPU)																											
	1	DPI Interface (RGB)																											
	<table border="1"> <thead> <tr> <th>Display State</th> <th>Operation Mode</th> <th>RAM Access(RM)</th> <th>Display Operation Mode(DM)</th> </tr> </thead> <tbody> <tr> <td>Still pictures</td> <td>Internal clock operation</td> <td>System interface (RM=0)</td> <td>Internal clock operation (DM=0)</td> </tr> <tr> <td>Moving pictures</td> <td>RGB interface (1)</td> <td>RGB interface (RM = 1)</td> <td>RGB interface (DM = 1)</td> </tr> <tr> <td>Rewrite still picture area while displaying moving pictures.</td> <td>RGB interface</td> <td>System interface (RM = 0)</td> <td>RGB interface (DM = 1)</td> </tr> </tbody> </table>														Display State	Operation Mode	RAM Access(RM)	Display Operation Mode(DM)	Still pictures	Internal clock operation	System interface (RM=0)	Internal clock operation (DM=0)	Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM = 1)	Rewrite still picture area while displaying moving pictures.	RGB interface	System interface (RM = 0)
Display State	Operation Mode	RAM Access(RM)	Display Operation Mode(DM)																										
Still pictures	Internal clock operation	System interface (RM=0)	Internal clock operation (DM=0)																										
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM = 1)																										
Rewrite still picture area while displaying moving pictures.	RGB interface	System interface (RM = 0)	RGB interface (DM = 1)																										

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Register Availability	Status		Availability
	Normal Mode On, Idle Mode Off, Sleep Out		Yes
	Normal Mode On, Idle Mode On, Sleep Out		Yes
	Partial Mode On, Idle Mode Off, Sleep Out		Yes
	Partial Mode On, Idle Mode On, Sleep Out		Yes
	Sleep In		Yes
Default	Status	Default Value	
	Power On Sequence	DM=0, RM=0	
	SW Reset	No change	
	HW Reset	DM=0, RM=0	

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8.2.38. Device Code Read (BFh)

BFH	Device Code Read																									
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	xx	1	0	1	1	1	1	1	1	1	BF												
1st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x	x												
2nd parameter	1	↑	1	xx	0	0	0	0	0	0	1	0	01													
3rd parameter	1	↑	1	xx	0	0	0	0	0	1	0	0	D0													
4th parameter	1	↑	1	xx	1	0	0	1	0	1	0	0	68													
5th parameter	1	↑	1	xx	1	0	0	0	0	0	0	1	04													
6th parameter	1	↑	1	xx	1	1	1	1	1	1	1	1	1	FF												
Description	1st parameter : dummy read 2nd parameter : MIPI Alliance code 3rd parameter : MIPI Alliance code 4th parameter : Device ID code of RM68041 5th parameter : Device ID code of RM68041 6th parameter : Exit code (FFh)																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																									
Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In	Yes																									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>No change</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>No change</td> </tr> </tbody> </table>														Status	Default Value	Power On Sequence	No change	SW Reset	No change	HW Reset	No change				
Status	Default Value																									
Power On Sequence	No change																									
SW Reset	No change																									
HW Reset	No change																									

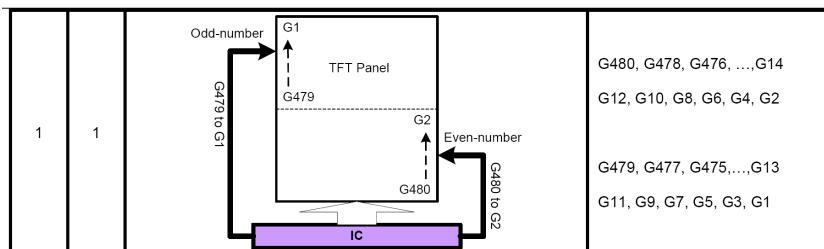
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8.2.39. Panel Driving Setting (C0h)

C0H	Panel Driving Setting												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	0	0	0	C0
1 st parameter	1	1	↑	x	0	0	0	REV	SM	GS	0	0	x
2 nd parameter	1	1	↑	x	0	0	NL[5]	NL[4]	NL[3]	NL[2]	NL[1]	NL[0]	xx
3 rd parameter	1	1	↑	x	0	SCN[6]	SCN[5]	SCN[4]	SCN[3]	SCN[2]	SCN[1]	SCN[0]	xx
4 th parameter	1	1	↑	x	0	0	0	NDL	0	PTS[2]	PTS[1]	PTS[0]	xx
5 th parameter	1	1	↑	x	0	0	0	PTG	ISC[3]	ISC[2]	ISC[1]	ISC[0]	xx
Description	SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.												
	SM	GS	Scan Direction								Gate Output Sequence		
	0	0									G1, G2, G3, G4, ..., G476 G477, G478, G479, G480		
	0	1									G480, G479, G478, ..., G9 G7, G5, G4, G3, G2, G1		
	1	0									G1, G3, G5, G7, ..., G471 G473, G475, G477, G479 G2, G4, G6, G8, ..., G472 G474, G476, G478, G480		

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REV: Enables the grayscale inversion of the image by setting REV=1.



REV	GRAM data	Source Output in Display Area	
		Positive polarity	Negative polarity
0	18'h00000	V63	V0
	:	:	:
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	:	:	:
	18'h3FFFF	V63	V0

NL[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[5:0]	LCD Drive Line
6'h00 ~ 6'h3B	8 * (NL[5:0]+1) lines
Others	Setting inhibited

SCN[6:0]	Scanning Start Position			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
00h ~ 3Bh	G[1+SCN[6:0]*4]	G[480 - SCN[6:0]*4]	G[1+SCN[6:0]*8]	G[480 - SCN[6:0]*8]
3Ch ~ 77h	G[1+SCN[6:0]*4]	G[480 - SCN[6:0]*4]	G[2+(SCN[6:0]-3Ch)*8]	G[479 - (SCN[6:0]-3Ch)*8]
Others	Setting disabled	Setting disabled	Setting disabled	Setting disabled

	<p>NDL: Sets the source output level in non-display area. Settings are different to normally black panels and normally white panels.</p> <table border="1"><thead><tr><th rowspan="2">NDL</th><th colspan="2">Non-display Area</th></tr><tr><th>Positive</th><th>Negative</th></tr></thead><tbody><tr><td>0</td><td>V63</td><td>V0</td></tr><tr><td>1</td><td>V0</td><td>V63</td></tr></tbody></table> <p>PTG: Sets the scan mode in non-display area. Select frame-inversion AC drive when interval-scan is selected.</p> <table border="1"><thead><tr><th>PTG</th><th>Scan Mode in non-display area</th></tr></thead><tbody><tr><td>0</td><td>Normal Scan</td></tr><tr><td>1</td><td>Interval Scan</td></tr></tbody></table> <p>ISC[3:0]: Set the scan cycle when PTG selects interval scan in non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.</p> <table border="1"><thead><tr><th>ISC[3:0]</th><th>Scan cycle</th><th>$(f_{FRAME})=60\text{Hz}$</th></tr></thead><tbody><tr><td>4'h0</td><td>Setting inhibited</td><td>—</td></tr><tr><td>4'h1</td><td>3 frames</td><td>50ms</td></tr><tr><td>4'h2</td><td>5 frames</td><td>84ms</td></tr><tr><td>4'h3</td><td>7 frames</td><td>117ms</td></tr><tr><td>4'h4</td><td>9 frames</td><td>150ms</td></tr><tr><td>4'h5</td><td>11 frames</td><td>184ms</td></tr><tr><td>4'h6</td><td>13 frames</td><td>217ms</td></tr><tr><td>4'h7</td><td>15 frames</td><td>251ms</td></tr><tr><td>4'h8</td><td>17 frames</td><td>284ms</td></tr><tr><td>4'h9</td><td>19 frames</td><td>317ms</td></tr><tr><td>4'hA</td><td>21 frames</td><td>351ms</td></tr><tr><td>4'hB</td><td>23 frames</td><td>384ms</td></tr></tbody></table>	NDL	Non-display Area		Positive	Negative	0	V63	V0	1	V0	V63	PTG	Scan Mode in non-display area	0	Normal Scan	1	Interval Scan	ISC[3:0]	Scan cycle	$(f_{FRAME})=60\text{Hz}$	4'h0	Setting inhibited	—	4'h1	3 frames	50ms	4'h2	5 frames	84ms	4'h3	7 frames	117ms	4'h4	9 frames	150ms	4'h5	11 frames	184ms	4'h6	13 frames	217ms	4'h7	15 frames	251ms	4'h8	17 frames	284ms	4'h9	19 frames	317ms	4'hA	21 frames	351ms	4'hB	23 frames	384ms
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4'hB	23 frames	384ms																																																							

	4'hD	27 frames	451ms	
	4'hE	29 frames	484ms	
	4'hF	31 frames	518ms	

PTS[2:0]:

Set the source output level in non-display area drive period (front/back porch period and blank area between partial displays).

When PTS[2] = 1, the operation of amplifiers which generates the grayscales other than V0 and V63 are halted and the step-up clock frequency becomes half the normal frequency in non-display drive period in order to reduce power consumption.

PTS[2:0]	Source output level		Grayscale amplifier in operation	Step-up clock frequency
	Positive polarity	Negative polarity		
000	V63	V0	V63 and V0	Register Setting(DC1, DC0)
001	V0	V63	-	-
010	GND	GND	V63 and V0	Register Setting(DC1, DC0)
011	Hi-Z	Hi-Z	V63 and V0	Register Setting(DC1, DC0)
100	Setting Prohibited	Setting Prohibited		
101	Setting Prohibited	Setting Prohibited		
110	Setting Prohibited	Setting Prohibited		
111	Setting Prohibited	Setting Prohibited		

Restriction		
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	SM=0, GS=0, REV=1, NL[6:0]=7'h3B, SCN[6:0]=7'h0, PTV=0, NDL=0, PTG=1, ISC[3:0]=4'h1, PTS[2:0]=3'h2
	SW Reset	No change
	HW Reset	SM=0, GS=0, REV=1, NL[6:0]=7'h3B, SCN[6:0]=7'h0, PTV=0, NDL=0, PTG=1, ISC[3:0]=4'h1, PTS[2:0]=3'h2

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8.2.40. Display_Timing_Setting for Normal Mode (C1h)

C1H	Display_Timing_Setting for Normal Mode																						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX										
Command	0	1	↑	x	1	1	0	0	0	0	0	1	C1										
1 st parameter	1	1	↑	0	0	0	0	BC0	0	0	DIV0[1]	DIV0[0]	xx										
2 nd parameter	1	1	↑	0	0	0	0	RTN0[4]	RTN0[3]	RTN0[2]	RTN0[1]	RTN0[0]	xx										
3 rd parameter	1	1	↑	0	FP0[3]	FP0[2]	FP0[1]	FP0[0]	BP0[3]	BP0[2]	BP0[1]	BP0[0]	xx										
Description	<p>BC0: BC0 is used to select VCOM liquid crystal drive waveform. BC0 = 0: Frame inversion waveform is selected. BC0 = 1: Line inversion waveform is selected.</p> <p>DIV0[1:0]: DIV0[1:0] is used to set division ratio of internal clock frequency. The internal operation is synchronized with the frequency divided internal clock. When DIV0 setting is changed, the width of the reference clock for liquid crystal control signals is changed. The frame frequency can be adjusted by register setting (RTN and DIV bits). When number of lines to drive is changed, adjust the frame frequency too.</p> <table border="1"> <thead> <tr> <th>DIV0[1:0]</th> <th>Division Ratio</th> </tr> </thead> <tbody> <tr> <td>2'h0</td> <td>1/1</td> </tr> <tr> <td>2'h1</td> <td>1/2</td> </tr> <tr> <td>2'h2</td> <td>1/4</td> </tr> <tr> <td>2'h3</td> <td>1/8</td> </tr> </tbody> </table> <p>Frame Frequency = fosc. / [Clocks per line x division ratio x (Line +BP+FP)] fosc. : internal oscillator frequency clocks per line : RTNn setting division ratio: DIVn setting Line: total driving line number BP: back porch line number FP: front porch line number</p>													DIV0[1:0]	Division Ratio	2'h0	1/1	2'h1	1/2	2'h2	1/4	2'h3	1/8
DIV0[1:0]	Division Ratio																						
2'h0	1/1																						
2'h1	1/2																						
2'h2	1/4																						
2'h3	1/8																						

RTN0[4:0]: RTN0[4:0] is used to set 1H (line) period.

RTN0[4:0]	Clocks per line
5'h00~0F	Setting prohibited
5'h10	16clocks
5'h11	17clocks
5'h12	18clocks
5'h13	19clocks
5'h14	20clocks
5'h15	21clocks
5'h16	22clocks
5'h17	23clocks
5'h18	24clocks
5'h19	25clocks
5'h1A	26clocks
5'h1B	27clocks
5'h1C	28clocks
5'h1D	29clocks
5'h1E	30clocks
5'h1F	31clocks

FP0[3:0], BP0[3:0]

FP0[3:0] is used to set the number of lines for a front porch period (a blank period following the end of display).

BP0[3:0] is used to set the number of lines for a back porch period (a blank period made before the beginning of display).

FP[3:0] BP[3:0]	Front and back porch period (line period)
4'h0	Setting prohibited
4'h1	Setting prohibited
4'h2	2 lines
4'h3	3 lines

		<table border="1"> <tr><td>4'h4</td><td>4 lines</td></tr> <tr><td>4'h5</td><td>5 lines</td></tr> <tr><td>4'h6</td><td>6 lines</td></tr> <tr><td>4'h7</td><td>7 lines</td></tr> <tr><td>4'h8</td><td>8 lines</td></tr> <tr><td>4'h9</td><td>9 lines</td></tr> <tr><td>4'hA</td><td>10 lines</td></tr> <tr><td>4'hB</td><td>11 lines</td></tr> <tr><td>4'hC</td><td>12 lines</td></tr> <tr><td>4'hD</td><td>13 lines</td></tr> <tr><td>4'hE</td><td>14 lines</td></tr> <tr><td>4'hF</td><td>15 lines</td></tr> </table>	4'h4	4 lines	4'h5	5 lines	4'h6	6 lines	4'h7	7 lines	4'h8	8 lines	4'h9	9 lines	4'hA	10 lines	4'hB	11 lines	4'hC	12 lines	4'hD	13 lines	4'hE	14 lines	4'hF	15 lines	
4'h4	4 lines																										
4'h5	5 lines																										
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4'hB	11 lines																										
4'hC	12 lines																										
4'hD	13 lines																										
4'hE	14 lines																										
4'hF	15 lines																										
Note to Setting BP and FP																											
The condition in setting BP and FP bits are: $BP \geq 2$ lines $FP \geq 2$ lines $FP+BP \leq 16$ lines																											
Restriction																											
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Sleep In</td><td>Yes</td></tr> </tbody> </table>			Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes												
Status	Availability																										
Normal Mode On, Idle Mode Off, Sleep Out	Yes																										
Normal Mode On, Idle Mode On, Sleep Out	Yes																										
Partial Mode On, Idle Mode Off, Sleep Out	Yes																										
Partial Mode On, Idle Mode On, Sleep Out	Yes																										
Sleep In	Yes																										
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr><td>Power On Sequence</td><td>BC0=1'h1, DIV0=2'h0, RTN0=5'h10, FP0=4'h8, BP0=4'h8</td></tr> <tr><td>SW Reset</td><td>No change</td></tr> <tr><td>HW Reset</td><td>BC0=1'h1, DIV0=2'h0, RTN0=5'h10, FP0=4'h8, BP0=4'h8</td></tr> </tbody> </table>			Status	Default Value	Power On Sequence	BC0=1'h1, DIV0=2'h0, RTN0=5'h10, FP0=4'h8, BP0=4'h8	SW Reset	No change	HW Reset	BC0=1'h1, DIV0=2'h0, RTN0=5'h10, FP0=4'h8, BP0=4'h8																
Status	Default Value																										
Power On Sequence	BC0=1'h1, DIV0=2'h0, RTN0=5'h10, FP0=4'h8, BP0=4'h8																										
SW Reset	No change																										
HW Reset	BC0=1'h1, DIV0=2'h0, RTN0=5'h10, FP0=4'h8, BP0=4'h8																										

8.2.41. Display_Timing_Setting for Partial Mode (C2h)

C2H	Display_Timing_Setting for Partial Mode																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command	0	1	↑	x	1	1	0	0	0	0	1	0	C2											
1 st parameter	1	1	↑	x	0	0	0	BC1	0	0	DIV1[1]	DIV1[0]	xx											
2 nd parameter	1	1	↑	x	0	0	0	RTN1[4]	RTN1[3]	RTN1[2]	RTN1[1]	RTN1[0]	xx											
3 rd parameter	1	1	↑	x	FP1[3]	FP1[2]	FP1[1]	FP1[0]	BP1[3]	BP1[2]	BP1[1]	BP1[0]	xx											
Description	<p>BC1: BC1 is used to select VCOM liquid crystal drive waveform.</p> <p>BC1 = 0: Frame inversion waveform is selected.</p> <p>BC1 = 1: Line inversion waveform is selected.</p> <p>DIV1[1:0]: DIV1[1:0] is used to set division ratio of internal clock frequency.</p> <p>The internal operation is synchronized with the frequency divided internal clock. When DIV1 setting is changed, the width of the reference clock for liquid crystal control signals is changed.</p> <p>The frame frequency can be adjusted by register setting (RTN and DIV bits). When number of lines to drive is changed, adjust the frame frequency too.</p> <table border="1"> <thead> <tr> <th>DIV1[1:0]</th> <th>Division Ratio</th> </tr> </thead> <tbody> <tr> <td>2'h0</td> <td>1/1</td> </tr> <tr> <td>2'h1</td> <td>1/2</td> </tr> <tr> <td>2'h2</td> <td>1/4</td> </tr> <tr> <td>2'h3</td> <td>1/8</td> </tr> </tbody> </table> <p>Frame Frequency = fosc. / [Clocks per line x division ratio x (Line +BP+FP)]</p> <p>fosc. : internal oscillator frequency</p> <p>clocks per line : RTNn setting</p> <p>division ratio: DIVn setting</p> <p>Line: total driving line number</p> <p>BP: back porch line number</p> <p>FP: front porch line number</p>														DIV1[1:0]	Division Ratio	2'h0	1/1	2'h1	1/2	2'h2	1/4	2'h3	1/8
DIV1[1:0]	Division Ratio																							
2'h0	1/1																							
2'h1	1/2																							
2'h2	1/4																							
2'h3	1/8																							

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RTN1[4:0]: RTN1[4:0] is used to set 1H (line) period.

RTN1[4:0]	Clocks per line
5'h00~0F	Setting prohibited
5'h10	16clocks
5'h11	17clocks
5'h12	18clocks
5'h13	19clocks
5'h14	20clocks
5'h15	21clocks
5'h16	22clocks
5'h17	23clocks
5'h18	24clocks
5'h19	25clocks
5'h1A	26clocks
5'h1B	27clocks
5'h1C	28clocks
5'h1D	29clocks
5'h1E	30clocks
5'h1F	31clocks

FP1[3:0], BP1[3:0]

FP1[3:0] is used to set the number of lines for a front porch period (a blank period following the end of display).

BP1[3:0] is used to set the number of lines for a back porch period (a blank period made before the beginning of display).

FP[3:0] BP[3:0]	Front and back porch period (line period)
4'h0	Setting prohibited
4'h1	Setting prohibited
4'h2	2 lines
4'h3	3 lines

		<table border="1"> <tr><td>4'h4</td><td>4 lines</td></tr> <tr><td>4'h5</td><td>5 lines</td></tr> <tr><td>4'h6</td><td>6 lines</td></tr> <tr><td>4'h7</td><td>7 lines</td></tr> <tr><td>4'h8</td><td>8 lines</td></tr> <tr><td>4'h9</td><td>9 lines</td></tr> <tr><td>4'hA</td><td>10 lines</td></tr> <tr><td>4'hB</td><td>11 lines</td></tr> <tr><td>4'hC</td><td>12 lines</td></tr> <tr><td>4'hD</td><td>13 lines</td></tr> <tr><td>4'hE</td><td>14 lines</td></tr> <tr><td>4'hF</td><td>15 lines</td></tr> </table>	4'h4	4 lines	4'h5	5 lines	4'h6	6 lines	4'h7	7 lines	4'h8	8 lines	4'h9	9 lines	4'hA	10 lines	4'hB	11 lines	4'hC	12 lines	4'hD	13 lines	4'hE	14 lines	4'hF	15 lines	
4'h4	4 lines																										
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8.2.42. Display_Timing_Setting for Idle Mode (C3h)

C3H	Display_Timing_Setting for Normal Mode																						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX										
Command	0	1	↑	x	1	1	0	0	0	0	1	1	C3										
1 st parameter	1	1	↑	0	0	0	0	BC2	0	0	DIV2[1]	DIV2[0]	xx										
2 nd parameter	1	1	↑	0	0	0	0	RTN2[4]	RTN2[3]	RTN2[2]	RTN2[1]	RTN2[0]	xx										
3 rd parameter	1	1	↑	0	FP2[3]	FP2[2]	FP2[1]	FP2[0]	BP2[3]	BP2[2]	BP2[1]	BP2[0]	xx										
Description	<p>BC2: BC2 is used to select VCOM liquid crystal drive waveform. BC2 = 0: Frame inversion waveform is selected. BC2 = 1: Line inversion waveform is selected.</p> <p>DIV2[1:0]: DIV0[1:0] is used to set division ratio of internal clock frequency. The internal operation is synchronized with the frequency divided internal clock. When DIV0 setting is changed, the width of the reference clock for liquid crystal control signals is changed. The frame frequency can be adjusted by register setting (RTN and DIV bits). When number of lines to drive is changed, adjust the frame frequency too.</p> <table border="1"> <thead> <tr> <th>DIV2[1:0]</th> <th>Division Ratio</th> </tr> </thead> <tbody> <tr> <td>2'h0</td> <td>1/1</td> </tr> <tr> <td>2'h1</td> <td>1/2</td> </tr> <tr> <td>2'h2</td> <td>1/4</td> </tr> <tr> <td>2'h3</td> <td>1/8</td> </tr> </tbody> </table> <p>Frame Frequency = fosc. / [Clocks per line x division ratio x (Line +BP+FP)] fosc. : internal oscillator frequency clocks per line : RTNn setting division ratio: DIVn setting Line: total driving line number BP: back porch line number FP: front porch line number</p>													DIV2[1:0]	Division Ratio	2'h0	1/1	2'h1	1/2	2'h2	1/4	2'h3	1/8
DIV2[1:0]	Division Ratio																						
2'h0	1/1																						
2'h1	1/2																						
2'h2	1/4																						
2'h3	1/8																						

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RTN2[4:0]: RTN2[4:0] is used to set 1H (line) period.

RTN2[4:0]	Clocks per line
5'h00~0F	Setting prohibited
5'h10	16clocks
5'h11	17clocks
5'h12	18clocks
5'h13	19clocks
5'h14	20clocks
5'h15	21clocks
5'h16	22clocks
5'h17	23clocks
5'h18	24clocks
5'h19	25clocks
5'h1A	26clocks
5'h1B	27clocks
5'h1C	28clocks
5'h1D	29clocks
5'h1E	30clocks
5'h1F	31clocks

FP2[3:0], BP2[3:0]

FP2[3:0] is used to set the number of lines for a front porch period (a blank period following the end of display).

BP2[3:0] is used to set the number of lines for a back porch period (a blank period made before the beginning of display).

FP[3:0] BP[3:0]	Front and back porch period (line period)
4'h0	Setting prohibited
4'h1	Setting prohibited

		<table border="1"> <tr><td>4'h2</td><td>2 lines</td></tr> <tr><td>4'h3</td><td>3 lines</td></tr> <tr><td>4'h4</td><td>4 lines</td></tr> <tr><td>4'h5</td><td>5 lines</td></tr> <tr><td>4'h6</td><td>6 lines</td></tr> <tr><td>4'h7</td><td>7 lines</td></tr> <tr><td>4'h8</td><td>8 lines</td></tr> <tr><td>4'h9</td><td>9 lines</td></tr> <tr><td>4'hA</td><td>10 lines</td></tr> <tr><td>4'hB</td><td>11 lines</td></tr> <tr><td>4'hC</td><td>12 lines</td></tr> <tr><td>4'hD</td><td>13 lines</td></tr> <tr><td>4'hE</td><td>14 lines</td></tr> <tr><td>4'hF</td><td>15 lines</td></tr> </table>	4'h2	2 lines	4'h3	3 lines	4'h4	4 lines	4'h5	5 lines	4'h6	6 lines	4'h7	7 lines	4'h8	8 lines	4'h9	9 lines	4'hA	10 lines	4'hB	11 lines	4'hC	12 lines	4'hD	13 lines	4'hE	14 lines	4'hF	15 lines	
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SW Reset	No change																														
HW Reset	BC2=1'h1, DIV2=2'h0, RTN2=5'h10, FP2=4'h8, BP2=4'h8																														

8.2.43. Frame Rate and Inversion Control (C5h)

C5H	Frame Rate Control																														
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
Command	0	1	↑	1	1	1	0	0	0	1	0	1	C5																		
1 st parameter	1	1	↑	0	0	0	0	0	0	FRA[2]	FRA[1]	FRA[0]	-																		
Description	Set the frame frequency of the full colors normal mode. The frame frequency needs to meet 80Hz±5% in this mode. <table border="1"> <thead> <tr> <th>FRA[2:0]</th><th>Frame Rate (Hz)</th></tr> </thead> <tbody> <tr><td>000</td><td>125</td></tr> <tr><td>001</td><td>100</td></tr> <tr><td>010</td><td>85</td></tr> <tr><td>011</td><td>72 (default)</td></tr> <tr><td>100</td><td>56</td></tr> <tr><td>101</td><td>50</td></tr> <tr><td>110</td><td>45</td></tr> <tr><td>111</td><td>42</td></tr> </tbody> </table>													FRA[2:0]	Frame Rate (Hz)	000	125	001	100	010	85	011	72 (default)	100	56	101	50	110	45	111	42
FRA[2:0]	Frame Rate (Hz)																														
000	125																														
001	100																														
010	85																														
011	72 (default)																														
100	56																														
101	50																														
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111	42																														
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Status	Default Value																														
	FRA[3:0]																														
Power On Sequence	4'b0011																														
SW Reset	4'b0011																														
HW Reset	4'b0011																														

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8.2.44. Interface Control (C6h)

C6H	Interface Control																									
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	x	1	1	0	0	0	1	1	0	C6													
Parameter	1	1	↑	x	SDA_EN	0	0	VSPL	HSPL	0	EPL	DPL	xx													
Description	<p>DPL: Sets the signal polarity of the PCLK pin.</p> <p>DPL = "0" The data is input on the rising edge of PCLK.</p> <p>DPL = "1" The data is input on the falling edge of PCLK.</p> <p>EPL: Sets the signal polarity of the ENABLE pin.</p> <p>EPL = "0" The data DB[17:0] is written when ENABLE = "0".</p> <p>EPL = "1" The data DB[17:0] is written when ENABLE = "1".</p> <p>HSPL: Sets the signal polarity of the HSYNC pin.</p> <p>HSPL = "0" Low active</p> <p>HSPL = "1" High active</p> <p>VSPL: Sets the signal polarity of the VSYNC pin.</p> <p>VSPL = "0" Low active</p> <p>VSPL = "1" High active</p> <p>SDA_EN: DBI type C interface selection</p> <p>SDA_EN = "0", DIN and DOUT pins are used for DBI type C interface mode.</p> <p>SDA_EN = "1", DIN/SDA pin is used for DBI type C interface mode and DOUT pin is not used.</p>																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In	Yes																									

Default		Status	Default Value
		Power On Sequence	DPL=1'h0, EPL=1'h1, VSPL=1'h0, HSPL=:1'h0,SDA_EN=1'h0
		SW Reset	No change
		HW Reset	DPL=1'h0, EPL=1'h1, VSPL=1'h0, HSPL=:1'h0,SDA_EN=1'h0

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8.2.45. Gamma Setting (C8h)

C8H	Gamma Setting																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	1	1	0	0	1	0	0	0	C8												
1 st parameter	1	1	↑	x	0	KP1[2]	KP1[1]	KP1[0]	0	KP0[2]	KP0[1]	KP0[0]	00												
2 nd parameter	1	1	↑	x	0	KP3[2]	KP3[1]	KP3[0]	0	KP2[2]	KP2[1]	KP2[0]	44												
3 rd parameter	1	1	↑	x	0	KP5[2]	KP5[1]	KP5[0]	0	KP4[2]	KP4[1]	KP4[0]	06												
4 th parameter	1	1	↑	x	0	RP1[2]	RP1[1]	RP1[0]	0	RP0[2]	RP0[1]	RP0[0]	44												
5 th parameter	1	1	↑	x	0	0	0	0	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]	0A												
6 th parameter	1	1	↑	x	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	08												
7 th parameter	1	1	↑	x	0	KN1[2]	KN1[1]	KN1[0]	0	KN0[2]	KN0[1]	KN0[0]	17												
8 th parameter	1	1	↑	x	0	KN3[2]	KN3[1]	KN3[0]	0	KN2[2]	KN2[1]	KN2[0]	33												
9 th parameter	1	1	↑	x	0	KN5[2]	KN5[1]	KN5[0]	0	KN4[2]	KN4[1]	KN4[0]	77												
10 th parameter	1	1	↑	x	0	RN1[2]	RN1[1]	RN1[0]	0	RN0[2]	RN0[1]	RN0[0]	44												
11 th parameter	1	1	↑	x	0	0	0	0	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]	08												
12 th parameter	1	1	↑	x	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0C												
Description	KP5-0[2:0] : γ fine adjustment register for positive polarity RP1-0[2:0] : γ gradient adjustment register for positive polarity VRP1-0[4:0] : γ amplitude adjustment register for positive polarity KN5-0[2:0] : γ fine adjustment register for negative polarity RN1-0[2:0] : γ gradient adjustment register for negative polarity VRN1-0[4:0] : γ amplitude adjustment register for negative polarity																								
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Default	Status	Default Value	
	Power On Sequence	As above	
	SW Reset	No change	
	HW Reset	As above	

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8.2.46. Power_Setting (D0h)

D0H	Power_Setting																																																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																												
Command	0	1	↑	x	1	1	0	1	0	0	0	0	D0																																												
1 st parameter	1	1	↑	x	0	0	0	0	0	VC[2]	VC[1]	VC[0]	xx																																												
2 nd parameter	1	1	↑	x	0	PON	0	0	0	BT[2]	BT[1]	BT[0]	xx																																												
3 rd parameter	1	1	↑	x	0	0	0	VCIRE	VRH[3]	VRH[2]	VRH[1]	VRH[0]	xx																																												
Description	VC[2:0] Sets the ratio factor of Vci to generate the reference voltages Vci1. <table border="1"> <thead> <tr> <th>VC[2:0]</th> <th>Vci1 voltage</th> </tr> </thead> <tbody> <tr> <td>3'h0</td> <td>0.95 x Vci</td> </tr> <tr> <td>3'h1</td> <td>0.90 x Vci</td> </tr> <tr> <td>3'h2</td> <td>0.85 x Vci</td> </tr> <tr> <td>3'h3</td> <td>0.80 x Vci</td> </tr> <tr> <td>3'h4</td> <td>0.75 x Vci</td> </tr> <tr> <td>3'h5</td> <td>0.70 x Vci</td> </tr> <tr> <td>3'h6</td> <td>Disable</td> </tr> <tr> <td>3'h7</td> <td>1.0 x Vci</td> </tr> </tbody> </table> BT[2:0] Sets the Step up factor and output voltage level from the reference voltages Vci1. <table border="1"> <thead> <tr> <th>BT[2:0]</th> <th>DDVDH</th> <th>VCL</th> <th>VGH</th> <th>VGL</th> </tr> </thead> <tbody> <tr> <td>3'h0</td> <td rowspan="8">Vci1 x 2</td> <td rowspan="4">- Vci1</td> <td rowspan="4">Vci1 x 6</td> <td>- Vci1 x 5</td> </tr> <tr> <td>3'h1</td> <td>- Vci1 x 4</td> </tr> <tr> <td>3'h2</td> <td>- Vci1 x 3</td> </tr> <tr> <td>3'h3</td> <td>- Vci1 x 5</td> </tr> <tr> <td>3'h4</td> <td rowspan="4">Vci1 x 5</td> <td>- Vci1 x 4</td> </tr> <tr> <td>3'h5</td> <td>- Vci1 x 3</td> </tr> <tr> <td>3'h6</td> <td rowspan="2">Vci1 x 4</td> <td>- Vci1 x 4</td> </tr> <tr> <td>3'h7</td> <td>- Vci1 x 3</td> </tr> </tbody> </table>													VC[2:0]	Vci1 voltage	3'h0	0.95 x Vci	3'h1	0.90 x Vci	3'h2	0.85 x Vci	3'h3	0.80 x Vci	3'h4	0.75 x Vci	3'h5	0.70 x Vci	3'h6	Disable	3'h7	1.0 x Vci	BT[2:0]	DDVDH	VCL	VGH	VGL	3'h0	Vci1 x 2	- Vci1	Vci1 x 6	- Vci1 x 5	3'h1	- Vci1 x 4	3'h2	- Vci1 x 3	3'h3	- Vci1 x 5	3'h4	Vci1 x 5	- Vci1 x 4	3'h5	- Vci1 x 3	3'h6	Vci1 x 4	- Vci1 x 4	3'h7	- Vci1 x 3
VC[2:0]	Vci1 voltage																																																								
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	<p>Note 1: Connect capacitors where required when using DDVDH, VGH, VGL and VCL voltages.</p> <p>Note 2: Set following voltages within the respective ranges:</p> <p>DDVDH = 6.0V (max)</p> <p>VGH = 18.0V (max)</p> <p>VGL= -12.5V (max)</p> <p>VCL= -3.0V (max).</p> <p>PON is used to control the operation to generate VGL.</p> <p>PON=0: Halts the step-up operation to generate VGL.</p> <p>PON=1: Starts the step-up operation to generate VGL.</p> <p>VRH[3:0]: Sets the factor to generate VREG1OUT from VCI</p> <p>VCIRE: Select the external reference voltage Vci or internal reference voltage VCIR.</p> <table border="1"><tr><td>VCIRE=0</td><td>External reference voltage Vci (default)</td></tr><tr><td>VCIRE =1</td><td>Internal reference voltage 2.5V</td></tr></table> <p>When VCI<2.5V, Internal reference voltage will be same as VCI.</p> <p>Make sure that VC[2:0] and VRH[3:0] setting restriction: $VREG1OUT \leq (DDVDH - 0.25)V$.</p> <table border="1"><thead><tr><th colspan="5">VCIRE =1</th></tr><tr><th>VRH3</th><th>VRH2</th><th>VRH1</th><th>VRH0</th><th>VREG1OUT</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Halt</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>$2.5V \times 2.00=5.000V$</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>$2.5V \times 2.05=5.125V$</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>$2.5V \times 2.10=5.250V$</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>$2.5V \times 2.20=5.500V$</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>$2.5V \times 2.30=5.750V$</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>$2.5V \times 2.40=6.000V$</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>$2.5V \times 2.40=6.000V$</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>$2.5V \times 1.60=4.000V$</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>$2.5V \times 1.65=4.125V$</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>$2.5V \times 1.70=4.250V$</td></tr></tbody></table>	VCIRE=0	External reference voltage Vci (default)	VCIRE =1	Internal reference voltage 2.5V	VCIRE =1					VRH3	VRH2	VRH1	VRH0	VREG1OUT	0	0	0	0	Halt	0	0	0	1	$2.5V \times 2.00=5.000V$	0	0	1	0	$2.5V \times 2.05=5.125V$	0	0	1	1	$2.5V \times 2.10=5.250V$	0	1	0	0	$2.5V \times 2.20=5.500V$	0	1	0	1	$2.5V \times 2.30=5.750V$	0	1	1	0	$2.5V \times 2.40=6.000V$	0	1	1	1	$2.5V \times 2.40=6.000V$	1	0	0	0	$2.5V \times 1.60=4.000V$	1	0	0	1	$2.5V \times 1.65=4.125V$	1	0	1	0	$2.5V \times 1.70=4.250V$
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1	0	1	1	2.5V x 1.75=4.375V
1	1	0	0	2.5V x 1.80=4.500V
1	1	0	1	2.5V x 1.85=4.625V
1	1	1	0	2.5V x 1.90=4.750V
1	1	1	1	2.5V x 1.95=4.875V

VCIRE =0				
VRH3	VRH2	VRH1	VRH0	VREG1OUT
0	0	0	0	Halt
0	0	0	1	Vci x 2.00
0	0	1	0	Vci x 2.05
0	0	1	1	Vci x 2.10
0	1	0	0	Vci x 2.20
0	1	0	1	Vci x 2.30
0	1	1	0	Vci x 2.40
0	1	1	1	Vci x 2.40
1	0	0	0	Vci x 1.60
1	0	0	1	Vci x 1.65
1	0	1	0	Vci x 1.70
1	0	1	1	Vci x 1.75
1	1	0	0	Vci x 1.80
1	1	0	1	Vci x 1.85
1	1	1	0	Vci x 1.90
1	1	1	1	Vci x 1.95

When VCI<2.5V, Internal reference voltage will be same as VCI.

Make sure that VC[2:0] and VRH[3:0] setting restriction: VREG1OUT \leq (DDVDH - 0.25)V.

Register Availability	Status		Availability
	Normal Mode On, Idle Mode Off, Sleep Out		Yes
	Normal Mode On, Idle Mode On, Sleep Out		Yes
	Partial Mode On, Idle Mode Off, Sleep Out		Yes
	Partial Mode On, Idle Mode On, Sleep Out		Yes
	Sleep In		Yes
Default	Status	Default Value	
	Power On Sequence	VC[2:0]=3'h0, BT[2:0]=3'h3, PON=1'h1; VRH[3:0]=4'h8, VCIRE=1'h1	
	SW Reset	No change	
	HW Reset	VC[2:0]=3'h0, BT[2:0]=3'h3, PON=1'h1; VRH[3:0]=4'h8, VCIRE=1'h1	

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8.2.47. VCOM Control (D1h)

D1H	VCOM Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	0	0	0	1	D1
1 st parameter	1	1	↑	x	0	0	0	0	0	0	0	SEL VCM	xx
2 nd parameter	1	1	↑	x	0	0	VCM[5]	VCM[4]	VCM[3]	VCM[2]	VCM[1]	VCM[0]	xx
3 rd parameter	1	1	↑	x	0	0	0	VDV[4]	VDV[3]	VDV[2]	VDV[1]	VDV[0]	xx
Description	VCM [5:0] is used to set factor to generate VCOMH voltage from the reference voltage VREG1OUT.												
	VCM[5:0]	VCOMH Voltage			VCM[5:0]	VCOMH Voltage							
	6'h00	VREG1OUT x 0.685			6'h20	VREG1OUT x 0.845							
	6'h01	VREG1OUT x 0.690			6'h21	VREG1OUT x 0.850							
	6'h02	VREG1OUT x 0.695			6'h22	VREG1OUT x 0.855							
	6'h03	VREG1OUT x 0.700			6'h23	VREG1OUT x 0.860							
	6'h04	VREG1OUT x 0.705			6'h24	VREG1OUT x 0.865							
	6'h05	VREG1OUT x 0.710			6'h25	VREG1OUT x 0.870							
	6'h06	VREG1OUT x 0.715			6'h26	VREG1OUT x 0.875							
	6'h07	VREG1OUT x 0.720			6'h27	VREG1OUT x 0.880							
	6'h08	VREG1OUT x 0.725			6'h28	VREG1OUT x 0.885							
	6'h09	VREG1OUT x 0.730			6'h29	VREG1OUT x 0.890							
	6'h0A	VREG1OUT x 0.735			6'h2A	VREG1OUT x 0.895							
	6'h0B	VREG1OUT x 0.740			6'h2B	VREG1OUT x 0.900							
	6'h0C	VREG1OUT x 0.745			6'h2C	VREG1OUT x 0.905							
	6'h0D	VREG1OUT x 0.750			6'h2D	VREG1OUT x 0.910							
	6'h0E	VREG1OUT x 0.755			6'h2E	VREG1OUT x 0.915							
	6'h0F	VREG1OUT x 0.760			6'h2F	VREG1OUT x 0.920							
	6'h10	VREG1OUT x 0.765			6'h30	VREG1OUT x 0.925							
	6'h11	VREG1OUT x 0.770			6'h31	VREG1OUT x 0.930							
	6'h12	VREG1OUT x 0.775			6'h32	VREG1OUT x 0.935							
	6'h13	VREG1OUT x 0.780			6'h33	VREG1OUT x 0.940							
	6'h14	VREG1OUT x 0.785			6'h34	VREG1OUT x 0.945							
	6'h15	VREG1OUT x 0.790			6'h35	VREG1OUT x 0.950							
	6'h16	VREG1OUT x 0.795			6'h36	VREG1OUT x 0.955							
	6'h17	VREG1OUT x 0.800			6'h37	VREG1OUT x 0.960							
	6'h18	VREG1OUT x 0.805			6'h38	VREG1OUT x 0.965							
	6'h19	VREG1OUT x 0.810			6'h39	VREG1OUT x 0.970							

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		6'h1A	VREG1OUT x 0.815	6'h3A	VREG1OUT x 0.975	
		6'h1B	VREG1OUT x 0.820	6'h3B	VREG1OUT x 0.980	
		6'h1C	VREG1OUT x 0.825	6'h3C	VREG1OUT x 0.985	
		6'h1D	VREG1OUT x 0.830	6'h3D	VREG1OUT x 0.990	
		6'h1E	VREG1OUT x 0.835	6'h3E	VREG1OUT x 0.995	
		6'h1F	VREG1OUT x 0.840	6'h3F	VREG1OUT x 1.000	

VDV[4:0] is used to set the VCOM alternating amplitude in the range of VREG1OUT x 0.70 to VREG1OUT x1.32.

VDV[4:0]	VCOM amplitude	VDV[4:0]	VCOM amplitude
5'h00	VREG1OUT x 0.70	5'h10	VREG1OUT x 1.02
5'h01	VREG1OUT x 0.72	5'h11	VREG1OUT x 1.04
5'h02	VREG1OUT x 0.74	5'h12	VREG1OUT x 1.06
5'h03	VREG1OUT x 0.76	5'h13	VREG1OUT x 1.08
5'h04	VREG1OUT x 0.78	5'h14	VREG1OUT x 1.10
5'h05	VREG1OUT x 0.80	5'h15	VREG1OUT x 1.12
5'h06	VREG1OUT x 0.82	5'h16	VREG1OUT x 1.14
5'h07	VREG1OUT x 0.84	5'h17	VREG1OUT x 1.16
5'h08	VREG1OUT x 0.86	5'h18	VREG1OUT x 1.18
5'h09	VREG1OUT x 0.88	5'h19	VREG1OUT x 1.20
5'h0A	VREG1OUT x 0.90	5'h1A	VREG1OUT x 1.22
5'h0B	VREG1OUT x 0.92	5'h1B	VREG1OUT x 1.24
5'h0C	VREG1OUT x 0.94	5'h1C	VREG1OUT x 1.26
5'h0D	VREG1OUT x 0.96	5'h1D	VREG1OUT x 1.28
5'h0E	VREG1OUT x 0.98	5'h1E	VREG1OUT x 1.30
5'h0F	VREG1OUT x 1.00	5'h1F	VREG1OUT x 1.32

Set VDV[4:0] to let VCOM amplitude less than 6V.

SELVCM: Selection the VCM setting.

SELVCM =0	Register D1h for VCM setting
SELVCM =1	NV Memory selected for VCM setting

Register Availability	Status		Availability
	Normal Mode On, Idle Mode Off, Sleep Out		Yes
	Normal Mode On, Idle Mode On, Sleep Out		Yes
	Partial Mode On, Idle Mode Off, Sleep Out		Yes
	Partial Mode On, Idle Mode On, Sleep Out		Yes
	Sleep In		Yes
Default	Status	Default Value	
	Power On Sequence	VCM[5:0]=6'h00, VDV[4:0]=5'h00, SELVCM=1'h0	
	SW Reset	No change	
	HW Reset	VCM[5:0]=6'h00, VDV[4:0]=5'h00, SELVCM=1'h0	

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8.2.48. Power_Setting for Normal Mode (D2h)

D2H	Power_Setting for Normal Mode																																																									
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																													
Command	0	1	↑	x	1	1	0	1	0	0	1	0	D2																																													
1 st parameter	1	1	↑	x	0	0	0	0	0	AP0[2]	AP0[1]	AP0[0]	xx																																													
2 nd parameter	1	1	↑	x	0	DC10[2]	DC10[1]	DC10[0]	0	DC00[2]	DC00[1]	DC00[0]	xx																																													
Description	<p>AP0[2:0]</p> <p>AP0 bit is used to adjust the constant current in the operational amplifier circuit in the LCD power supply circuit. Larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off between the display quality and the current consumption into account. In no-display period, set AP=3'h0 to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.</p> <table border="1"> <thead> <tr> <th>AP0[2:0]</th> <th>Gamma Driver Amplifier</th> <th>Source Driver Amplifier</th> </tr> </thead> <tbody> <tr> <td>3'h0</td> <td>Halt operation</td> <td>Halt operation</td> </tr> <tr> <td>3'h1</td> <td>1.00</td> <td>1.00</td> </tr> <tr> <td>3'h2</td> <td>1.00</td> <td>0.75</td> </tr> <tr> <td>3'h3</td> <td>1.00</td> <td>0.50</td> </tr> <tr> <td>3'h4</td> <td>0.75</td> <td>1.00</td> </tr> <tr> <td>3'h5</td> <td>0.75</td> <td>0.75</td> </tr> <tr> <td>3'h6</td> <td>0.75</td> <td>0.50</td> </tr> <tr> <td>3'h7</td> <td>0.50</td> <td>0.50</td> </tr> </tbody> </table> <p>DC00[2:0], DC10[2:0]</p> <p>DC00/DC10 are used to select the charge-pump frequency of circuit and circuit2.</p> <table border="1"> <thead> <tr> <th>DC00[2:0]</th> <th>Step-up circuit 1 clock frequency (fDCDC1)</th> </tr> </thead> <tbody> <tr> <td>3'h0</td> <td>Fosc</td> </tr> <tr> <td>3'h1</td> <td>Fosc / 2</td> </tr> <tr> <td>3'h2</td> <td>Fosc / 4</td> </tr> <tr> <td>3'h3</td> <td>Fosc / 8</td> </tr> <tr> <td>3'h4</td> <td>Fosc / 16</td> </tr> <tr> <td>3'h5</td> <td>Fosc / 32</td> </tr> <tr> <td>3'h6</td> <td>Fosc / 64</td> </tr> <tr> <td>3'h7</td> <td>Halt step-up circuit 1</td> </tr> </tbody> </table>													AP0[2:0]	Gamma Driver Amplifier	Source Driver Amplifier	3'h0	Halt operation	Halt operation	3'h1	1.00	1.00	3'h2	1.00	0.75	3'h3	1.00	0.50	3'h4	0.75	1.00	3'h5	0.75	0.75	3'h6	0.75	0.50	3'h7	0.50	0.50	DC00[2:0]	Step-up circuit 1 clock frequency (fDCDC1)	3'h0	Fosc	3'h1	Fosc / 2	3'h2	Fosc / 4	3'h3	Fosc / 8	3'h4	Fosc / 16	3'h5	Fosc / 32	3'h6	Fosc / 64	3'h7	Halt step-up circuit 1
AP0[2:0]	Gamma Driver Amplifier	Source Driver Amplifier																																																								
3'h0	Halt operation	Halt operation																																																								
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3'h7	Halt step-up circuit 1																																																									

	<table border="1"><thead><tr><th>DC10[2:0]</th><th>Step-up circuit 2 clock frequency (fDCDC2)</th></tr></thead><tbody><tr><td>3'h0</td><td>Fosc / 16</td></tr><tr><td>3'h1</td><td>Fosc / 32</td></tr><tr><td>3'h2</td><td>Fosc / 64</td></tr><tr><td>3'h3</td><td>Fosc / 128</td></tr><tr><td>3'h4</td><td>Fosc / 256</td></tr><tr><td>3'h5</td><td>Fosc / 512</td></tr><tr><td>3'h6</td><td>Setting inhibited</td></tr><tr><td>3'h7</td><td>Halt step-up circuit 2</td></tr></tbody></table>	DC10[2:0]	Step-up circuit 2 clock frequency (fDCDC2)	3'h0	Fosc / 16	3'h1	Fosc / 32	3'h2	Fosc / 64	3'h3	Fosc / 128	3'h4	Fosc / 256	3'h5	Fosc / 512	3'h6	Setting inhibited	3'h7	Halt step-up circuit 2	
DC10[2:0]	Step-up circuit 2 clock frequency (fDCDC2)																			
3'h0	Fosc / 16																			
3'h1	Fosc / 32																			
3'h2	Fosc / 64																			
3'h3	Fosc / 128																			
3'h4	Fosc / 256																			
3'h5	Fosc / 512																			
3'h6	Setting inhibited																			
3'h7	Halt step-up circuit 2																			
Register availability	<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability																			
Normal Mode On, Idle Mode Off, Sleep Out	Yes																			
Normal Mode On, Idle Mode On, Sleep Out	Yes																			
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Partial Mode On, Idle Mode On, Sleep Out	Yes																			
Sleep In	Yes																			
Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>AP0[2:0]=3'h1, DC10[2:0]=3'h2, DC00[2:0]=3'h2</td></tr><tr><td>SW Reset</td><td>No change</td></tr><tr><td>HW Reset</td><td>AP0[2:0]=3'h1, DC10[2:0]=3'h2, DC00[2:0]=3'h2</td></tr></tbody></table>	Status	Default Value	Power On Sequence	AP0[2:0]=3'h1, DC10[2:0]=3'h2, DC00[2:0]=3'h2	SW Reset	No change	HW Reset	AP0[2:0]=3'h1, DC10[2:0]=3'h2, DC00[2:0]=3'h2											
Status	Default Value																			
Power On Sequence	AP0[2:0]=3'h1, DC10[2:0]=3'h2, DC00[2:0]=3'h2																			
SW Reset	No change																			
HW Reset	AP0[2:0]=3'h1, DC10[2:0]=3'h2, DC00[2:0]=3'h2																			

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8.2.49. Power_Setting for Partial Mode (D3h)

D3H	Power_Setting for Partial Mode																																																									
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																													
Command	0	1	↑	x	1	1	0	1	0	0	1	1	D3																																													
1 st parameter	1	1	↑	x	0	0	0	0	0	AP1[2]	AP1[1]	AP1[0]	xx																																													
2 nd parameter	1	1	↑	x	0	DC11[2]	DC11[1]	DC11[0]	0	DC01[2]	DC01[1]	DC01[0]	xx																																													
Description	AP1[2:0] AP1 bit is used to adjust the constant current in the operational amplifier circuit in the LCD power supply circuit. Larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off between the display quality and the current consumption into account. In no-display period, set AP1=3'h0 to halt the operational amplifier circuit and the step-up circuits to reduce current consumption. <table border="1"> <thead> <tr> <th>AP1[2:0]</th> <th>Gamma Driver Amplifier</th> <th>Source Driver Amplifier</th> </tr> </thead> <tbody> <tr> <td>3'h0</td> <td>Halt operation</td> <td>Halt operation</td> </tr> <tr> <td>3'h1</td> <td>1.00</td> <td>1.00</td> </tr> <tr> <td>3'h2</td> <td>1.00</td> <td>0.75</td> </tr> <tr> <td>3'h3</td> <td>1.00</td> <td>0.50</td> </tr> <tr> <td>3'h4</td> <td>0.75</td> <td>1.00</td> </tr> <tr> <td>3'h5</td> <td>0.75</td> <td>0.75</td> </tr> <tr> <td>3'h6</td> <td>0.75</td> <td>0.50</td> </tr> <tr> <td>3'h7</td> <td>0.50</td> <td>0.50</td> </tr> </tbody> </table> DC01[2:0], DC11[2:0] DC01/DC11 are used to select the charge-pump frequency of circuit and circuit2. <table border="1"> <thead> <tr> <th>DC01[2:0]</th> <th>Step-up circuit 1 clock frequency</th> </tr> </thead> <tbody> <tr> <td>3'h0</td> <td>Fosc</td> </tr> <tr> <td>3'h1</td> <td>Fosc / 2</td> </tr> <tr> <td>3'h2</td> <td>Fosc / 4</td> </tr> <tr> <td>3'h3</td> <td>Fosc / 8</td> </tr> <tr> <td>3'h4</td> <td>Fosc / 16</td> </tr> <tr> <td>3'h5</td> <td>Fosc / 32</td> </tr> <tr> <td>3'h6</td> <td>Fosc / 64</td> </tr> <tr> <td>3'h7</td> <td>Halt step-up circuit 1</td> </tr> </tbody> </table>													AP1[2:0]	Gamma Driver Amplifier	Source Driver Amplifier	3'h0	Halt operation	Halt operation	3'h1	1.00	1.00	3'h2	1.00	0.75	3'h3	1.00	0.50	3'h4	0.75	1.00	3'h5	0.75	0.75	3'h6	0.75	0.50	3'h7	0.50	0.50	DC01[2:0]	Step-up circuit 1 clock frequency	3'h0	Fosc	3'h1	Fosc / 2	3'h2	Fosc / 4	3'h3	Fosc / 8	3'h4	Fosc / 16	3'h5	Fosc / 32	3'h6	Fosc / 64	3'h7	Halt step-up circuit 1
AP1[2:0]	Gamma Driver Amplifier	Source Driver Amplifier																																																								
3'h0	Halt operation	Halt operation																																																								
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3'h6	0.75	0.50																																																								
3'h7	0.50	0.50																																																								
DC01[2:0]	Step-up circuit 1 clock frequency																																																									
3'h0	Fosc																																																									
3'h1	Fosc / 2																																																									
3'h2	Fosc / 4																																																									
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3'h7	Halt step-up circuit 1																																																									

	<table border="1"><tr><td>DC11[2:0]</td><td>Step-up circuit 2 clock</td></tr><tr><td>3'h0</td><td>Fosc / 16</td></tr><tr><td>3'h1</td><td>Fosc / 32</td></tr><tr><td>3'h2</td><td>Fosc / 64</td></tr><tr><td>3'h3</td><td>Fosc / 128</td></tr><tr><td>3'h4</td><td>Fosc / 256</td></tr><tr><td>3'h5</td><td>Fosc / 512</td></tr><tr><td>3'h6</td><td>Setting inhibited</td></tr><tr><td>3'h7</td><td>Halt step-up circuit 2</td></tr></table>	DC11[2:0]	Step-up circuit 2 clock	3'h0	Fosc / 16	3'h1	Fosc / 32	3'h2	Fosc / 64	3'h3	Fosc / 128	3'h4	Fosc / 256	3'h5	Fosc / 512	3'h6	Setting inhibited	3'h7	Halt step-up circuit 2	
DC11[2:0]	Step-up circuit 2 clock																			
3'h0	Fosc / 16																			
3'h1	Fosc / 32																			
3'h2	Fosc / 64																			
3'h3	Fosc / 128																			
3'h4	Fosc / 256																			
3'h5	Fosc / 512																			
3'h6	Setting inhibited																			
3'h7	Halt step-up circuit 2																			
Register Availability	<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability																			
Normal Mode On, Idle Mode Off, Sleep Out	Yes																			
Normal Mode On, Idle Mode On, Sleep Out	Yes																			
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Partial Mode On, Idle Mode On, Sleep Out	Yes																			
Sleep In	Yes																			
Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>AP1[2:0]=3'h1, DC11[2:0]=3'h2, DC01[2:0]=3'h2</td></tr><tr><td>SW Reset</td><td>No change</td></tr><tr><td>HW Reset</td><td>AP1[2:0]=3'h1, DC11[2:0]=3'h2, DC01[2:0]=3'h2</td></tr></tbody></table>	Status	Default Value	Power On Sequence	AP1[2:0]=3'h1, DC11[2:0]=3'h2, DC01[2:0]=3'h2	SW Reset	No change	HW Reset	AP1[2:0]=3'h1, DC11[2:0]=3'h2, DC01[2:0]=3'h2											
Status	Default Value																			
Power On Sequence	AP1[2:0]=3'h1, DC11[2:0]=3'h2, DC01[2:0]=3'h2																			
SW Reset	No change																			
HW Reset	AP1[2:0]=3'h1, DC11[2:0]=3'h2, DC01[2:0]=3'h2																			

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8.2.50. Power_Setting for Idle Mode (D4h)

D4H	Power_Setting for Idle Mode																																						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																										
Command	0	1	↑	x	1	1	0	1	0	1	0	0	D4																										
1 st parameter	1	1	↑	x	0	0	0	0	0	AP2[2]	AP2[1]	AP2[0]	xx																										
2 nd parameter	1	1	↑	x	0	DC12[2]	DC12[1]	DC12[0]	0	DC02[2]	DC02[1]	DC02[0]	xx																										
Description	AP2[2:0]																																						
	AP2 bit is used to adjust the constant current in the operational amplifier circuit in the LCD power supply circuit. Larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off between the display quality and the current consumption into account. In no-display period, set AP2=3'h0 to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.																																						
	<table border="1"> <thead> <tr> <th>AP2[2:0]</th> <th>Gamma Driver Amplifier</th> <th>Source Driver Amplifier</th> </tr> </thead> <tbody> <tr> <td>3'h0</td> <td>Halt operation</td> <td>Halt operation</td> </tr> <tr> <td>3'h1</td> <td>1.00</td> <td>1.00</td> </tr> <tr> <td>3'h2</td> <td>1.00</td> <td>0.75</td> </tr> <tr> <td>3'h3</td> <td>1.00</td> <td>0.50</td> </tr> <tr> <td>3'h4</td> <td>0.75</td> <td>1.00</td> </tr> <tr> <td>3'h5</td> <td>0.75</td> <td>0.75</td> </tr> <tr> <td>3'h6</td> <td>0.75</td> <td>0.50</td> </tr> <tr> <td>3'h7</td> <td>0.50</td> <td>0.50</td> </tr> </tbody> </table>													AP2[2:0]	Gamma Driver Amplifier	Source Driver Amplifier	3'h0	Halt operation	Halt operation	3'h1	1.00	1.00	3'h2	1.00	0.75	3'h3	1.00	0.50	3'h4	0.75	1.00	3'h5	0.75	0.75	3'h6	0.75	0.50	3'h7	0.50
AP2[2:0]	Gamma Driver Amplifier	Source Driver Amplifier																																					
3'h0	Halt operation	Halt operation																																					
3'h1	1.00	1.00																																					
3'h2	1.00	0.75																																					
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3'h7	0.50	0.50																																					
DC02[2:0], DC12[2:0]																																							
DC01/DC11 are used to select the charge-pump frequency of circuit and circuit2.																																							
<table border="1"> <thead> <tr> <th>DC02[2:0]</th> <th>Step-up circuit 1 clock</th> </tr> </thead> <tbody> <tr> <td>3'h0</td> <td>Fosc</td> </tr> <tr> <td>3'h1</td> <td>Fosc / 2</td> </tr> <tr> <td>3'h2</td> <td>Fosc / 4</td> </tr> <tr> <td>3'h3</td> <td>Fosc / 8</td> </tr> <tr> <td>3'h4</td> <td>Fosc / 16</td> </tr> <tr> <td>3'h5</td> <td>Fosc / 32</td> </tr> <tr> <td>3'h6</td> <td>Fosc / 64</td> </tr> <tr> <td>3'h7</td> <td>Halt step-up circuit 1</td> </tr> </tbody> </table>													DC02[2:0]	Step-up circuit 1 clock	3'h0	Fosc	3'h1	Fosc / 2	3'h2	Fosc / 4	3'h3	Fosc / 8	3'h4	Fosc / 16	3'h5	Fosc / 32	3'h6	Fosc / 64	3'h7	Halt step-up circuit 1									
DC02[2:0]	Step-up circuit 1 clock																																						
3'h0	Fosc																																						
3'h1	Fosc / 2																																						
3'h2	Fosc / 4																																						
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	<table border="1"><tr><td>DC12[2:0]</td><td>Step-up circuit 2 clock</td></tr><tr><td>3'h0</td><td>Fosc / 16</td></tr><tr><td>3'h1</td><td>Fosc / 32</td></tr><tr><td>3'h2</td><td>Fosc / 64</td></tr><tr><td>3'h3</td><td>Fosc / 128</td></tr><tr><td>3'h4</td><td>Fosc / 256</td></tr><tr><td>3'h5</td><td>Fosc / 512</td></tr><tr><td>3'h6</td><td>Setting inhibited</td></tr><tr><td>3'h7</td><td>Halt step-up circuit 2</td></tr></table>	DC12[2:0]	Step-up circuit 2 clock	3'h0	Fosc / 16	3'h1	Fosc / 32	3'h2	Fosc / 64	3'h3	Fosc / 128	3'h4	Fosc / 256	3'h5	Fosc / 512	3'h6	Setting inhibited	3'h7	Halt step-up circuit 2	
DC12[2:0]	Step-up circuit 2 clock																			
3'h0	Fosc / 16																			
3'h1	Fosc / 32																			
3'h2	Fosc / 64																			
3'h3	Fosc / 128																			
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3'h5	Fosc / 512																			
3'h6	Setting inhibited																			
3'h7	Halt step-up circuit 2																			
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Sleep In	Yes																			
Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>AP2[2:0]=3'h1, DC12[2:0]=3'h2, DC02[2:0]=3'h2</td></tr><tr><td>SW Reset</td><td>No change</td></tr><tr><td>HW Reset</td><td>AP2[2:0]=3'h1, DC11[2:0]=3'h2, DC02[2:0]=3'h2</td></tr></tbody></table>	Status	Default Value	Power On Sequence	AP2[2:0]=3'h1, DC12[2:0]=3'h2, DC02[2:0]=3'h2	SW Reset	No change	HW Reset	AP2[2:0]=3'h1, DC11[2:0]=3'h2, DC02[2:0]=3'h2											
Status	Default Value																			
Power On Sequence	AP2[2:0]=3'h1, DC12[2:0]=3'h2, DC02[2:0]=3'h2																			
SW Reset	No change																			
HW Reset	AP2[2:0]=3'h1, DC11[2:0]=3'h2, DC02[2:0]=3'h2																			

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8.2.51. NV Memory Write (E0h)

NV Memory Write																									
E0H	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	1	1	1	0	0	0	0	0	E0												
1 st parameter	1	1	↑	x	VM_D[7]	VM_D[6]	VM_D[5]	VM_D[4]	VM_D[3]	VM_D[2]	VM_D[1]	VM_D[0]	xx												
Description	This command is used to program the NV memory data. VM_D[7:0]: Use to write the data (including VCM and ID code) into the NV memory data.																								
Register Availability	<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>VM_D[7:0]=8'h00</td></tr><tr><td>SW Reset</td><td>No change</td></tr><tr><td>HW Reset</td><td>VM_D[7:0]=8'h00</td></tr></tbody></table>													Status	Default Value	Power On Sequence	VM_D[7:0]=8'h00	SW Reset	No change	HW Reset	VM_D[7:0]=8'h00				
Status	Default Value																								
Power On Sequence	VM_D[7:0]=8'h00																								
SW Reset	No change																								
HW Reset	VM_D[7:0]=8'h00																								

8.2.52. NV Memory Control (E1h)

E1H		NV Memory Control																																				
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																								
Command		0	1	↑	x	1	1	1	0	0	0	0	1	E1																								
1 st parameter		1	1	↑	x	0	0	ID_PGM_EN	VCM_PGM_EN	0	0	ID_SEL[1]	ID_SEL[0]	xx																								
Description	<p>This command is used to control the NV memory programming.</p> <p>ID_SEL[1:0]: ID NV memory selection</p> <table border="1"> <tr> <th>ID_SEL[1:0]</th><th>ID OTP Selection</th></tr> <tr> <td>00</td><td>ID code 1 [15:8]</td></tr> <tr> <td>01</td><td>ID code 1 [7:0]</td></tr> <tr> <td>10</td><td>ID code 2 [15:8]</td></tr> <tr> <td>11</td><td>ID code 2 [7:0]</td></tr> </table> <p>VCM_PGM_EN: VCM OTP programming enable. When writing the VCOMH NV memory, the bit must be set as '1'.</p> <p>ID_PGM_EN: ID OTP programming enable. When writing the ID code NV memory, the bit must be set as '1'.</p> <table border="1"> <tr> <th>ID_PGM_EN</th><th>VCM_PGM_EN</th><th>OTP Programming Selection</th></tr> <tr> <td>0</td><td>0</td><td>NV Memory programming disabled</td></tr> <tr> <td>0</td><td>1</td><td>VCM (VCOMH) NV Memory programming</td></tr> <tr> <td>1</td><td>0</td><td>ID code NV Memory programming enable</td></tr> <tr> <td>1</td><td>1</td><td>Setting Prohibited</td></tr> </table>													ID_SEL[1:0]	ID OTP Selection	00	ID code 1 [15:8]	01	ID code 1 [7:0]	10	ID code 2 [15:8]	11	ID code 2 [7:0]	ID_PGM_EN	VCM_PGM_EN	OTP Programming Selection	0	0	NV Memory programming disabled	0	1	VCM (VCOMH) NV Memory programming	1	0	ID code NV Memory programming enable	1	1	Setting Prohibited
ID_SEL[1:0]	ID OTP Selection																																					
00	ID code 1 [15:8]																																					
01	ID code 1 [7:0]																																					
10	ID code 2 [15:8]																																					
11	ID code 2 [7:0]																																					
ID_PGM_EN	VCM_PGM_EN	OTP Programming Selection																																				
0	0	NV Memory programming disabled																																				
0	1	VCM (VCOMH) NV Memory programming																																				
1	0	ID code NV Memory programming enable																																				
1	1	Setting Prohibited																																				
Restriction																																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes													
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Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>ID_PGM_EN=1'h0; VCM_PGM_EN=1'h0; ID_SEL[1:0]=2'h0</td></tr> <tr> <td>SW Reset</td><td>No change</td></tr> <tr> <td>HW Reset</td><td>ID_PGM_EN=1'h0; VCM_PGM_EN=1'h0; ID_SEL[1:0]=2'h0</td></tr> </tbody> </table>													Status	Default Value	Power On Sequence	ID_PGM_EN=1'h0; VCM_PGM_EN=1'h0; ID_SEL[1:0]=2'h0	SW Reset	No change	HW Reset	ID_PGM_EN=1'h0; VCM_PGM_EN=1'h0; ID_SEL[1:0]=2'h0																	
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8.2.53. NV Memory Status Read (E2h)

E2H		NV Memory Status Read																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	x	1	1	1	0	0	0	1	0	E2													
1 st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x													
2 nd parameter	1	↑	1	x	0	0	0	0	0	0	PGM_C_NT1	PGM_C_NT0	xx													
3 rd parameter	1	↑	1	x	0	0	NV_VCM _[5]	NV_VCM _[4]	NV_VCM _[3]	NV_VCM _[2]	NV_VCM _[1]	NV_VCM _[0]	xx													
Description	PGM_CNT[1:0]: NV memory programmed record. The bit will increase “+1” automatically when writing the NV_VCM [5:0].																									
	<table border="1"> <thead> <tr> <th>PGM_CNT[1:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>NV Memory clean</td> </tr> <tr> <td>01</td> <td>NV Memory programmed 1</td> </tr> <tr> <td>10</td> <td>NV Memory programmed 2</td> </tr> </tbody> </table> <p>These bits are read only.</p> <p>NV_VCM [5:0]: NV memory VCM data read value. These bits are read only.</p>														PGM_CNT[1:0]	Description	00	NV Memory clean	01	NV Memory programmed 1	10	NV Memory programmed 2				
PGM_CNT[1:0]	Description																									
00	NV Memory clean																									
01	NV Memory programmed 1																									
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Sleep In	Yes																									

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8.2.54. NV Memory Protection (E3h)

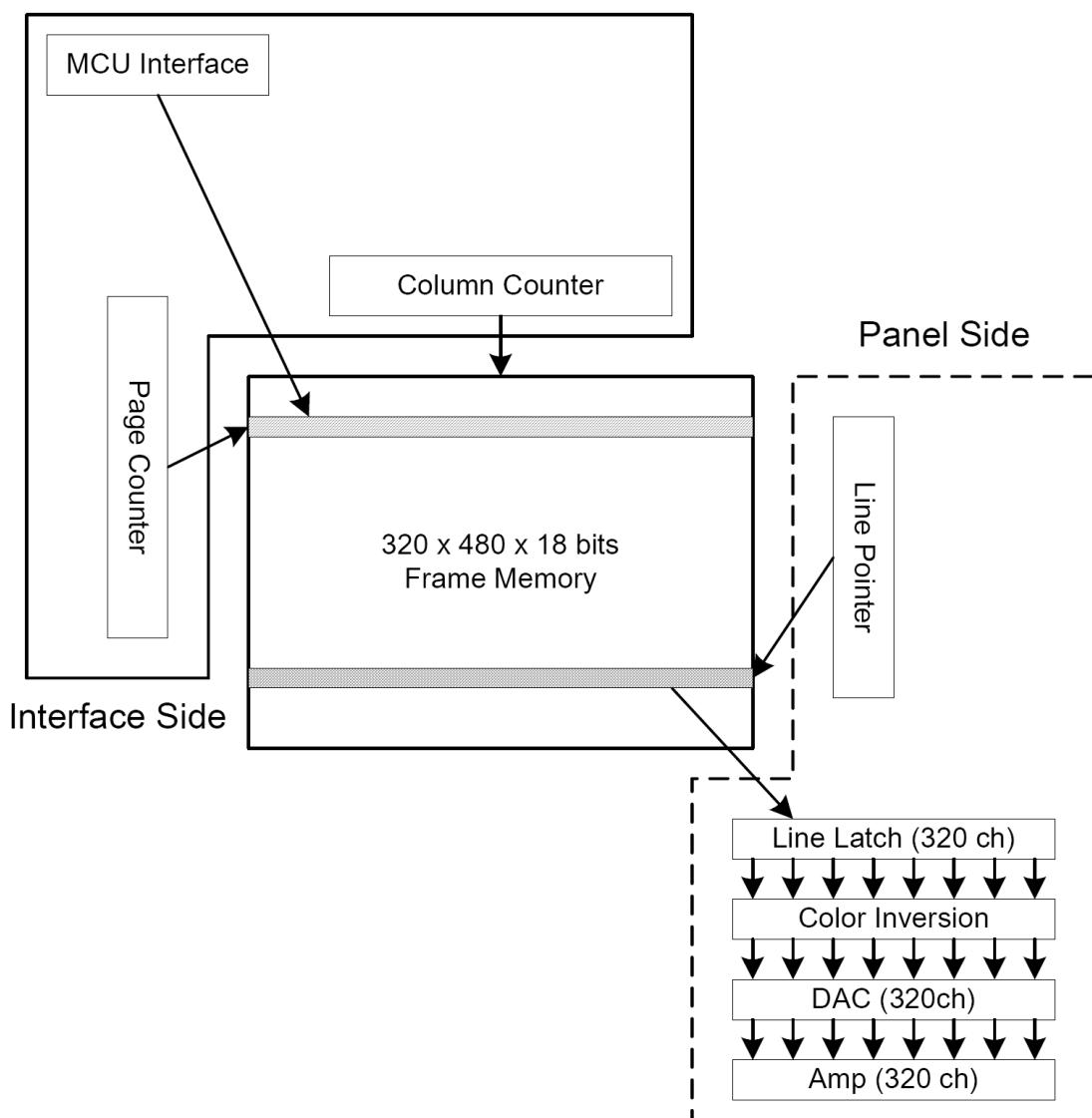
E3H	NV Memory Protection																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	x	1	1	1	0	0	0	1	1	E3												
1 st parameter	1	1	↑	x	KEY[15]	KEY[14]	KEY[13]	KEY[12]	KEY[11]	KEY[10]	KEY[9]	KEY[8]	xx												
2 nd parameter	1	1	↑	x	KEY[7]	KEY[6]	KEY[5]	KEY[4]	KEY[3]	KEY[2]	KEY[1]	KEY[0]	xx												
Description	KEY[15:0]: NV memory programming protection key. When writing OTP data C8h, this register must be set as 0xAA55 to enable OTP programming. If C8h register is not written with 0xAA55, NV memory programming will fail.																								
Restriction																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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9. Display Data RAM

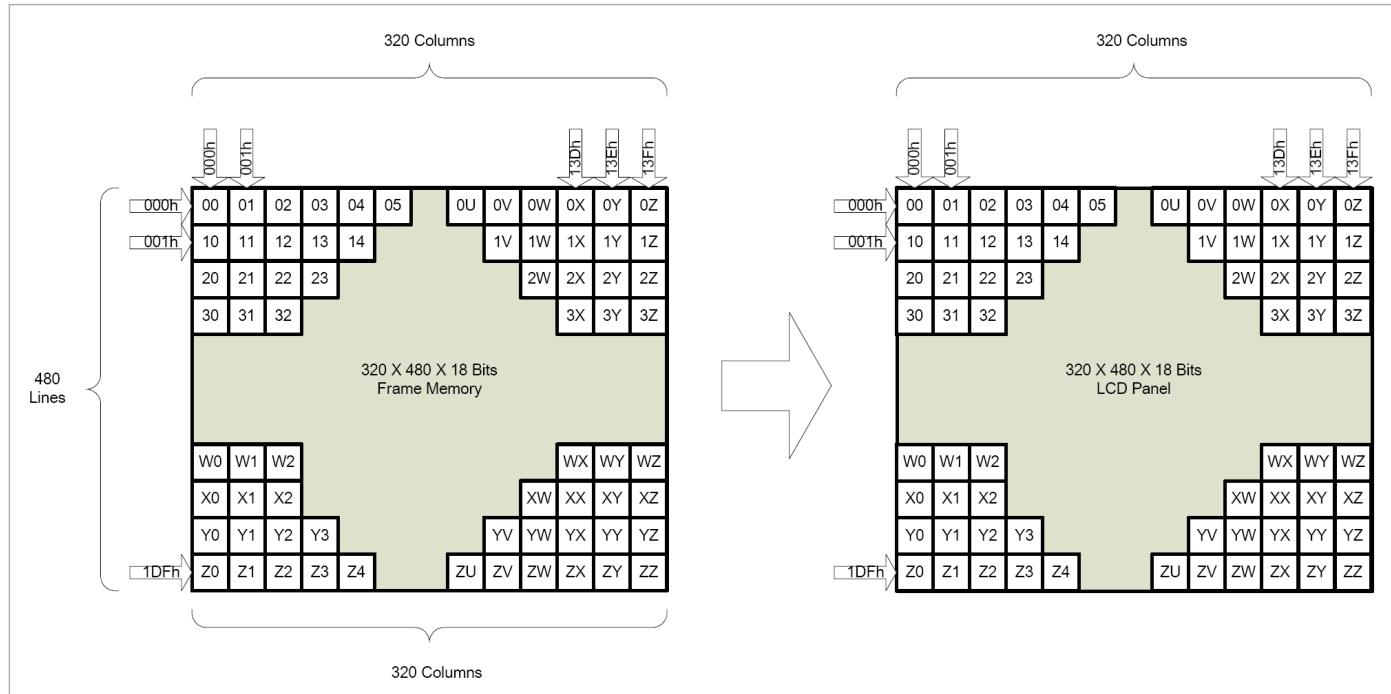
9.1. Configuration

The display data RAM stores display dots and consists of 2,764,800bits (320 x 18 x 480 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the frame memory.



9.2. Memory to Display Address Mapping

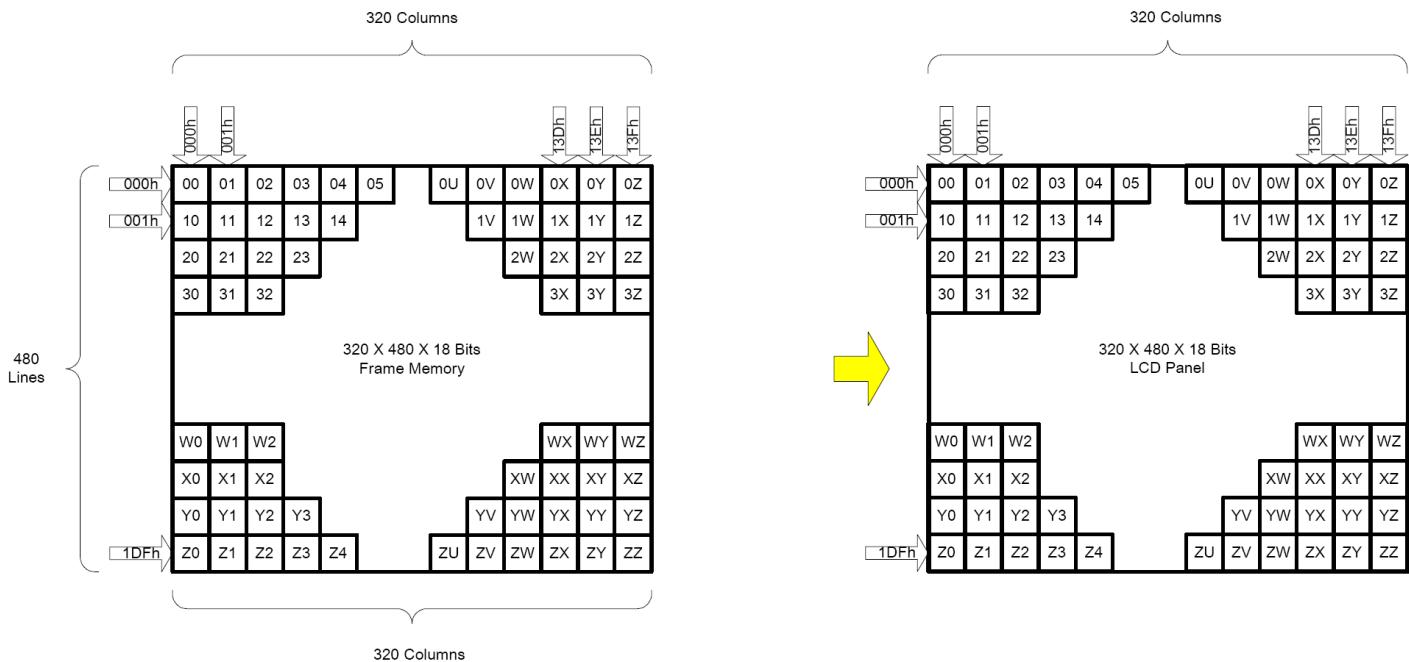
In this mode, content of the frame memory within an area where column pointer is 0000h to 013Fh and page pointer 0000h to 01DFh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0).



9.3. Vertical Scroll Mode

There is a vertical scrolling mode, which is described by the commands “set_scroll_area”(33h) and “set_scroll_start”(37h).

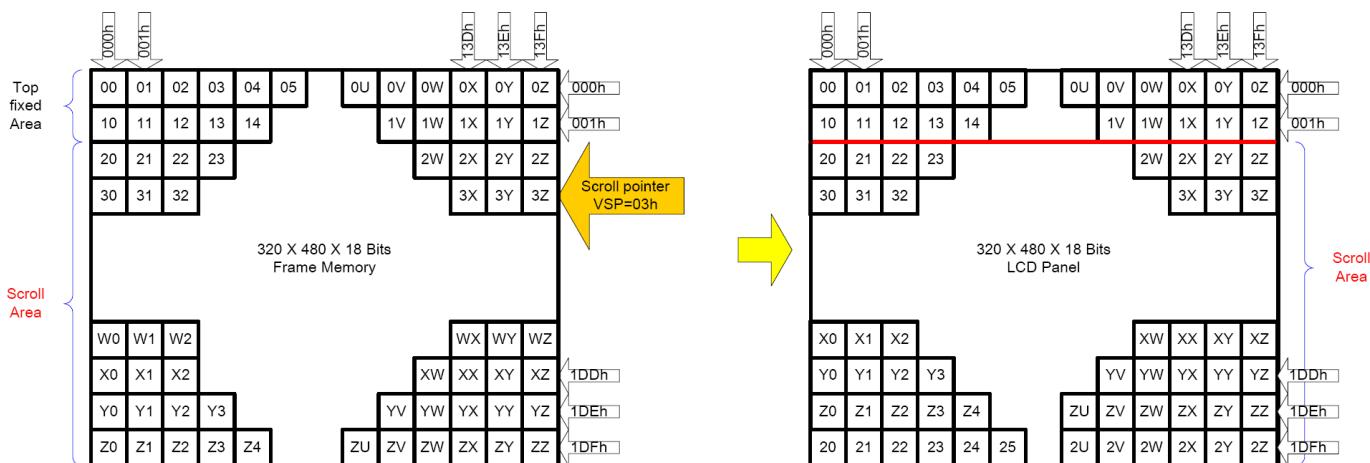
(1) Normal Display On or Partial Mode On, Vertical Scroll Off



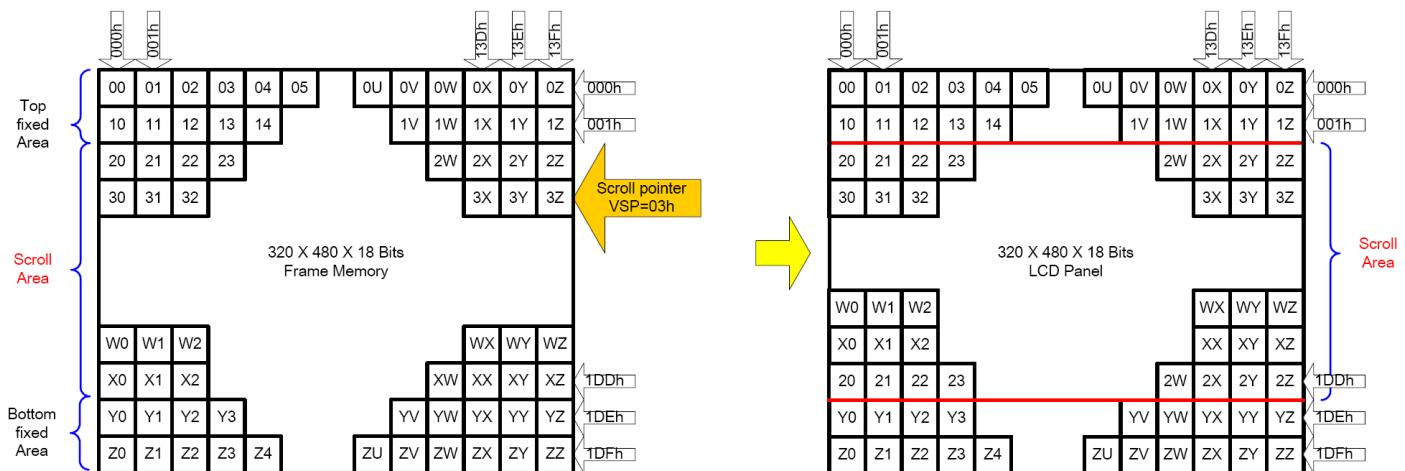
(2) Vertical Scroll Mode

“set_scroll_area(33h)”and “set_scroll_start(37h)” setting define the scroll area.

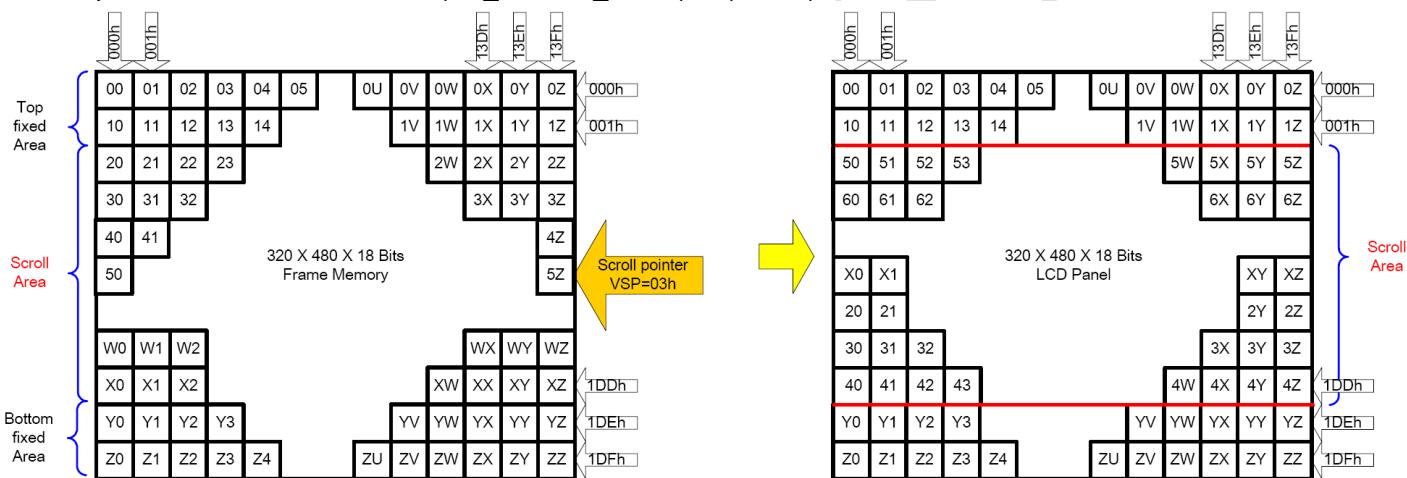
Example1: TFA=2, VSA=478, BFA=0 (set_address_mode(36h) B4=0), VSP=3



Example2: TFA=2,VSA=476,BFA=2 (set_address_mode(36h) B4=0), VSP=3



Example3: TFA=2, SA=476, FA=2 (set_address_mode(36h) B4=0), VSP=5

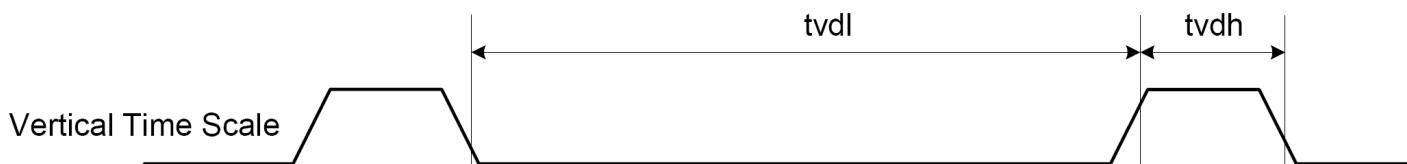


10. Tearing Effect Output

The tearing effect output line supplies to the MCU a panel synchronization signal. This signal can be enabled or disabled by the `set_tear_off` (34h) and `set_tear_on` (35h) commands. The mode of the tearing effect signal is defined by the parameter of the `set_tear_on` (35h) and `set_tear_scanline`(44h) commands. The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

10.1. Tearing Effect Line Modes

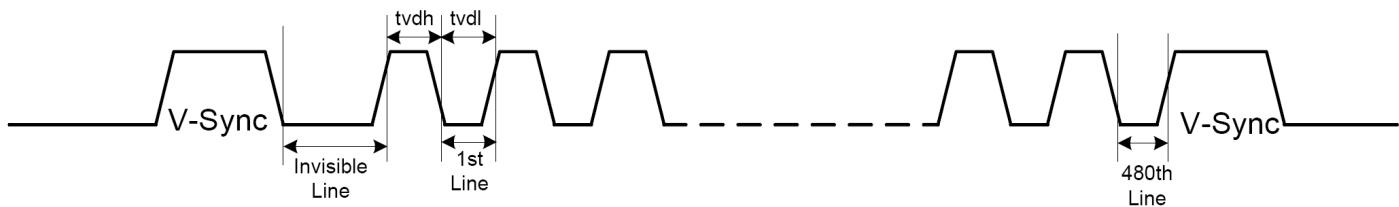
Mode 1 (`set_tear_on`, `TELOM=0`), the Tearing Effect Output signal consists of V-Sync information only:



`tvdh` = The LCD display is not updated from the Frame Memory.

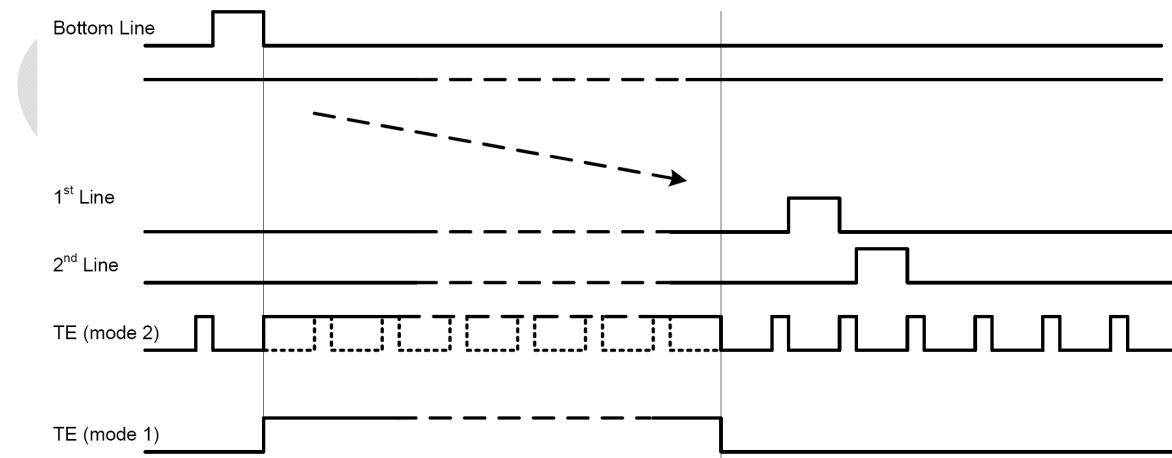
`tvdl` = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

Mode 2 (`set_tear_on`, `TELOM=1`), the tearing effect output signal consists of V-Sync and H-Sync information; there is one V-sync and 480 H-sync pulses per field:



`thdh` = The LCD display is not updated from the Frame Memory.

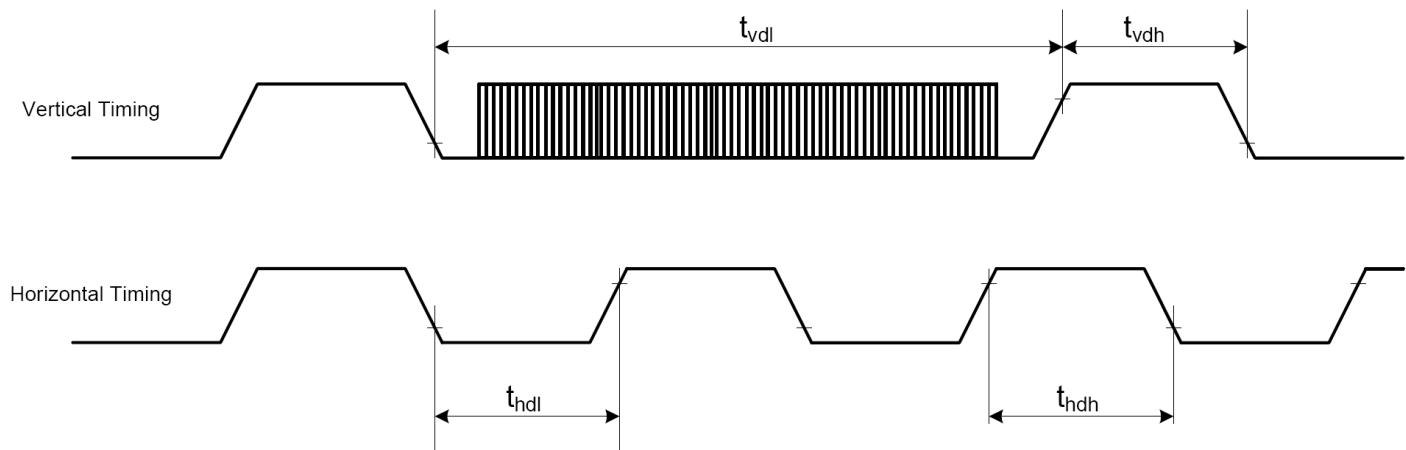
`thdl` = The LCD display is updated from the Frame Memory (except Invisible Line – see above).



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

10.2. Tearing Effect Line Timings

The tearing effect signal is described as below:

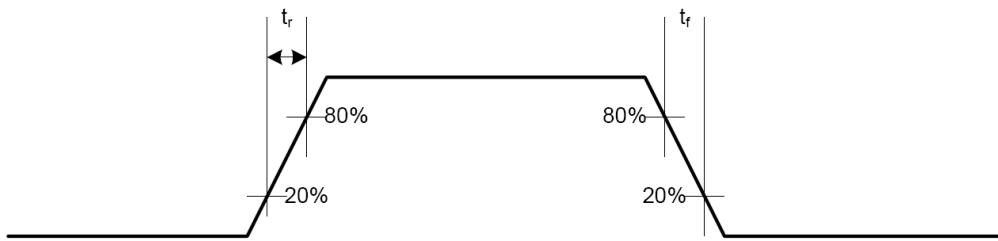


AC characteristics of Tearing Effect Signal (Frame Rate = 60.5Hz)

Symbol	Parameter	Min.	Max.	Unit	Description
t_{vdl}	Vertical timing low duration	TBD		ms	
t_{vdh}	Vertical timing high duration	TBD		us	
t_{hdl}	Horizontal timing low duration	TBD		us	
t_{hdh}	Horizontal timing high duration	TBD		us	

Notes:

1. The timings in Table 8.3.1 apply when MADCTL B4=0 and B4=1
2. The signal's rise and fall times (t_f , t_r) are stipulated to be equal to or less than 15ns.



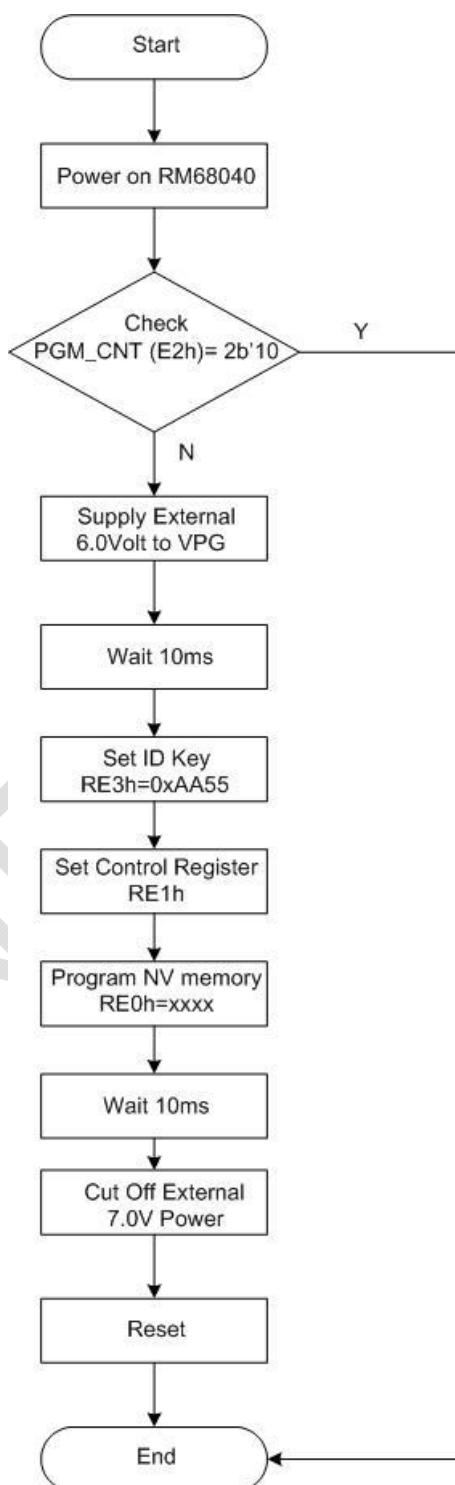
The Tearing Effect Output Line is fed back to the MCU and should be used as shown below to avoid tearing effect:

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The Tearing Effect output line supplies to the MCU a panel synchronization signal. This signal can be enabled or disabled by the set_tear_off(34h), set_tear_on(35h) commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command. The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

TEON (35h)	TEL0M (35h, 1st bit)	TE signal Output
0	*	GND
1	0	TE (Mode 1)
1	1	TE (Mode 2)

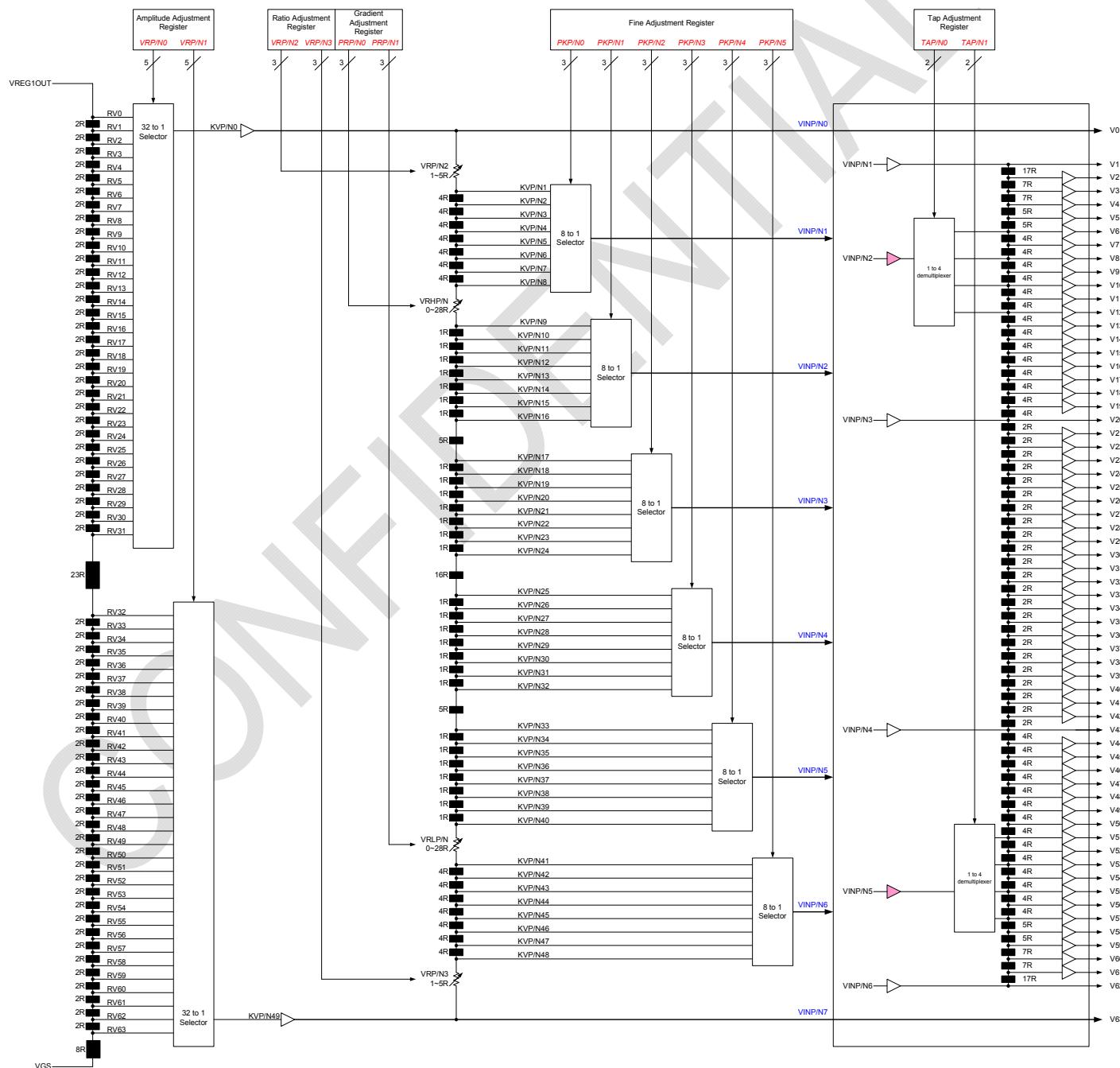
11. NV Memory Programming Flow



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12. Gamma Correction

The RM68041 supports γ -correction function to display in 262,144 colors simultaneously using gradient adjustment, amplitude-adjustment, fine-adjustment, tap-adjustment, and voltage division ratio adjustment registers. Each register consists of positive-polarity register and negative-polarity register to allow optimal gamma correction setting for the characteristics of the panel by enabling different settings for positive and negative polarities.



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Figure 1 Grayscale Voltage Adjustment**1. Gradient adjustment registers**

The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale reference voltage level. To adjust the gradient, the resistance values of variable resistors in the middle of the ladder resistor are adjusted by registers PRP0[2:0]/PRN0[2:0], PRP1[2:0]/PRN1[2:0]. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers, VRP0[3:0]/VRN0[3:0], VRP1[4:0]/VRN1[4:0], are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of variable resistors at the top and bottom of the ladder resistor are adjusted. Same as the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

4.Tap adjustment registers

The tap adjustment registers are for selecting two tap voltage supply points from V6 to V12 and from V51 to V57 by using selector.

5.Voltage division ratio adjustment

The voltage division ratio adjustment registers are used to change the division ratios between V0 and V1 and between V62 and V63.

Table 1 Grayscale voltage calculation formula

Pins	Formula	Pins	Formula
RV0	VREG1OUT	RV32	$VGS + (VREG1OUT - VGS) * (70/155)$
RV1	$VGS + (VREG1OUT - VGS) * (153/155)$	RV33	$VGS + (VREG1OUT - VGS) * (68/155)$
RV2	$VGS + (VREG1OUT - VGS) * (151/155)$	RV34	$VGS + (VREG1OUT - VGS) * (66/155)$
RV3	$VGS + (VREG1OUT - VGS) * (149/155)$	RV35	$VGS + (VREG1OUT - VGS) * (64/155)$

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RV4	VGS+(VREG1OUT-VGS)*(147/155)	RV36	VGS+(VREG1OUT-VGS)*(62/155)
RV5	VGS+(VREG1OUT-VGS)*(145/155)	RV37	VGS+(VREG1OUT-VGS)*(60/155)
RV6	VGS+(VREG1OUT-VGS)*(143/155)	RV38	VGS+(VREG1OUT-VGS)*(58/155)
RV7	VGS+(VREG1OUT-VGS)*(141/155)	RV39	VGS+(VREG1OUT-VGS)*(56/155)
RV8	VGS+(VREG1OUT-VGS)*(139/155)	RV40	VGS+(VREG1OUT-VGS)*(54/155)
RV9	VGS+(VREG1OUT-VGS)*(137/155)	RV41	VGS+(VREG1OUT-VGS)*(52/155)
RV10	VGS+(VREG1OUT-VGS)*(135/155)	RV42	VGS+(VREG1OUT-VGS)*(50/155)
RV11	VGS+(VREG1OUT-VGS)*(133/155)	RV43	VGS+(VREG1OUT-VGS)*(48/155)
RV12	VGS+(VREG1OUT-VGS)*(131/155)	RV44	VGS+(VREG1OUT-VGS)*(46/155)
RV13	VGS+(VREG1OUT-VGS)*(129/155)	RV45	VGS+(VREG1OUT-VGS)*(44/155)
RV14	VGS+(VREG1OUT-VGS)*(127/155)	RV46	VGS+(VREG1OUT-VGS)*(42/155)
RV15	VGS+(VREG1OUT-VGS)*(125/155)	RV47	VGS+(VREG1OUT-VGS)*(40/155)
RV16	VGS+(VREG1OUT-VGS)*(123/155)	RV48	VGS+(VREG1OUT-VGS)*(38/155)
RV17	VGS+(VREG1OUT-VGS)*(121/155)	RV49	VGS+(VREG1OUT-VGS)*(36/155)
RV18	VGS+(VREG1OUT-VGS)*(119/155)	RV50	VGS+(VREG1OUT-VGS)*(34/155)
RV19	VGS+(VREG1OUT-VGS)*(117/155)	RV51	VGS+(VREG1OUT-VGS)*(32/155)
RV20	VGS+(VREG1OUT-VGS)*(115/155)	RV52	VGS+(VREG1OUT-VGS)*(30/155)
RV21	VGS+(VREG1OUT-VGS)*(113/155)	RV53	VGS+(VREG1OUT-VGS)*(28/155)
RV22	VGS+(VREG1OUT-VGS)*(111/155)	RV54	VGS+(VREG1OUT-VGS)*(26/155)
RV23	VGS+(VREG1OUT-VGS)*(109/155)	RV55	VGS+(VREG1OUT-VGS)*(24/155)
RV24	VGS+(VREG1OUT-VGS)*(107/155)	RV56	VGS+(VREG1OUT-VGS)*(22/155)
RV25	VGS+(VREG1OUT-VGS)*(105/155)	RV57	VGS+(VREG1OUT-VGS)*(20/155)
RV26	VGS+(VREG1OUT-VGS)*(103/155)	RV58	VGS+(VREG1OUT-VGS)*(18/155)
RV27	VGS+(VREG1OUT-	RV59	VGS+(VREG1OUT-

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	VGS)*(101/155)		VGS)*(16/155)
RV28	VGS+(VREG1OUT-VGS)*(99/155)	RV60	VGS+(VREG1OUT-VGS)*(14/155)
RV29	VGS+(VREG1OUT-VGS)*(97/155)	RV61	VGS+(VREG1OUT-VGS)*(12/155)
RV30	VGS+(VREG1OUT-VGS)*(95/155)	RV62	VGS+(VREG1OUT-VGS)*(10/155)
RV31	VGS+(VREG1OUT-VGS)*(93/155)	RV63	VGS+(VREG1OUT-VGS)*(8/155)

Variable resistors

The resistance values of these variable resistors are set by gradient adjustment registers and γadjustment registers as follows.

Table 2

Gradient adjustment		Ratio adjustment(1)		Ratio adjustment(2)	
PRP(N)0/1[2:0] Register	VRH/LP(N) Resistance	VRP(N)2[2:0] Register	VRP(N)2[2:0] Resistance	VRP(N)3[2:0] Register	VRP(N)3[2:0] Resistance
000	0R	001	1R	001	1R
001	4R	010	2R	010	2R
010	8R	011	3R	011	3R
011	12R	100	4R	100	4R
100	16R	101	5R	101	5R
101	20R				
110	24R				
111	28R				

Table 3 Grayscale Voltage Calculation Formula (Positive Gamma)

Pins	Formula	Level	Pins	Formula	Level
KVP0	VINP0	VINP1	KVP25	VINP0-ΔV*(VRP2+63R+VRHP)/SUMRP	VINP4
KVP1	VINP0-ΔV*(VRP2)/SUMRP		KVP26	VINP0-ΔV*(VRP2+64R+VRHP)/SUMRP	
KVP2	VINP0-ΔV*(VRP2+4R)/SUMRP		KVP27	VINP0-ΔV*(VRP2+65R+VRHP)/SUMRP	
KVP3	VINP0-ΔV*(VRP2+8R)/SUMRP		KVP28	VINP0-ΔV*(VRP2+66R+VRHP)/SUMRP	
KVP4	VINP0-ΔV*(VRP2+12R)/SUMRP		KVP29	VINP0-ΔV*(VRP2+67R+VRHP)/SUMRP	
KVP5	VINP0-ΔV*(VRP2+16R)/SUMRP		KVP30	VINP0-ΔV*(VRP2+68R+VRHP)/SUMRP	
KVP6	VINP0-ΔV*(VRP2+20R)/SUMRP		KVP31	VINP0-ΔV*(VRP2+69R+VRHP)/SUMRP	
KVP7	VINP0-ΔV*(VRP2+24R)/SUMRP		KVP32	VINP0-ΔV*(VRP2+70R+VRHP)/SUMRP	
KVP8	VINP0-ΔV*(VRP2+28R)/SUMRP		KVP33	VINP0-ΔV*(VRP2+75R+VRHP)/SUMRP	VINP5
KVP9	VINP0-ΔV*(VRP2+28R+VRHP)/SUMRP		KVP34	VINP0-ΔV*(VRP2+76R+VRHP)/SUMRP	

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KVP10	VINP0-ΔV*(VRP2+29R+VRHP)/SUMRP	VINP3	KVP35	VINP0-ΔV*(VRP2+77R+VRHP)/SUMRP	VINP6
KVP11	VINP0-ΔV*(VRP2+30R+VRHP)/SUMRP		KVP36	VINP0-ΔV*(VRP2+78R+VRHP)/SUMRP	
KVP12	VINP0-ΔV*(VRP2+31R+VRHP)/SUMRP		KVP37	VINP0-ΔV*(VRP2+79R+VRHP)/SUMRP	
KVP13	VINP0-ΔV*(VRP2+32R+VRHP)/SUMRP		KVP38	VINP0-ΔV*(VRP2+80R+VRHP)/SUMRP	
KVP14	VINP0-ΔV*(VRP2+33R+VRHP)/SUMRP		KVP39	VINP0-ΔV*(VRP2+81R+VRHP)/SUMRP	
KVP15	VINP0-ΔV*(VRP2+34R+VRHP)/SUMRP		KVP40	VINP0-ΔV*(VRP2+82R+VRHP)/SUMRP	
KVP16	VINP0-ΔV*(VRP2+35R+VRHP)/SUMRP		KVP41	VINP0-ΔV*(VRP2+82R+VRHP+VRLP)/SUMRP	
KVP17	VINP0-ΔV*(VRP2+40R+VRHP)/SUMRP		KVP42	VINP0-ΔV*(VRP2+86R+VRHP+VRLP)/SUMRP	
KVP18	VINP0-ΔV*(VRP2+41R+VRHP)/SUMRP		KVP43	VINP0-ΔV*(VRP2+90R+VRHP+VRLP)/SUMRP	
KVP19	VINP0-ΔV*(VRP2+42R+VRHP)/SUMRP		KVP44	VINP0-ΔV*(VRP2+94R+VRHP+VRLP)/SUMRP	
KVP20	VINP0-ΔV*(VRP2+43R+VRHP)/SUMRP		KVP45	VINP0-ΔV*(VRP2+98R+VRHP+VRLP)/SUMRP	
KVP21	VINP0-ΔV*(VRP2+44R+VRHP)/SUMRP		KVP46	VINP0-ΔV*(VRP2+102R+VRHP+VRLP)/SUMRP	
KVP22	VINP0-ΔV*(VRP2+45R+VRHP)/SUMRP		KVP47	VINP0-ΔV*(VRP2+106R+VRHP+VRLP)/SUMRP	
KVP23	VINP0-ΔV*(VRP2+46R+VRHP)/SUMRP		KVP48	VINP0-ΔV*(VRP2+110R+VRHP+VRLP)/SUMRP	
KVP24	VINP0-ΔV*(VRP2+47R+VRHP)/SUMRP		KVP49	VINP7	VINP7

$$\text{SUMRP} = \text{VRP2} + \text{VRHP} + 110\text{R} + \text{VRLP} + \text{VRP}$$

$$\Delta V = \text{VINP7} - \text{VINP0}$$

Table 4 Grayscale Voltage Calculation Formula (Negative Gamma)

Pins	Formula	Level	Pins	Formula	Level
KVN0	VINN0	VINN1	KVN25	VINN0-ΔV*(VRN2+63R+VRHN)/SUMRN	VINN4
KVN1	VINN0-ΔV*(VRN2)/SUMRN		KVN26	VINN0-ΔV*(VRN2+64R+VRHN)/SUMRN	
KVN2	VINN0-ΔV*(VRN2+4R)/SUMRN		KVN27	VINN0-ΔV*(VRN2+65R+VRHN)/SUMRN	
KVN3	VINN0-ΔV*(VRN2+8R)/SUMRN		KVN28	VINN0-ΔV*(VRN2+66R+VRHN)/SUMRN	
KVN4	VINN0-ΔV*(VRN2+12R)/SUMRN		KVN29	VINN0-ΔV*(VRN2+67R+VRHN)/SUMRN	
KVN5	VINN0-ΔV*(VRN2+16R)/SUMRN		KVN30	VINN0-ΔV*(VRN2+68R+VRHN)/SUMRN	
KVN6	VINN0-ΔV*(VRN2+20R)/SUMRN		KVN31	VINN0-ΔV*(VRN2+69R+VRHN)/SUMRN	
KVN7	VINN0-ΔV*(VRN2+24R)/SUMRN		KVN32	VINN0-ΔV*(VRN2+70R+VRHN)/SUMRN	
KVN8	VINN0-ΔV*(VRN2+28R)/SUMRN		KVN33	VINN0-ΔV*(VRN2+75R+VRHN)/SUMRN	VINN5
KVN9	VINN0-ΔV*(VRN2+28R+VRHN)/SUMRN		KVN34	VINN0-ΔV*(VRN2+76R+VRHN)/SUMRN	
KVN10	VINN0-ΔV*(VRN2+29R+VRHN)/SUMRN		KVN35	VINN0-ΔV*(VRN2+77R+VRHN)/SUMRN	
KVN11	VINN0-ΔV*(VRN2+30R+VRHN)/SUMRN		KVN36	VINN0-ΔV*(VRN2+78R+VRHN)/SUMRN	
KVN12	VINN0-ΔV*(VRN2+31R+VRHN)/SUMRN		KVN37	VINN0-ΔV*(VRN2+79R+VRHN)/SUMRN	
KVN13	VINN0-ΔV*(VRN2+32R+VRHN)/SUMRN		KVN38	VINN0-ΔV*(VRN2+80R+VRHN)/SUMRN	
KVN14	VINN0-ΔV*(VRN2+33R+VRHN)/SUMRN		KVN39	VINN0-ΔV*(VRN2+81R+VRHN)/SUMRN	
KVN15	VINN0-ΔV*(VRN2+34R+VRHN)/SUMRN		KVN40	VINN0-ΔV*(VRN2+82R+VRHN)/SUMRN	

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KVN16	VINN0-ΔV*(VRN2+35R+VRHN)/SUMRN	VINN3	KVN41	VINN0-ΔV*(VRN2+82R+VRHN+VRLN)/SUMRN	VINN6
KVN17	VINN0-ΔV*(VRN2+40R+VRHN)/SUMRN		KVN42	VINN0-ΔV*(VRN2+86R+VRHN+VRLN)/SUMRN	
KVN18	VINN0-ΔV*(VRN2+41R+VRHN)/SUMRN		KVN43	VINN0-ΔV*(VRN2+90R+VRHN+VRLN)/SUMRN	
KVN19	VINN0-ΔV*(VRN2+42R+VRHN)/SUMRN		KVN44	VINN0-ΔV*(VRN2+94R+VRHN+VRLN)/SUMRN	
KVN20	VINN0-ΔV*(VRN2+43R+VRHN)/SUMRN		KVN45	VINN0-ΔV*(VRN2+98R+VRHN+VRLN)/SUMRN	
KVN21	VINN0-ΔV*(VRN2+44R+VRHN)/SUMRN		KVN46	VINN0-ΔV*(VRN2+102R+VRHN+VRLN)/SUMRN	
KVN22	VINN0-ΔV*(VRN2+45R+VRHN)/SUMRN		KVN47	VINN0-ΔV*(VRN2+106R+VRHN+VRLN)/SUMRN	
KVN23	VINN0-ΔV*(VRN2+46R+VRHN)/SUMRN		KVN48	VINN0-ΔV*(VRN2+110R+VRHN+VRLN)/SUMRN	
KVN24	VINN0-ΔV*(VRN2+47R+VRHN)/SUMRN		KVN49	VINN7	
					VINN7

SUMRN=VRN2+VRHN+110R+VRLN+VRN3

ΔV=VINN7-VINN0

Ladder resistors and 8-to-1 selector Block configuration

The reference voltage generating block consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the γ -correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels

Table 5

Fine Adjustment(1)		Fine Adjustment(2)		Fine Adjustment(3)	
VINP/N1 Level	PKP/N0[2:0]	VINP/N2 Level	PKP/N1[2:0]	VINP/N3 Level	PKP/N2[2:0]
KVP/N1	000	KVP/N9	000	KVP/N17	000
KVP/N2	001	KVP/N10	001	KVP/N18	001
KVP/N3	010	KVP/N11	010	KVP/N19	010
KVP/N4	011	KVP/N12	011	KVP/N20	011
KVP/N5	100	KVP/N13	100	KVP/N21	100
KVP/N6	101	KVP/N14	101	KVP/N22	101
KVP/N7	110	KVP/N15	110	KVP/N23	110
KVP/N8	111	KVP/N16	111	KVP/N24	111
Fine Adjustment(4)		Fine Adjustment(5)		Fine Adjustment(6)	
VINP/N4 Level	PKP/N3[2:0]	VINP/N5 Level	PKP/N4[2:0]	VINP/N6 Level	PKP/N5[2:0]
KVP/N25	000	KVP/N33	000	KVP/N41	000
KVP/N26	001	KVP/N34	001	KVP/N42	001
KVP/N27	010	KVP/N35	010	KVP/N43	010
KVP/N28	011	KVP/N36	011	KVP/N44	011

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KVP/N29	100	KVP/N37	100	KVP/N45	100
KVP/N30	101	KVP/N38	101	KVP/N46	101
KVP/N31	110	KVP/N39	110	KVP/N47	110
KVP/N32	111	KVP/N40	111	KVP/N48	111

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13. Electrical Characteristics

13.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When RM68041 is used out of the absolute maximum ratings, the RM68041 may be permanently damaged. To use the RM68041 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the RM68041 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power supply voltage	IOVCC	V	-0.3 ~ + 4.6	1,
Power supply voltage	VCI - GND	V	-0.3 ~ + 4.6	2
Power supply voltage	DDVDH - GND	V	-0.3 ~ + 6.5	3
Power supply voltage	GND - VCL	V	-0.3 ~ + 4.6	4
Power supply voltage	DDVDH - VCL	V	-0.3 ~ + 9.0	
Power supply voltage	VGH - GND	V	-0.3 ~ + 18.5	
Power supply voltage	GND - VGL	V	-0.3 ~ + 18.5	
Power supply voltage	VGH - VGL	V	-0.3 ~ + 32	
Input voltage	Vt	V	-0.3 ~ IOVCC+ 0.3	
Operating temperature	Topr	°C	-40 ~ + 85	8, 9
Storage temperature	Tstg	°C	-55 ~ + 110	8, 9

Notes:

1. Make sure IOVCC \geq GND
2. Make sure VCI \geq AGND.
3. Make sure DDVDH \geq VCL and DDVDH \geq VCI
4. Make sure AGND \geq VGL.

13.2. DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog Power Supply	VCI	Analog Operation Voltage	2.5	2.8	3.3	V
I/O pin Power Supply	IOVCC	I/O pin Operation Voltage	1.65	2.8	3.3	V
Logic High level input	VIH	IOVCC = 1.65V ~ 3.3V	0.7*IOVCC	-	IOVCC	V
Logic Low level input	VIL	IOVCC = 1.65V ~ 3.3V	0.0	-	0.3*IOVCC	V
Logic High level	VIH	Iout = -1 mA	0.8*IOVCC	-	IOVCC	V
Logic Low level	VIL	Iout = +1 mA	0.0	-	0.2*IOVCC	V
Logic High level input	IIHD	D[17:0]			10	uA
Logic Low level input	IILD	D[17:0]	-10			uA

13.3. AC Characteristics

13.3.1. Reset timing

Reset Timing

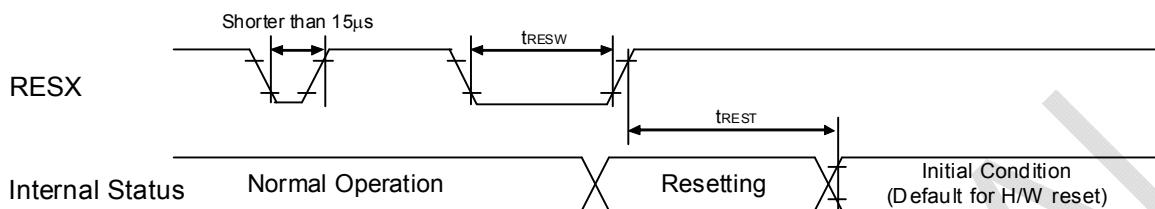


Table 8.18.4.1 Reset input timing

IOVCC=1.65 to 3.3V, VCI=2.5 to 3.3V, AGND=DGND=0V, Ta=-40 to 85°C

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
tRESW	*1) Reset low pulse width	RESX	15	-	-	-	μs
tREST	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

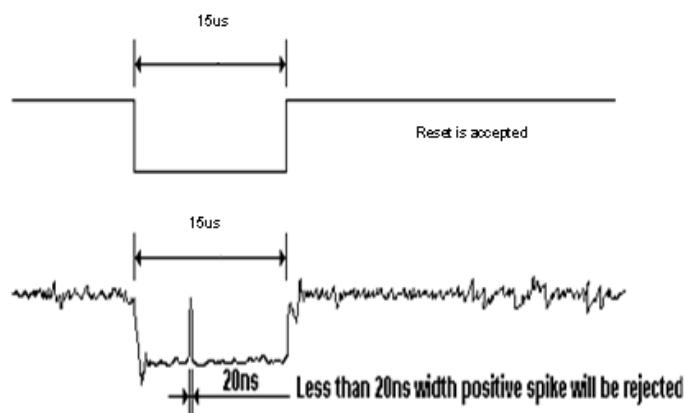
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 15μs	Reset
Between 5μs and 15μs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

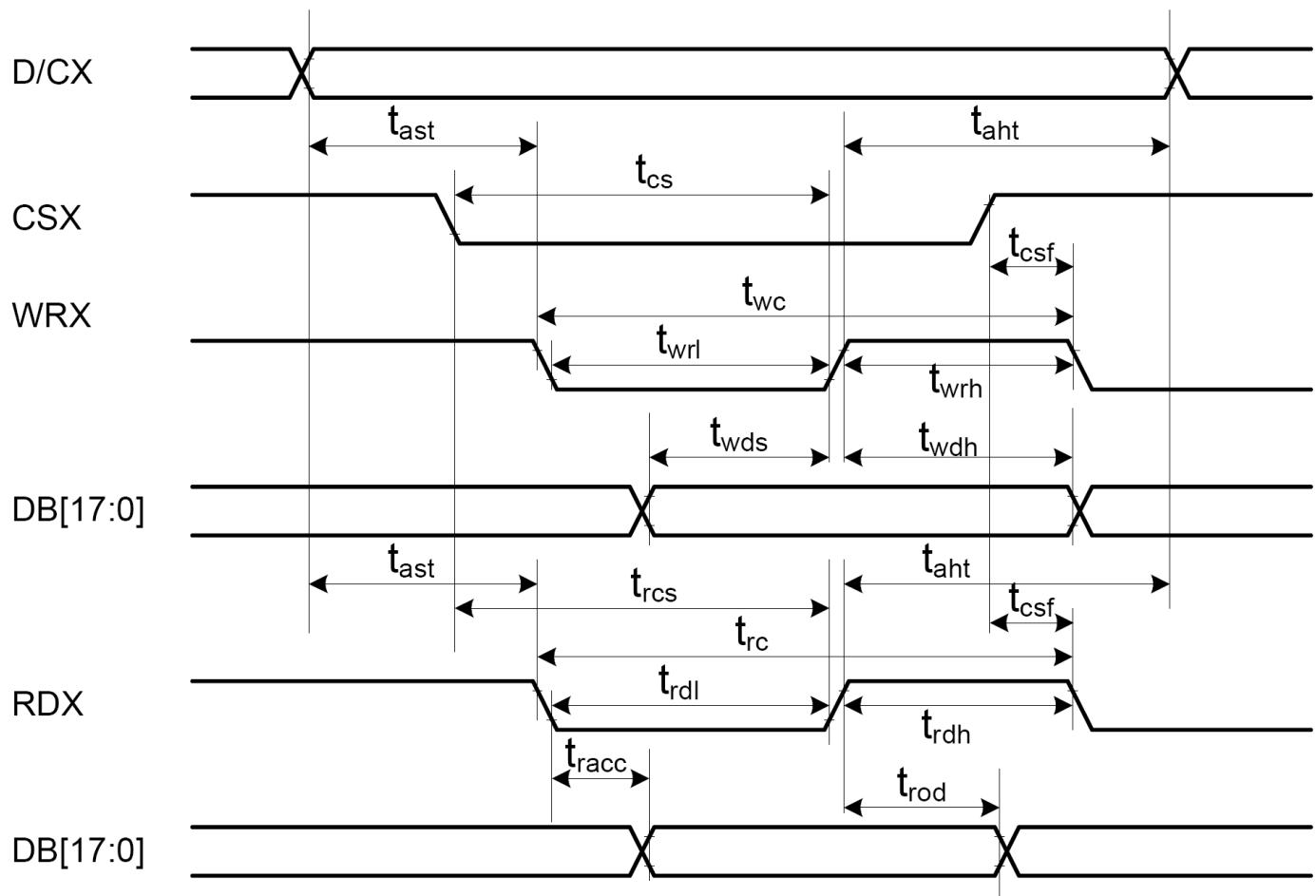
Note 3. During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

13.3.2. DBI Type B (18/16/9/8 bit) Interface Timing Characteristics

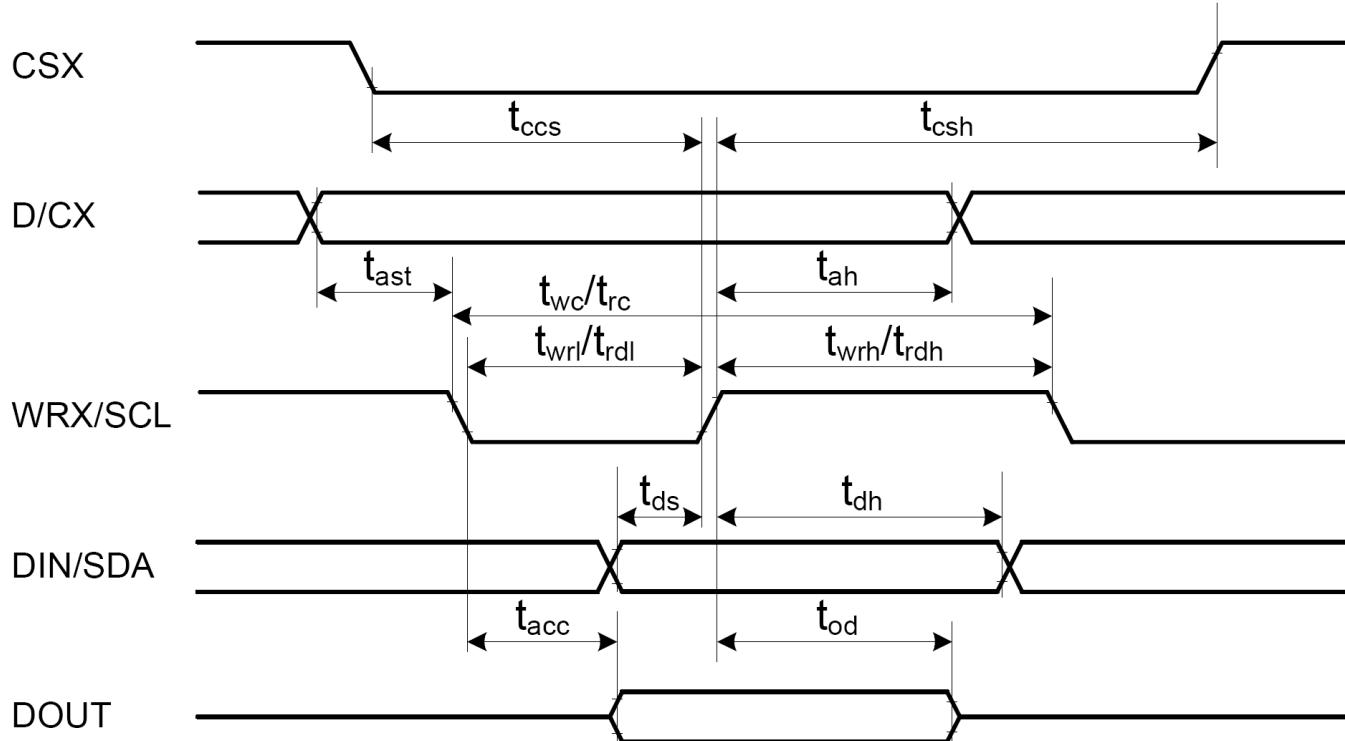


Signal	Symbol	Parameter	min	max	Unit	Description
D/CX	tast	Address setup time	10	-	ns	
	taht	Address hold time (Write/Read)	10	-	ns	
CSX	tcs	Chip Select setup time (Write)	20	-	ns	
	trcs	Chip Select setup time (Read)	20	-	ns	
	tcsf	Chip Select Wait time	20	-	ns	
WRX	twc	Write cycle	100	-	ns	
	twrh	Write Control pulse H duration	30	-	ns	
	twrl	Write Control pulse L duration	25	-	ns	
RDX	trc	Read cycle	450	-	ns	
	trdh	Read Control pulse H duration	250	-	ns	
	trdl	Read Control pulse L duration	170	-	ns	
DB[17:0], DB[15:0], DB[8:0], DB[7:0]	twds	Write data setup time	15	-	ns	For maximum CL=30pF
	twdh	Write data hold time	25	-	ns	
	tracc	Read access time	10	340	ns	For minimum CL=8pF
	trod	Read output disable time	10	-	ns	

Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, GND=0V

13.3.3. DBI Type C Interface Timing Characteristics

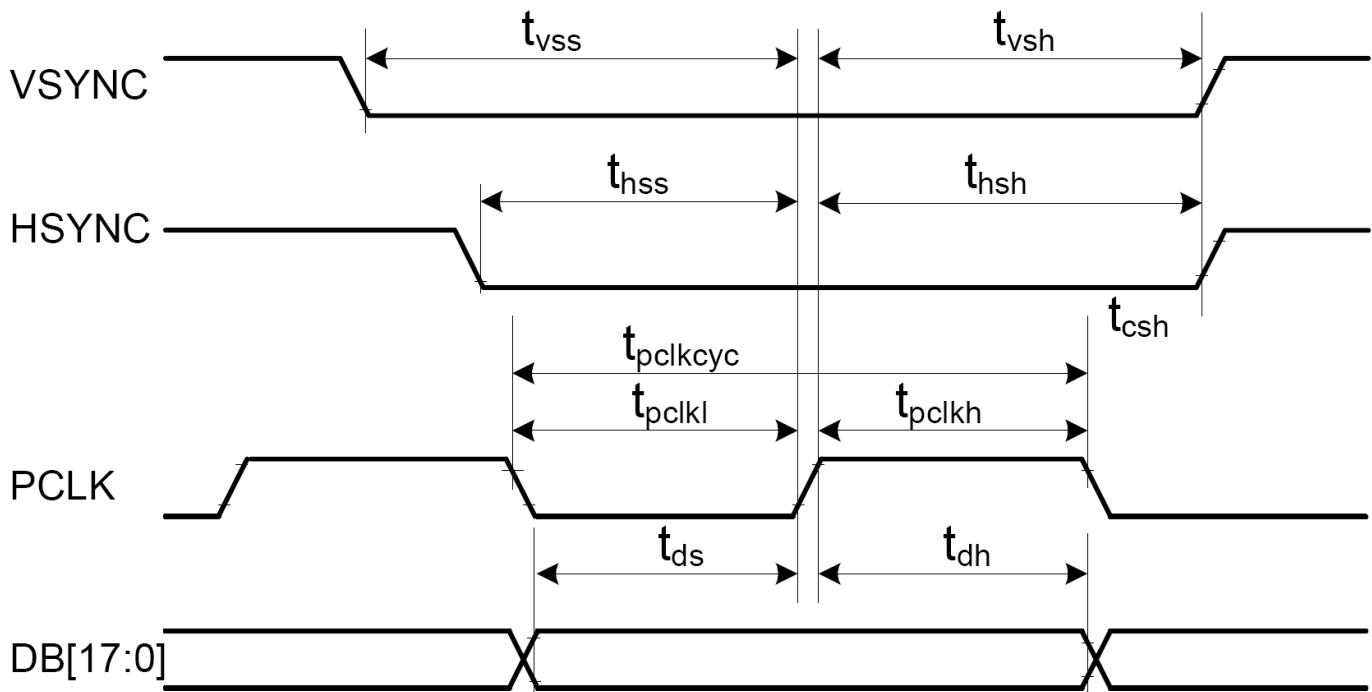


Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	tcss	Chip select setup time (Write)	40	-	ns	
	tcsh	Chip select hold time (Write)	40	-	ns	
D/CX	tas	Address setup time	10		ns	

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	tah	Address hold time (Write/Read)	10		ns	
WRX/SCL (Write)	twc	Write cycle	100		ns	
	twrh	SCL High duration (write)	40		ns	
	twrl	SCL Low duration (write)	40		ns	
	trc	Read cycle	300		ns	
WRX/SCL (Read)	trdh	SCL High duration (read)	120		ns	
	trdl	SCL Low duration (read)	120		ns	
	tds	Data setup time	30		ns	
DIN/SDA (Driver IC)	tdh	Data hold time	30		ns	
	tacc	Access time	-	110	ns	
DOUT (Driver IC)	tod	Output disable time	10		ns	

13.3.3. DPI Interface Timing Characteristics



Parameter	Symbol	Condition	Min.	Max.	Unit
Vsync Setup Time	t_{vss}		15	-	ns
Vsync Hold Time	t_{vsh}		15	-	ns
Hsync Setup Time	t_{hss}		15	-	ns
Hsync Hold Time	t_{hsh}		15	-	ns
Pixel Clock Duty Cycle	$t_{pclkcyc}$		33	67	%
Pixel Clock Low Duration	t_{pclkl}		15	-	ns
Pixel Clock High Duration	t_{pclkh}		15	-	ns
Data Setup Time	t_{ds}		15	-	ns
Data Hold Time	t_{dh}		15	-	ns

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