National Institute of Technology, Calicut

Computer Science & Engineering Department

CS6122E: Computer Architecture & Design

Assignment-2

Important Instructions

➔ This is a group Assignment.

➔ Everyone in a group must submit a report (pdf), with all necessary plots and explanations, on EduServer for this assignment. Everyone in the group can have the same report, but the report must include a work distribution section.

➔ For all of the tasks, you need to use the **GEM5** simulator.

➔ For all simulations, you must warm up for the first **50M instructions** and do a detailed simulation for **50M instructions**.

➔ Each team will be given four specific benchmarks and a specific 'i' used in LRU_i for the experiments which can be found at the link.

Table 1: List of applications to be simulated

astar	hmmer	milc	specrand_integer
bzip2	lbm	namd	gobmk
gamess	mcf	sphinx3	libquantum

Table 2: Baseline System Configuration

Parameter	Value
Core	OoO, Single Core
Frequency	3 GHz
Fetch/Decode/Issue/Commit Width	2
IQ/LSQ size	64/32
ROB size	192
Branch Predictor	Tage SC-L Predictor
BTB/RAS size	4K/32
Cache Block Size	64 Bytes
L1 I-cache	32 KB, 4-way, 3-cycle latency, 32 MSHRs, LRU
L1 D-cache	32 KB, 4-way, 3-cycle latency, 32 MSHRs, LRU
L2 Cache (LLC)	256 KB, 16-way, 9-cycle latency, 32 MSHRs, LRU, Best Offset Prefetcher (BOP)
Main Memory	4 GB, DDR3 1600 MHz

MIP Replacement Policy

- The *LRU_i* cache replacement policy is for the last-level cache (LLC).
- **Insertion Policy:** *LRU_i* inserts the cache block at the **i**[th] position in the MRU recency stack, where 0 is MRU, and 15 is LRU. For example, LRU_0 will insert the incoming block at the MRU position in the MRU recency stack. LRU_15, which will insert the incoming cache block at the LRU position, is the same as the baseline LRU replacement policy
- **Eviction Policy:** The eviction policy of *LRU_i* is the same as the LRU policy. The cache block at the LRU position in the recency stack is the eviction candidate.
- **Promotion/Update Policy:** The update policy of *LRU_i* is also the same as the LRU policy. On a hit, the cache block is moved to the MRU position in the recency stack.

Tasks

1. Implement the *LRU_i* cache replacement policy for the last-level cache (LLC). Analyze the applications listed in Table 1 using both LRU and LRU_i as the replacement policies for the LLC.
2. For each group the value of **i = (sum of roll numbers of all team members) mod 15**
3. Analyse and compare the results of both simulated policies (LRU, LRU_i).
4. Identify the best-performing cache replacement policy among them.
5. Provide all necessary plots and a detailed explanation to justify your conclusion.
6. Plots may include the miss rate of LLC, MPKI (misses per kilo instructions) of LLC and IPC (instructions per cycle) for both replacement policies.

Evaluation Guidelines

- For the plots, use the LRU as the baseline LLC replacement policy and normalize the parameters for other the *LRU_i* replacement policy with respect to the baseline configuration.
- Use absolute values for LLC miss rate comparison.