SOC Design Laboratory

Lab4-1 Execute Code in User Memory

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一、Firmware:

1.FIR algorithm

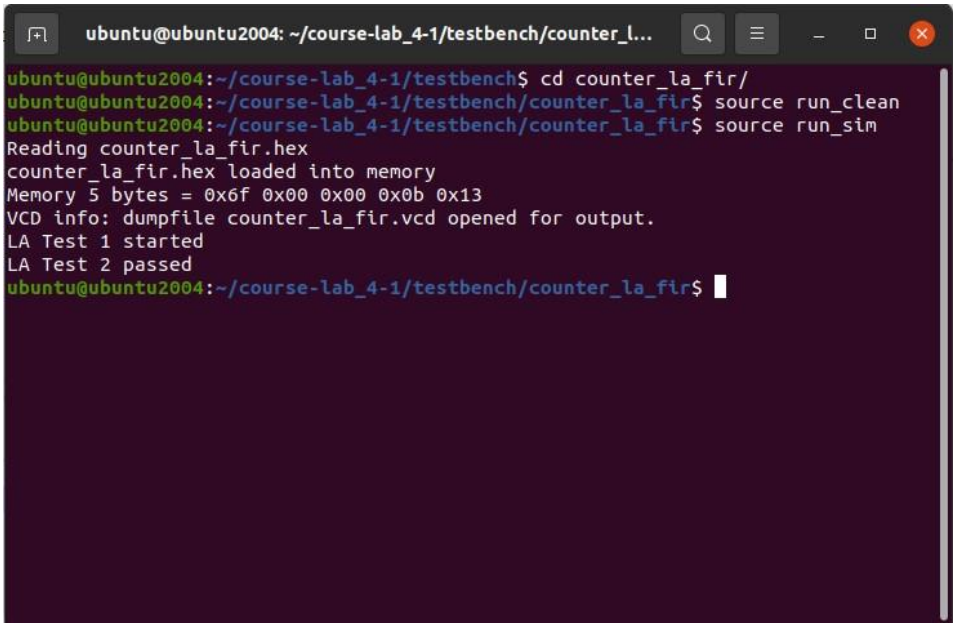
運用兩個 for 迴圈執行 tap 與 data 交叉相成的動作並累加後輸出。

2.Space

Firmware code space is about 32kb (N=10)

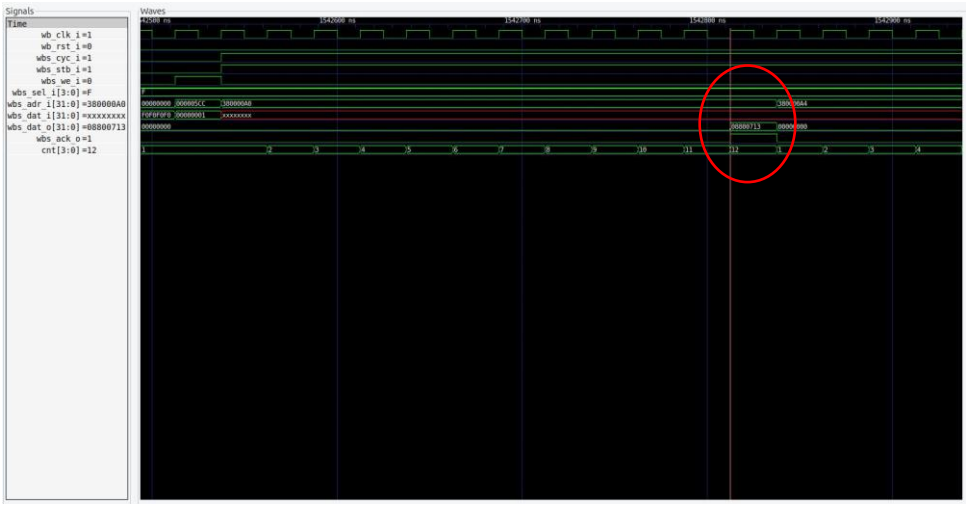
二、Interface:

Simulation 結果:



Checkbits 讀取到 AB40

Counter 等於 12 時，wbs_ack_o 升起，接收 BRAM 讀出的值。



三、Synthesis report:

Timing report:

Frequency:100MHZ

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Max Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             6.899ns  (required time - arrival time)
  Source:                 cnt_reg[2]/C
                            (rising edge-triggered cell FDRE clocked by wb_clk_i  {rise@0.000ns fall@5.000ns period=10.000ns})
  Destination:            user_bram/RAM_reg/WEA[0]
                            (rising edge-triggered cell RAMB36E1 clocked by wb_clk_i  {rise@0.000ns fall@5.000ns period=10.000ns})
  Path Group:             wb_clk_i
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (wb_clk_i rise@10.000ns - wb_clk_i rise@0.000ns)
  Data Path Delay:        2.389ns  (logic 0.773ns (32.361%)  route 1.616ns (67.639%))
  Logic Levels:           1  (LUT4=1)
  Clock Path Skew:        -0.145ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    2.128ns = ( 12.128 - 10.000 )
    Source Clock Delay      (SCD):    2.456ns
    Clock Pessimism Removal (CPR):    0.184ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns
```

```
  Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
-------------------------------------------------------------------    -------------------
                     (clock wb_clk_i rise edge)
                                                  0.000     0.000 r
                                                  0.000     0.000 r  wb_clk_i (IN)
                     net (fo=0)                   0.000     0.000    wb_clk_i
                                                                 r  wb_clk_i_IBUF_inst/I
                     IBUF (Prop_ibuf_I_O)         0.972     0.972 r  wb_clk_i_IBUF_inst/O
                     net (fo=1, unplaced)         0.800     1.771    wb_clk_i_IBUF
                                                                 r  wb_clk_i_IBUF_BUFG_inst/I
                     BUFG (Prop_bufg_I_O)         0.101     1.872 r  wb_clk_i_IBUF_BUFG_inst/O
                     net (fo=6, unplaced)         0.584     2.456    wb_clk_i_IBUF_BUFG
                     FDRE                                        r  cnt_reg[2]/C
-------------------------------------------------------------------    -------------------
                     FDRE (Prop_fdre_C_Q)         0.478     2.934 r  cnt_reg[2]/Q
                     net (fo=37, unplaced)        0.816     3.750    user_bram/Q[2]
                                                                 r  user_bram/RAM_reg_i_2/I1
                     LUT4 (Prop_lut4_I1_O)        0.295     4.045 r  user_bram/RAM_reg_i_2/O
                     net (fo=4, unplaced)         0.800     4.845    user_bram/we[3]
                     RAMB36E1                                    r  user_bram/RAM_reg/WEA[0]
-------------------------------------------------------------------    -------------------

                     (clock wb_clk_i rise edge)
                                                 10.000    10.000 r
                                                  0.000    10.000 r  wb_clk_i (IN)
                     net (fo=0)                   0.000    10.000    wb_clk_i
                                                                 r  wb_clk_i_IBUF_inst/I
                     IBUF (Prop_ibuf_I_O)         0.838    10.838 r  wb_clk_i_IBUF_inst/O
                     net (fo=1, unplaced)         0.760    11.598    wb_clk_i_IBUF
                                                                 r  wb_clk_i_IBUF_BUFG_inst/I
                     BUFG (Prop_bufg_I_O)         0.091    11.689 r  wb_clk_i_IBUF_BUFG_inst/O
                     net (fo=6, unplaced)         0.439    12.128    user_bram/CLK
                     RAMB36E1                                    r  user_bram/RAM_reg/CLKARDCLK
                     clock pessimism              0.184    12.311
                     clock uncertainty           -0.035    12.276
                     RAMB36E1 (Setup_ramb36e1_CLKARDCLK_WEA[0])
                                                 -0.532    11.744    user_bram/RAM_reg
-------------------------------------------------------------------
                     required time                         11.744
                     arrival time                          -4.845
-------------------------------------------------------------------
                     slack                                  6.899
```

Utilization:

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1. Slice Logic
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+-------------------------+------+-------+------------+-----------+-------+
|        Site Type        | Used | Fixed | Prohibited | Available | Util% |
+-------------------------+------+-------+------------+-----------+-------+
| Slice LUTs*             |   38 |     0 |          0 |     53200 |  0.07 |
|   LUT as Logic          |   38 |     0 |          0 |     53200 |  0.07 |
|   LUT as Memory         |    0 |     0 |          0 |     17400 |  0.00 |
| Slice Registers         |    4 |     0 |          0 |    106400 | <0.01 |
|   Register as Flip Flop |    4 |     0 |          0 |    106400 | <0.01 |
|   Register as Latch     |    0 |     0 |          0 |    106400 |  0.00 |
| F7 Muxes                |    0 |     0 |          0 |     26600 |  0.00 |
| F8 Muxes                |    0 |     0 |          0 |     13300 |  0.00 |
+-------------------------+------+-------+------------+-----------+-------+
```

四、Discovery:

Wbs_cyc_i 和 wbs_we_i 並沒有同步，所以需要在兩者皆為 1，且 counter 為 10 時，才能將 we 升起，寫入 BRAM，否則會寫入錯的值以至於程式無法運行。