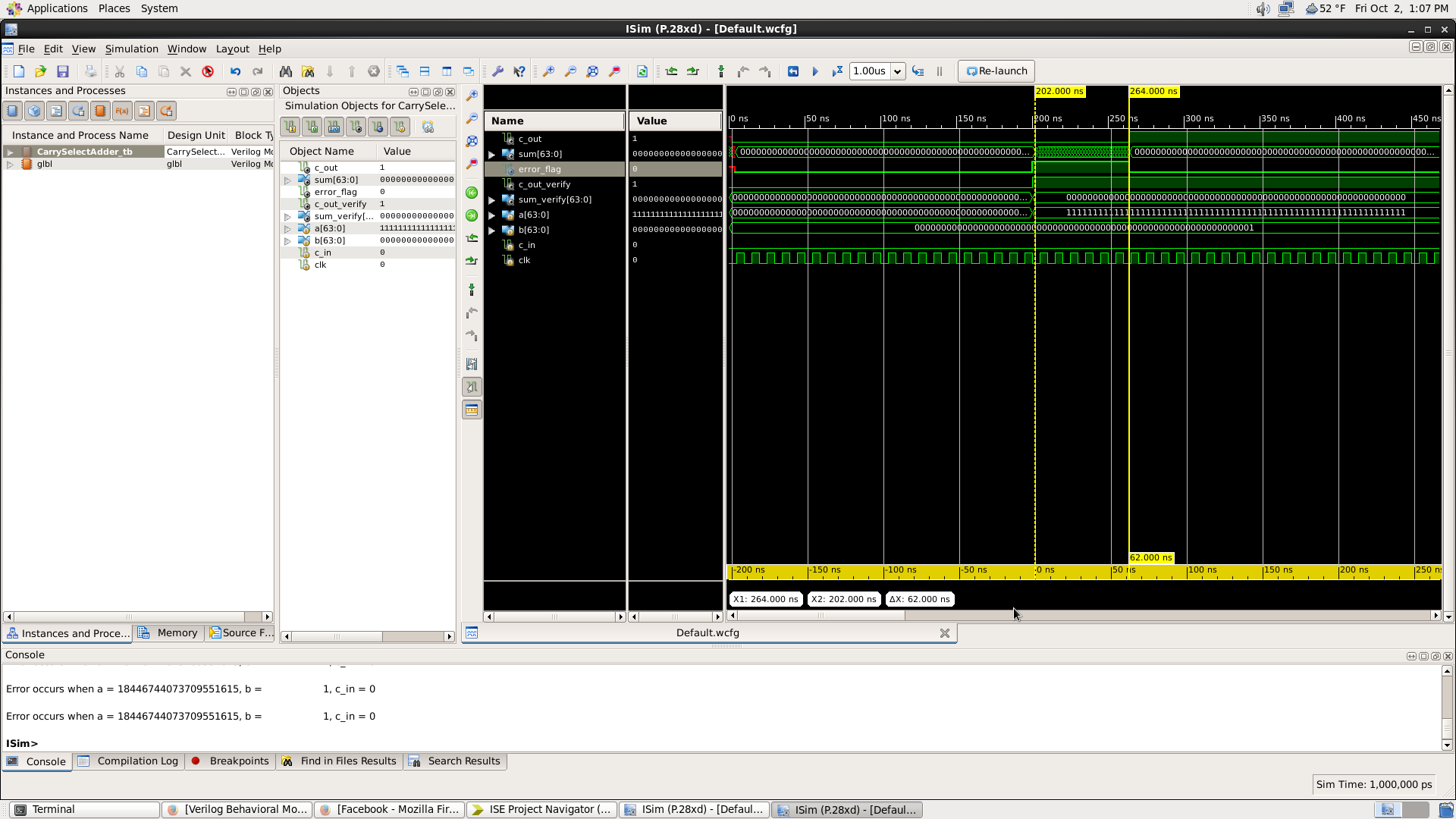
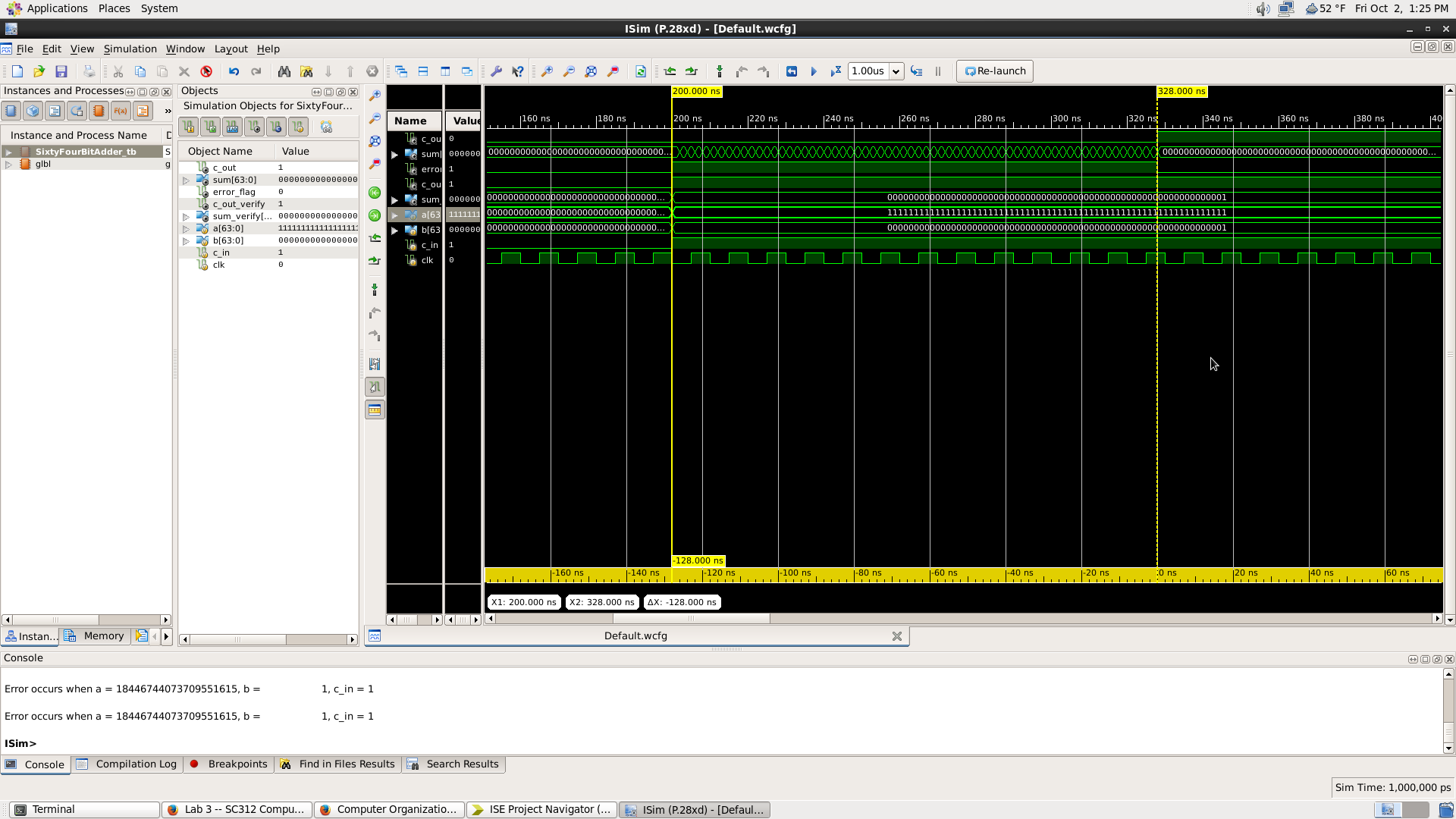
Computer Organization lab 4 write up

The modules I used to build the 64 bit ripple carry adders were the 16 bit adders, 4 bit adders, and the full adders. The 4 bit adders consisted of 4 full adders, the 16 bit adders consisted of 4 4-bit adders, and the 64-bit adder consisted of 4 16-bit adders.



The time delay for the ripple carry adder was 128 ns. This is what I expected because each full adder has a delay of 2 ns and to make a 64 bit ripple carry adder, you need 64 full adders. So when you multiple the 2ns delay 64 times it becomes 128ns, which is what was shown in the waveform diagram.

The delay time for the carry select adder was 64ns in the simulation. Since the adders are running in parallel and it is made up of 32 bit adders, the delay will only be 2ns \* 32 which becomes 64ns. But in actuality the delay should be 66ns because the mux has a 2ns delay, which is not counted in the simulation.